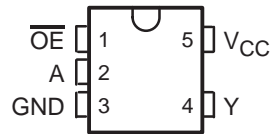


# SN74LVC1G125 SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

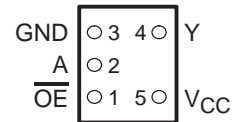
SCES223M – APRIL 1999 – REVISED APRIL 2005

- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Supports 5-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 3.7 ns at 3.3 V
- Low Power Consumption, 10- $\mu$ A Max  $I_{CC}$
- $\pm 24$ -mA Output Drive at 3.3 V
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

DBV, DCK, OR DRL PACKAGE  
(TOP VIEW)



YEA, YEP, YZA, OR YZP PACKAGE  
(BOTTOM VIEW)



## description/ordering information

This bus buffer gate is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC1G125 is a single line driver with a 3-state output. The output is disabled when the output-enable (OE) input is high.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.17-mm Small Bump – YEA	Reel of 3000	SN74LVC1G125YEAR	---CM_
	NanoFree™ – WCSP (DSBGA) 0.17-mm Small Bump – YZA (Pb-free)		SN74LVC1G125YZAR	
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP		SN74LVC1G125YEPR	
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74LVC1G125YZPR	
	SOT (SOT-23) – DBV	Reel of 3000	SN74LVC1G125DBVR	C25_
		Reel of 250	SN74LVC1G125DBVT	
	SOT (SC-70) – DCK	Reel of 3000	SN74LVC1G125DCKR	CM_
		Reel of 250	SN74LVC1G125DCKT	
	SOT (SOT-533) – DRL	Reel of 4000	SN74LVC1G125DRLR	PREVIEW

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

‡ DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.

YEA/YZA, YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar and NanoFree are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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# SN74LVC1G125

## SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

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### description/ordering information (continued)

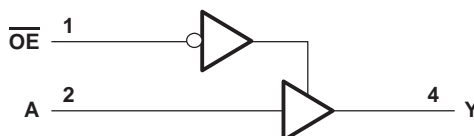
This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

### logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 6.5 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Continuous output current, $I_O$	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND	$\pm 100$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 3):	
DBV package	206°C/W
DCK package	252°C/W
DRL package	142°C/W
YEA/YZA package	154°C/W
YEP/YZP package	132°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  2. The value of  $V_{CC}$  is provided in the recommended operating conditions table.
  3. The package thermal impedance is calculated in accordance with JESD 51-7.

**SN74LVC1G125**  
**SINGLE BUS BUFFER GATE**  
**WITH 3-STATE OUTPUT**

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**recommended operating conditions (see Note 4)**

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
		V <sub>CC</sub> = 3 V to 3.6 V	2		
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.35 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7		
		V <sub>CC</sub> = 3 V to 3.6 V	0.8		
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.3 × V <sub>CC</sub>		
V <sub>I</sub>	Input voltage	0	5.5	V	
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V	–4		mA
		V <sub>CC</sub> = 2.3 V	–8		
		V <sub>CC</sub> = 3 V	–16		
		V <sub>CC</sub> = 4.5 V	–24		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V	4		mA
		V <sub>CC</sub> = 2.3 V	8		
		V <sub>CC</sub> = 3 V	16		
		V <sub>CC</sub> = 4.5 V	32		
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V	20		ns/V
		V <sub>CC</sub> = 3.3 V ± 0.3 V	10		
		V <sub>CC</sub> = 5 V ± 0.5 V	5		
T <sub>A</sub>	Operating free-air temperature	–40	85	°C	

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



# SN74LVC1G125

## SINGLE BUS BUFFER GATE

### WITH 3-STATE OUTPUT

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>		I <sub>OH</sub> = -100 μA	1.65 V to 5.5 V	V <sub>CC</sub> - 0.1			V
		I <sub>OH</sub> = -4 mA	1.65 V	1.2			
		I <sub>OH</sub> = -8 mA	2.3 V	1.9			
		I <sub>OH</sub> = -16 mA	3 V	2.4			
		I <sub>OH</sub> = -24 mA		2.3			
		I <sub>OH</sub> = -32 mA	4.5 V	3.8			
V <sub>OL</sub>		I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V			0.1	V
		I <sub>OL</sub> = 4 mA	1.65 V			0.45	
		I <sub>OL</sub> = 8 mA	2.3 V			0.3	
		I <sub>OL</sub> = 16 mA	3 V			0.4	
		I <sub>OL</sub> = 24 mA				0.55	
		I <sub>OL</sub> = 32 mA	4.5 V			0.55	
I <sub>I</sub>	A or $\overline{OE}$ inputs	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±5	μA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0			±10	μA
I <sub>OZ</sub>		V <sub>O</sub> = 0 to 5.5 V	3.6 V			10	μA
I <sub>CC</sub>		V <sub>I</sub> = 5.5 V or GND, I <sub>O</sub> = 0	1.65 V to 5.5 V			10	μA
ΔI <sub>CC</sub>		One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V			500	μA
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V			4	pF

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 15 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	1.9	6.9	0.7	4.6	0.6	3.7	0.5	3.4	ns

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 30 pF or 50 pF (unless otherwise noted) (see Figure 2)

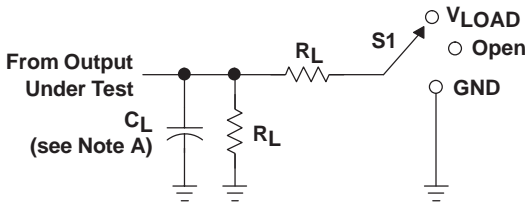
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	2.8	9	1.2	5.5	1	4.5	1	4	ns
t <sub>en</sub>	$\overline{OE}$	Y	3.3	10.1	1.5	6.6	1	5.3	1	5	ns
t <sub>dis</sub>	$\overline{OE}$	Y	1.3	9.2	1	5	1	5	1	4.2	ns

operating characteristics, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz	18	18	19	21	pF
			Outputs enabled	2	2	2	



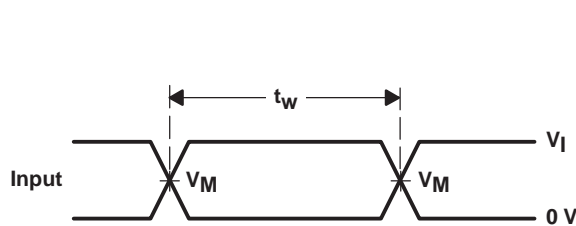
**PARAMETER MEASUREMENT INFORMATION**



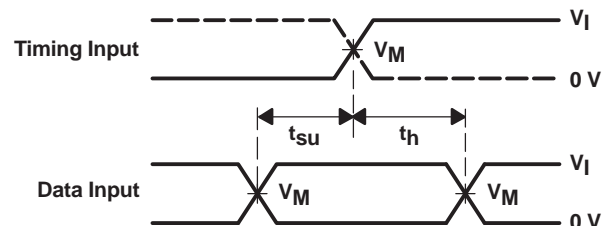
**LOAD CIRCUIT**

TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	V <sub>LOAD</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

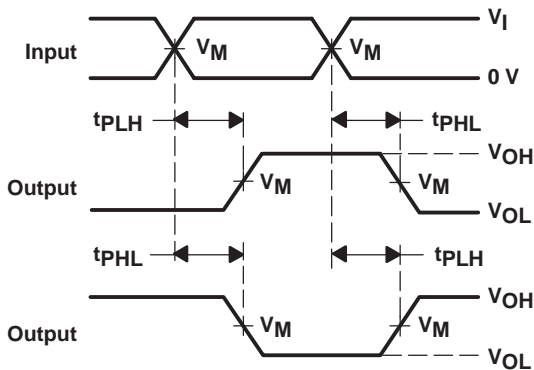
V <sub>CC</sub>	INPUTS		V <sub>M</sub>	V <sub>LOAD</sub>	C <sub>L</sub>	R <sub>L</sub>	V <sub>Δ</sub>
	V <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>					
1.8 V ± 0.15 V	V <sub>CC</sub>	≤ 2 ns	V <sub>CC</sub> /2	2 × V <sub>CC</sub>	15 pF	1 MΩ	0.15 V
2.5 V ± 0.2 V	V <sub>CC</sub>	≤ 2 ns	V <sub>CC</sub> /2	2 × V <sub>CC</sub>	15 pF	1 MΩ	0.15 V
3.3 V ± 0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	15 pF	1 MΩ	0.3 V
5 V ± 0.5 V	V <sub>CC</sub>	≤ 2.5 ns	V <sub>CC</sub> /2	2 × V <sub>CC</sub>	15 pF	1 MΩ	0.3 V



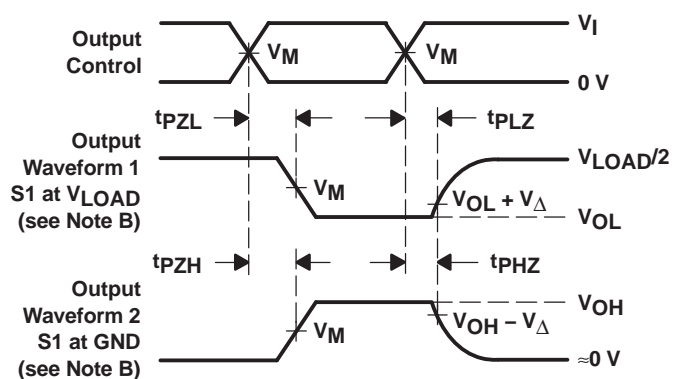
**VOLTAGE WAVEFORMS  
PULSE DURATION**



**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING**

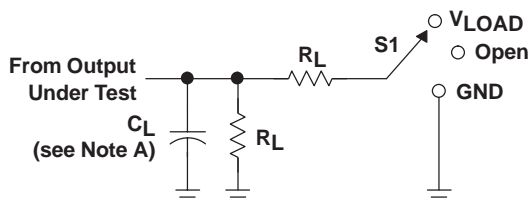
- NOTES:
- A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω.
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E. t<sub>PZL</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.
  - H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

# SN74LVC1G125 SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

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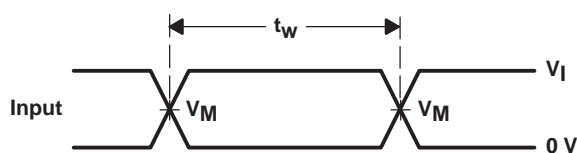
## PARAMETER MEASUREMENT INFORMATION



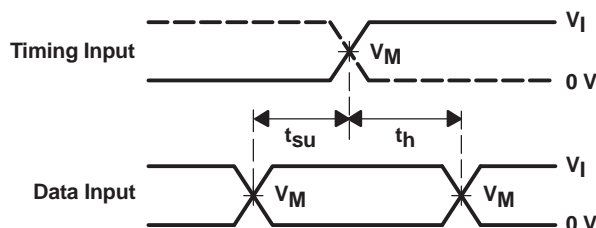
LOAD CIRCUIT

TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	V <sub>LOAD</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

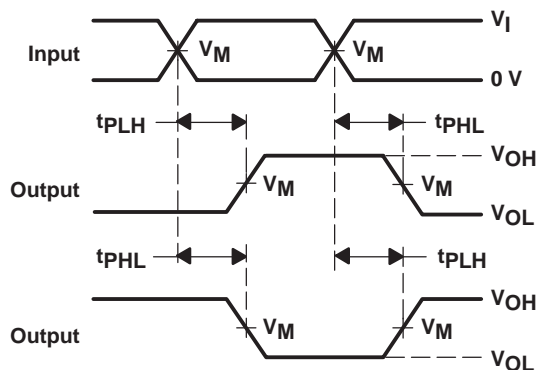
V <sub>CC</sub>	INPUTS		V <sub>M</sub>	V <sub>LOAD</sub>	C <sub>L</sub>	R <sub>L</sub>	V <sub>Δ</sub>
	V <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>					
1.8 V ± 0.15 V	V <sub>CC</sub>	≤ 2 ns	V <sub>CC</sub> /2	2 × V <sub>CC</sub>	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V <sub>CC</sub>	≤ 2 ns	V <sub>CC</sub> /2	2 × V <sub>CC</sub>	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V <sub>CC</sub>	≤ 2.5 ns	V <sub>CC</sub> /2	2 × V <sub>CC</sub>	50 pF	500 Ω	0.3 V



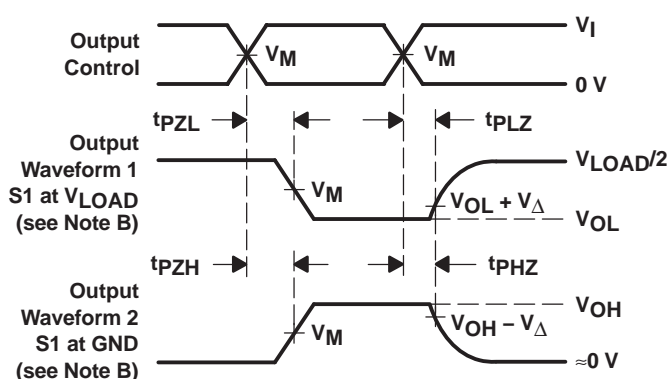
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C<sub>L</sub> includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω.
  - The outputs are measured one at a time, with one transition per measurement.
  - t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.
  - All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LVC1G125DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G125DBVT	ACTIVE	SOT-23	DBV	5	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G125DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G125DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G125DRLR	PREVIEW	SOP	DRL	5	4000	TBD	Call TI	Call TI
SN74LVC1G125YEAR	ACTIVE	WCSP	YEA	5	3000	TBD	SNPB	Level-1-260C-UNLIM
SN74LVC1G125YEPR	ACTIVE	WCSP	YEP	5	3000	TBD	SNPB	Level-1-260C-UNLIM
SN74LVC1G125YZAR	ACTIVE	WCSP	YZA	5	3000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM
SN74LVC1G125YZPR	ACTIVE	WCSP	YZP	5	3000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

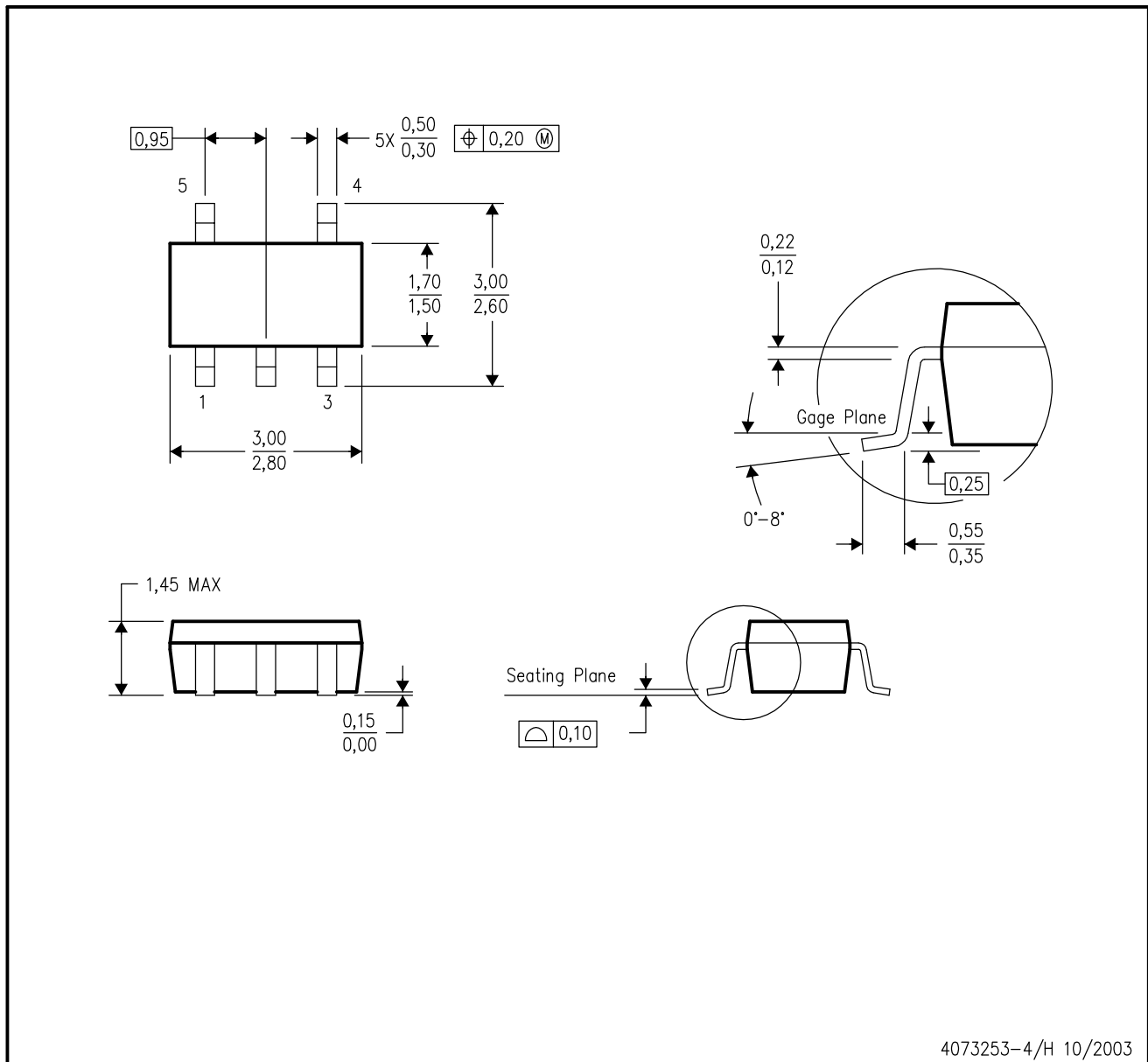
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

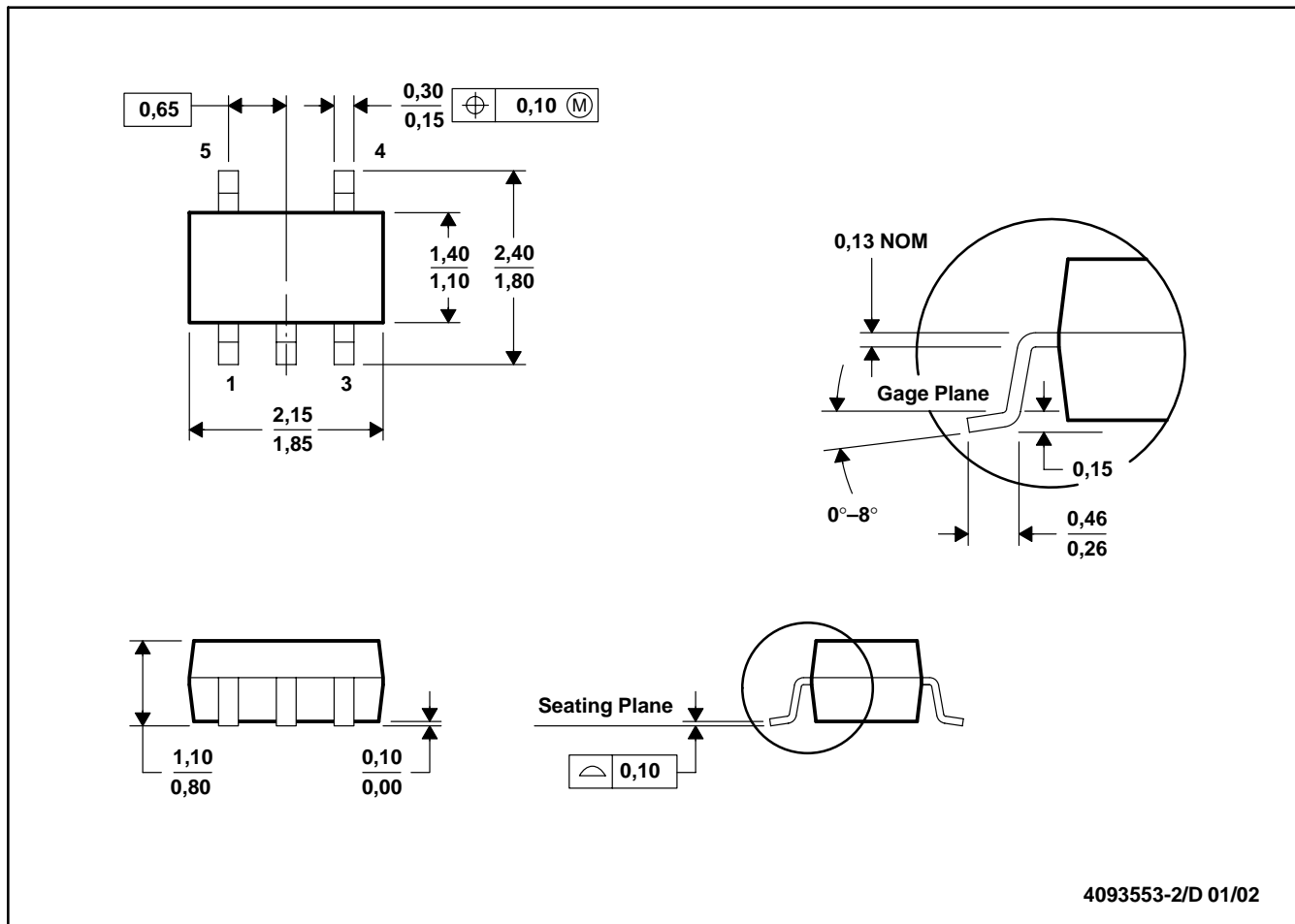


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion.
  - D. Falls within JEDEC MO-178 Variation AA.



DCK (R-PDSO-G5)

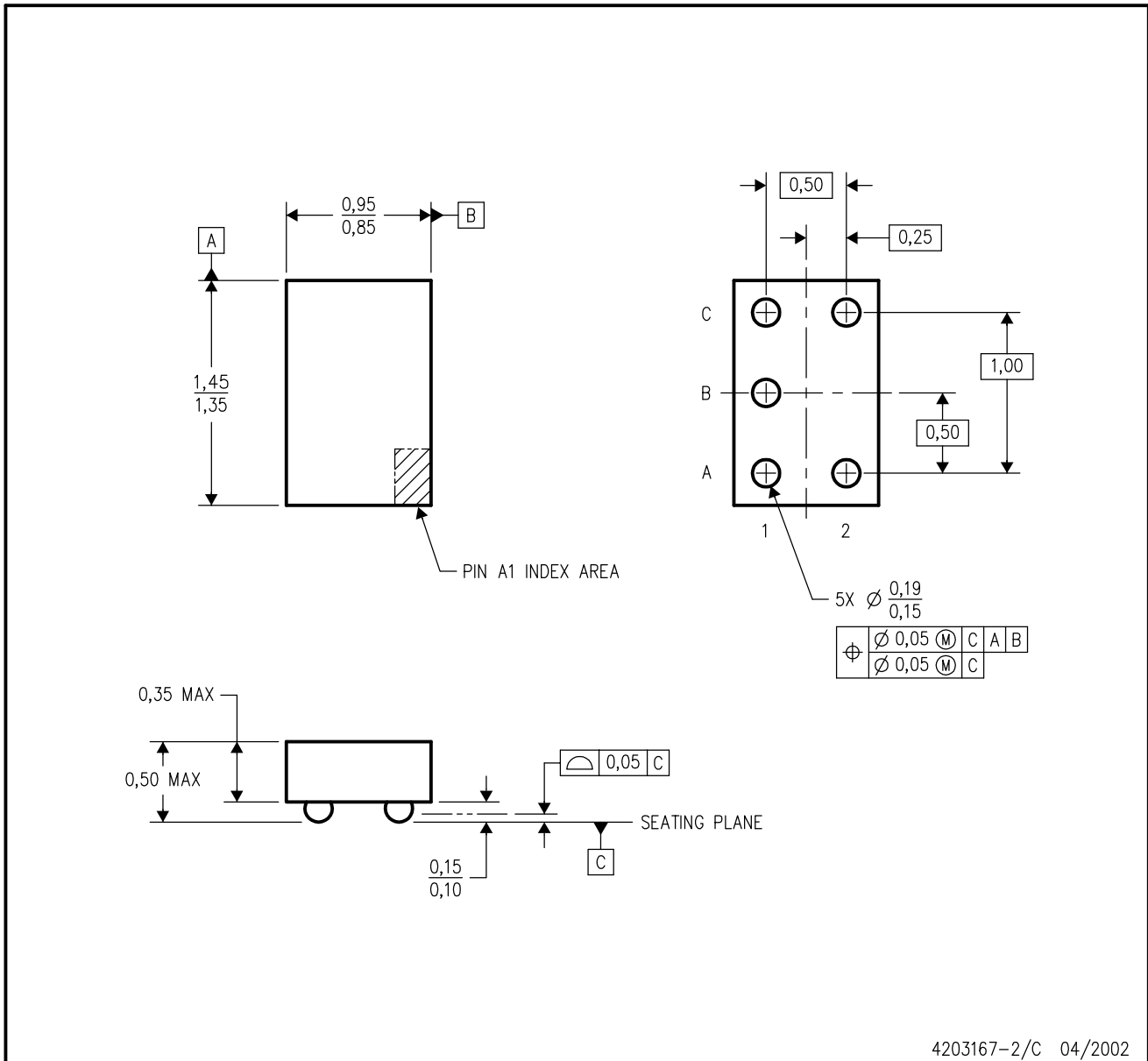
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion.  
 D. Falls within JEDEC MO-203

YEA (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY

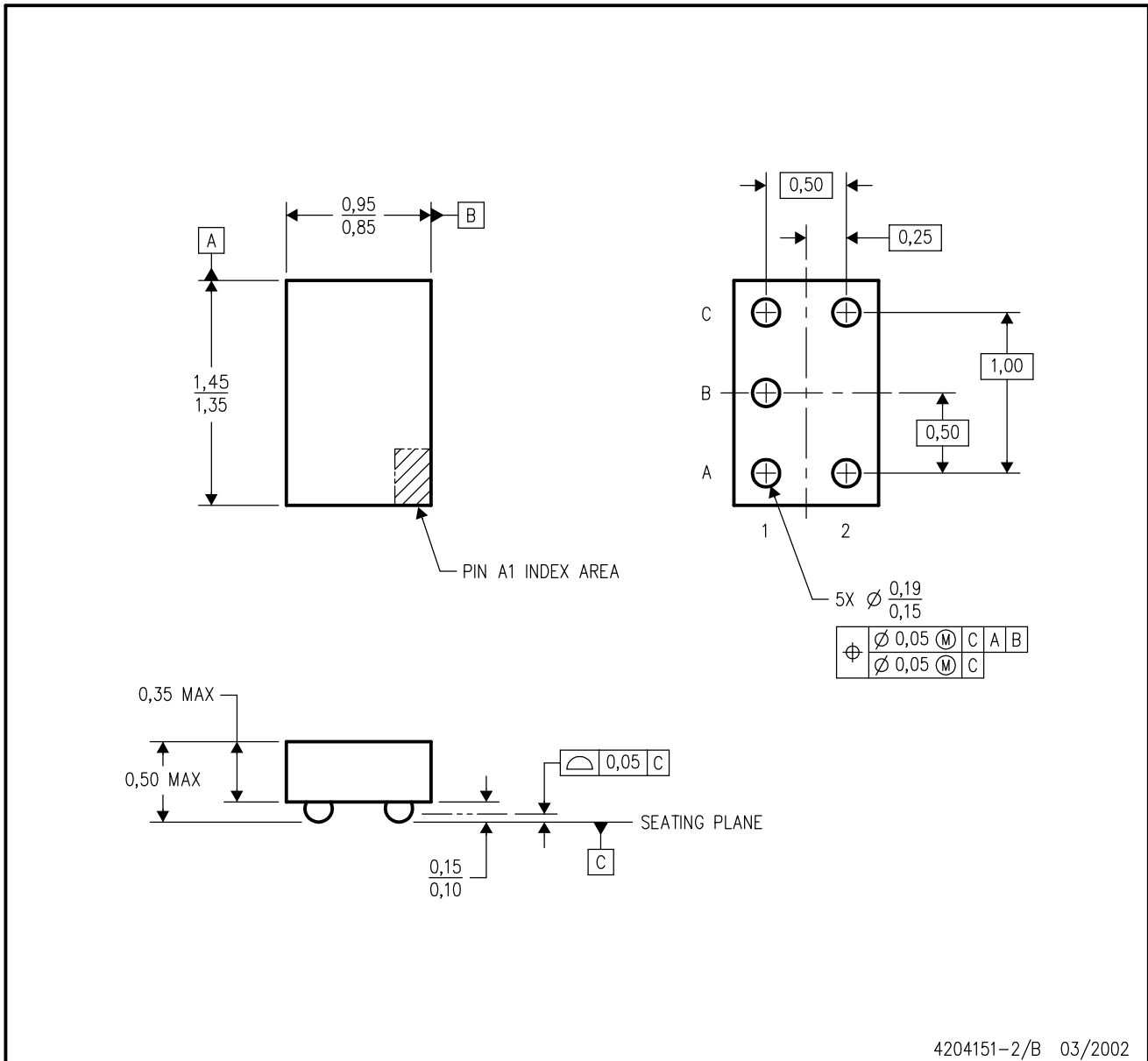


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. NanoStar™ package configuration.
  - D. Package complies to JEDEC MO-211 variation EA.
  - E. This package is tin-lead (SnPb). Refer to the 5 YZA package (drawing 4204151) for lead-free.

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YZA (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY

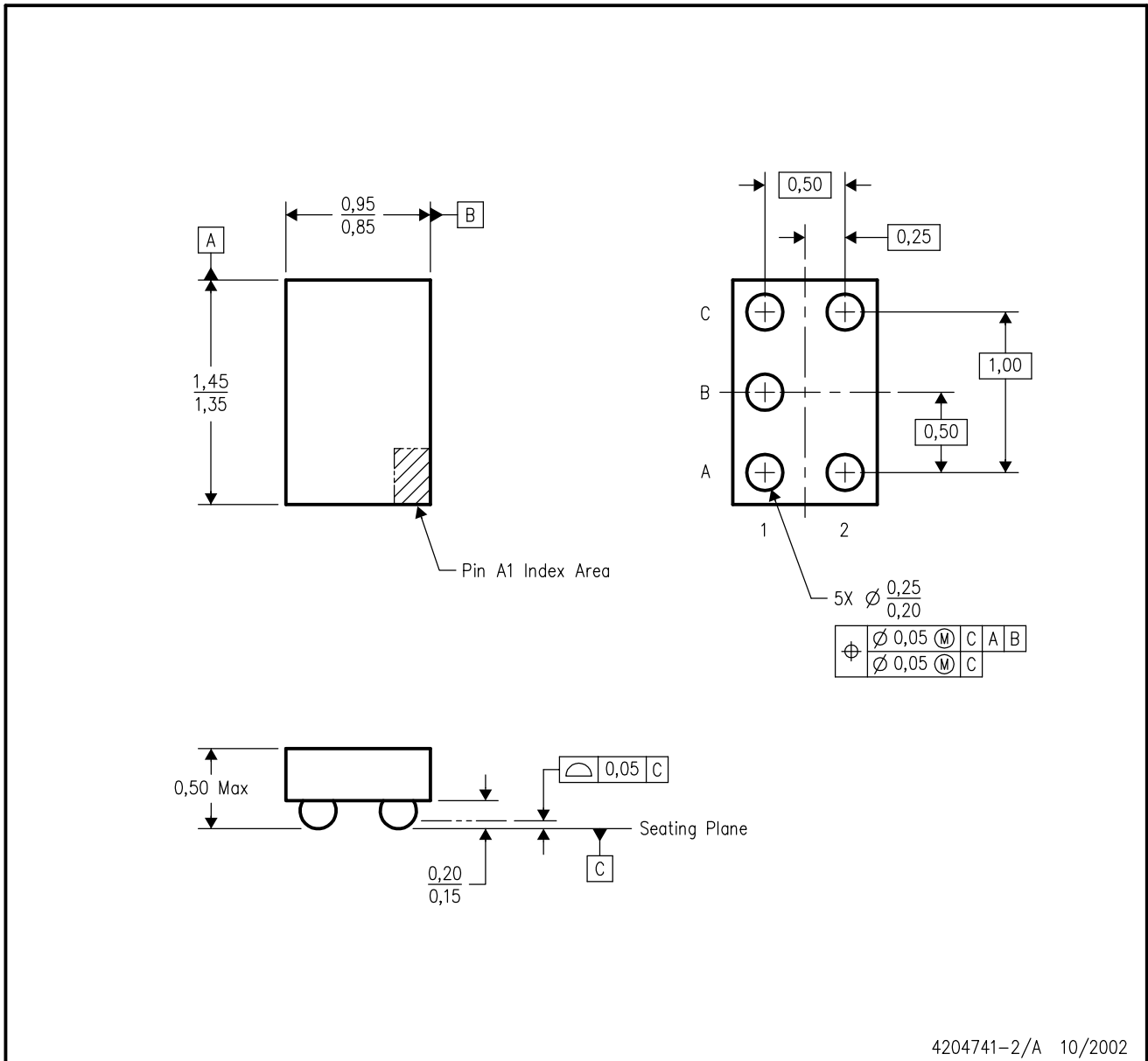


- NOTES:
- A. All linear dimensions are in millimeters.
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  - C. NanoFree™ package configuration.
  - D. Package complies to JEDEC MO-211 variation EA.
  - E. This package is lead-free. Refer to the 5 YEA package (drawing 4203167) for tin-lead (SnPb).

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YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY

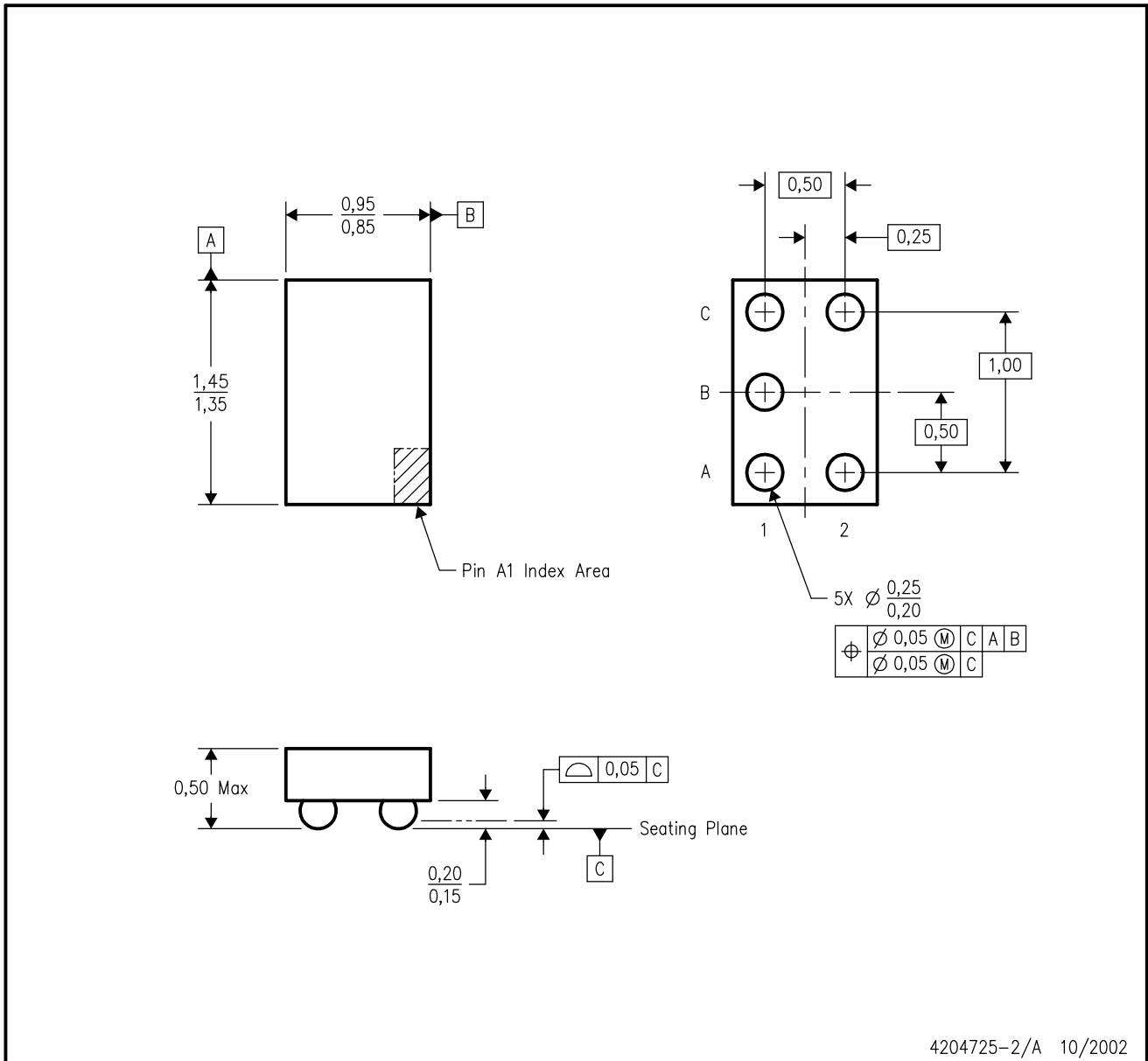


- NOTES:
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  - D. This package is lead-free. Refer to the 5 YEP package (drawing 4204725) for tin-lead (SnPb).

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YEP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



4204725-2/A 10/2002

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