DN74LS197 N74LS197

30MHz Settable Binary Counters / Latches

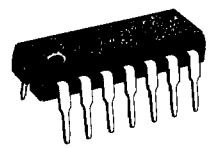
■ Description

DN74LS197 is an asynchronous hexadecimal (4-bit binary) counter with direct-coupled reset input and set input.

■ Features

- Direct-coupled reset input and asynchronous set input
- Capability for independent use as binary and octal counters
- High-speed counting (f_{max} = 40 MHz typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-1

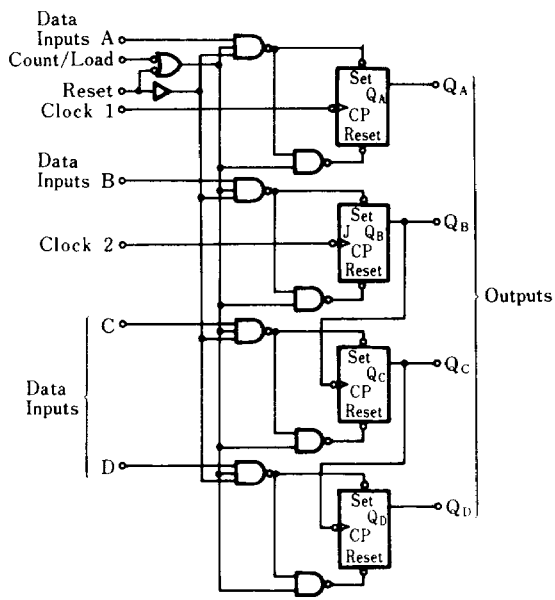


14-pin plastic DIL package

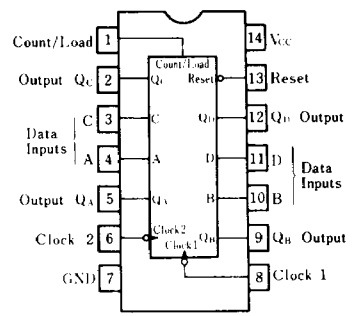
P-4

14-pin Panaflat package (SO-14D)

■ Logic diagram



Pin configuration (top view)



■ Absolute maximum ratings

Parameter	Sym.	Rating		Unit
Input voltage	V_I	−0.5	5.5	V

* Refer to the family ratings for other parameters.

■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Count frequency	Clock 1 Input	t_{count}	0		30	MHz
	Clock 2 Input		0		15	
Pulse width	Clock 1 Input	t_w	20			ns
	Clock 2 put		30			
	Reset		15			
	Loacb		20			
Set-up time	High Level Data	t_{su}	10			ns
	Low Level Data		15			
Hold time	High Level Data	t_h	20			ns
	Low Level Data		20			
Enable time		t_{enable}	30			ns

■ DC characteristics (Ta = −20 ~ +75℃)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage**		V_{OH}	V_{CC} = 4.75V, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −400μA		2.7	3.4		V
		V_{OL1}	V_{CC} = 4.75V V_{IH} = 2V V_{IL} = 0.8V	I_{OL} = 4mA		0.25	0.4	V
		V_{OL2}		I_{OL} = 8mA		0.35	0.5	V
Input current	Data, Count / Load	I_{IH}	V_{CC} = 5.25V V_I = 2.7V				20	μA
	Reset, Clock-1						40	μA
	Clock-2						80	μA
	Data, Count / Load	I_{IL}	V_{CC} = 5.25V V_I = 0.4V				−0.4	mA
	Reset						−0.8	mA
	Clock-1						−2.4	mA
	Clock-2						−1.3	mA
	Data, Count / Load	I_I	V_{CC} = 5.25V V_I = 5.5V				0.1	mA
	Reset, Clock-1						0.2	mA
	Clock-2						0.4	mA
Output short circuit current***		I_{OS}	V_{CC} = 5.25V V_{in} = 0V		−15		−100	mA
Input clamp voltage		V_{IK}	V_{CC} = 4.75V I_I = −18mA				−1.5	V
Supply current***		I_{CC}	V_{CC} = 5.25V			16	27	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** When testing Q_A output, a current to which the rated upper limit value for the I_{IL} of the clock-2 input has been added is applied to the specified I_{OL}.

*** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

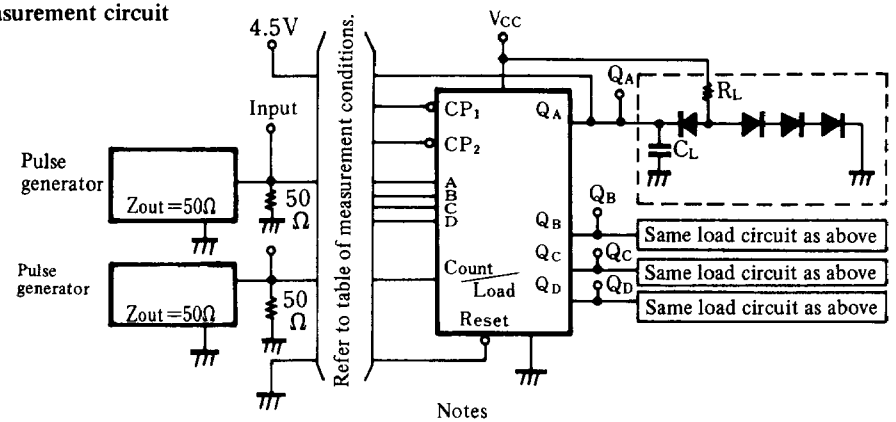
**** Measured with all outputs open and all inputs grounded.

■ Switching characteristics (V_{CC}=5V, Ta=25℃)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}	Clock 1	Q_A	C_L=15pF, R_L=2kΩ	30	40		MHz
Propagation delay time	t_{PLH}	Clock 1	Q_A			8	15	ns
	t_{PHL}					14	21	
	t_{PLH}	Clock 2	Q_B			12	19	ns
	t_{PHL}					23	35	
	t_{PLH}	Clock 2	Q_C			34	51	ns
	t_{PHL}					42	63	
	t_{PLH}	Clock 2	Q_D			55	78	ns
	t_{PHL}					63	95	
	t_{PLH}	A, B, C, D	Q_A, Q_B Q_C, Q_D			18	27	ns
	t_{PHL}					29	44	
	t_{PLH}	Load	Q_A~Q_D			26	39	ns
	t_{PHL}					30	45	
	t_{PHL}	Reset	Q_A~Q_D			34	51	ns

※ Switching parameter measurement information

1. Measurement circuit



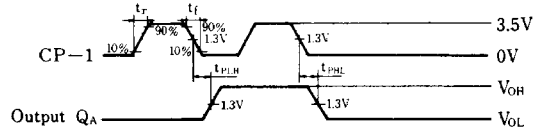
Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Table of measurement conditions

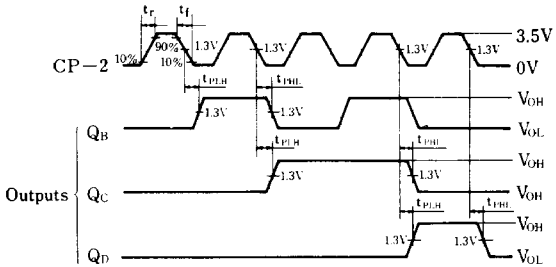
Parameter	Inputs/Outputs	Inputs								Outputs			
		Reset	Count/Load	CP-1	CP-2	Data A	Data B	Data C	Data D	Q_A	Q_B	Q_C	Q_D
f_{max}		4.5V	4.5V	IN	Linked to Q_A	GND	GND	GND	GND	OUT	OUT	OUT	OUT
t_{PLH} t_{PHL}	CP-1→Q_A	4.5V	4.5V	IN	Linked to Q_A	GND	GND	GND	GND	OUT			
	CP-2→Q_B, Q_C Q_D	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND		OUT	OUT	OUT
	A, B, C, D→Q_A, Q_B Q_C, Q_D	4.5V	GND	4.5V	Linked to Q_A	IN	IN	IN	IN	OUT	OUT	OUT	OUT
	Load→Q_A, Q_B Q_C, Q_D	4.5V	IN	4.5V	Linked to Q_A	4.5V or GND	4.5V or GND	4.5V or GND	4.5V or GND	OUT	OUT	OUT	OUT
	Reset→Q_A, Q_B Q_C, Q_D	IN	IN	4.5V	Linked to Q_A	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT

3.Waveforms

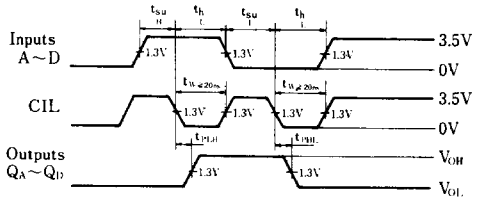
Waveforms-1 f_{max}(CP−1), t_W(CP−1), t_{PLH}, t_{PHL}(CP → Q_A)



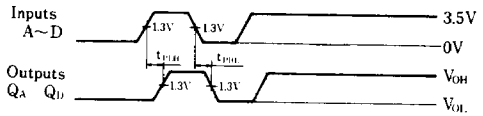
Waveforms-2 f_{max} (CP−2), t_W(CP−2), t_{PLH}, t_{PHL} (CP−2 → Q_B, Q_C, Q_D)



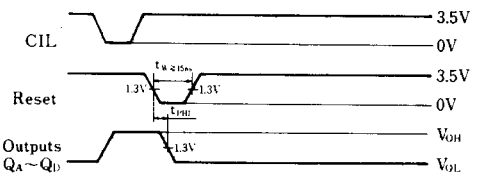
Waveforms-3 t_W(Reset), t_{PHL}(Reset → Q)



Waveforms-4 t_W(Load), t_{su}, t_h(H, L), t_{PHL}, t_{PLH}(Load → Q)



Waveforms-5 t_{PLH}, t_{PHL}(Data → Q)



Notes

1. CP-1 and CP-2 waveforms:
   $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.
2. When measuring f_{max}, t_r and $t_f \leqq 2.5$ns.

■ Truth tables

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Notes 1. Output Q_A is connected to clock CP-2. 2. H: HIGH voltage level. 3. L: LOW voltage level.