

Description

The GM71V(S)18163C/CL is the new generation dynamic RAM organized 1,048,576 x 16 bit. GM71V(S)18163C/CL has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71V(S)18163C/CL offers Extended Data out(EDO) Mode as a high speed access mode. Multiplexed address inputs permit the GM71V(S)18163C/CL to be packaged in standard 400 mil 42pin plastic SOJ, and standard 400mil 44(50)pin plastic TSOP II. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

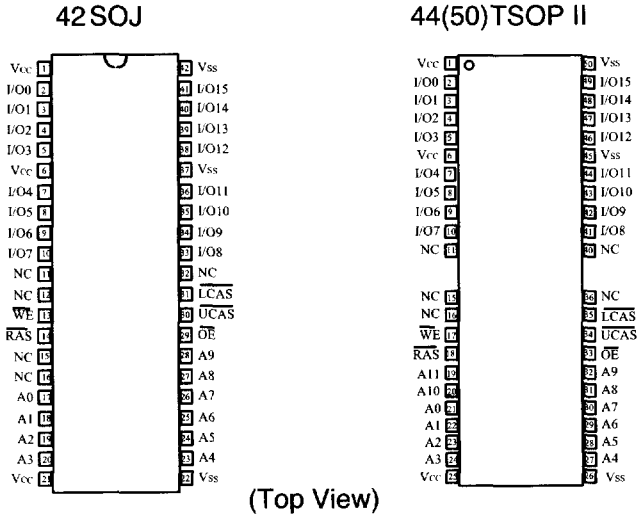
Features

- * 1,048,576 Words x 16 Bit Organization
- * Extended Data Out Mode Capability
- * Single Power Supply (3.3V±0.3V)
- * Fast Access Time & Cycle Time (Unit: ns)

	t _{TRAC}	t _{CAC}	t _{RC}	t _{HPC}
GM71V(S)18163C/CL-5	50	13	84	20
GM71V(S)18163C/CL-6	60	15	104	25
GM71V(S)18163C/CL-7	70	18	124	30

- * Low Power
 Active : 684/612/540mW (MAX)
 Standby : 7.2mW (CMOS level : MAX)
 0.83mW (L-version : MAX)
- * RAS Only Refresh, CAS before RAS Refresh, Hidden Refresh Capability
- * All inputs and outputs TTL Compatible
- * 1024 Refresh Cycles/16ms
- * 1024 Refresh Cycles/128ms (L-version)
- * Self Refresh Operation (L-version)
- * Battery Back Up Operation (L-version)
- * 2 CAS byte Control

Pin Configuration



16M-bit
DRAM

Pin Description

Pin	Function	Pin	Function
A0-A9	Address Inputs	\overline{WE}	Read/Write Enable
A0-A9	Refresh Address Inputs	\overline{OE}	Output Enable
I/O0-I/O15	Data-In/Out	V _{CC}	Power (+3.3V)
\overline{RAS}	Row Address Strobe	V _{SS}	Ground
$\overline{UCAS, LCAS}$	Column Address Strobe	NC	No Connection

Ordering Information

Type No.	Access Time	Package
GM71V(S)18163CJ/CLJ -5 GM71V(S)18163CJ/CLJ -6 GM71V(S)18163CJ/CLJ -7	50ns 60ns 70ns	400 Mil 42 Pin Plastic SOJ
GM71V(S)18163CT/CLT -5 GM71V(S)18163CT/CLT -6 GM71V(S)18163CT/CLT -7	50ns 60ns 70ns	400 Mil 44(50) Pin Plastic TSOP II

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T _A	Ambient Temperature under Bias	0 ~ 70	C
T _{STG}	Storage Temperature	-55 ~ 125	C
V _{IN/OUT}	Voltage on any Pin Relative to V _{SS}	-0.5 ~ V _{CC} +0.5 (<=4.6V(MAX))	V
V _{CC}	Supply Voltage Relative to V _{SS}	-0.5 ~ 4.6	V
I _{OUT}	Short Circuit Output Current	50	mA
P _D	Power Dissipation	1.0	W

Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended DC Operating Conditions ($T_A = 0 \sim 70^\circ\text{C}$)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	-	$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V

Note: All voltage referred to V_{SS} .

The supply voltage with all VCC pins must be on the same level. The supply voltage with all VSS pins must be on the same level.

Truth Table

RAS	LCAS	UCAS	WE	OE	Output	Operation	Notes
H	D	D	D	D	Open	Standby	1,3
L	L	H	H	L	Valid	Lower byte	Read cycle 1,3
L	H	L	H	L	Valid	Upper byte	
L	L	L	H	L	Valid	Word	
L	L	H	L	D	Open	Lower byte	Early write cycle 1,2,3
L	H	L	L	D	Open	Upper byte	
L	L	L	L	D	Open	Word	
L	L	H	L	H	Undefined	Lower byte	Delayed Write cycle 1,2,3
L	H	L	L	H	Undefined	Upper byte	
L	L	L	L	H	Undefined	Word	
L	L	H	H to L	L to H	Valid	Lower byte	Read-modify -write cycle 1,3
L	H	L	H to L	L to H	Valid	Upper byte	
L	L	L	H to L	L to H	Valid	Word	
H to L	H	L	D	D	Open	Word	CBR Refresh or Self Refresh (L-series) 1,3
H to L	L	H	D	D	Open	Word	
H to L	L	L	D	D	Open	Word	
L	H	H	D	D	Open	Word	RAS-only Refresh cycle 1,3
L	L	L	H	H	Open	Read cycle (Output disabled)	1,3

Notes: 1. H: High (inactive) L: Low(active) D: H or L

2. $t_{wCS} \geq 0ns$ Early write cycle

$t_{wCS} \leq 0ns$ Delayed write cycle

3. Mode is determined by the OR function of the UCAS and LCAS. (Mode is set by earliest of UCAS and LCAS active edge and reset by the latest of UCAS and LCAS inactive edge.) However write OPERATION and output High-Z control are done independently by each UCAS,LCAS.
ex) if RAS = H to L, UCAS = H, LCAS = L, then CAS-before-RAS refresh cycle is selected.

DC Electrical Characteristics ($V_{CC} = 3.3V \pm 0.3V$, $V_{SS} = 0V$, $T_A = 0 \sim 70C$)

	Parameter	Min	Max	Unit	Note	
V	Output Level Output "H" Level Voltage ($I_{OUT} = -2mA$)	2.4	V_{CC}	V		
V	Output Level Output "L" Level Voltage ($I_{OUT} = 2mA$)	0	0.4	V		
I _{CC1}	Operating Current Average Power Supply Operating Current (\overline{RAS} , \overline{UCAS} or \overline{LCAS} Cycling: $t_{RC} = t_{RC \min}$)	50ns	-	190	mA	1, 2
		60ns	-	170		
		70ns	-	150		
I _{CC2}	Standby Current (TTL) Power Supply Standby Current (\overline{RAS} , \overline{UCAS} , $\overline{LCAS} = V_{IH}$, $D_{OUT} = \text{High-Z}$)	-	2	mA		
I _{CC3}	RAS Only Refresh Current Average Power Supply Current RAS Only Refresh Mode ($t_{RC} = t_{RC \min}$)	50ns	-	190	mA	2
		60ns	-	170		
		70ns	-	150		
I _{CC4}	EDO Page Mode Current Average Power Supply Current EDO Page Mode ($t_{HPC} = t_{HPC \min}$)	50ns	-	185	mA	1, 3
		60ns	-	165		
		70ns	-	145		
I _{CC5}	Standby Current (CMOS) Power Supply Standby Current (\overline{RAS} , \overline{UCAS} or $\overline{LCAS} \geq V_{CC} - 0.2V$, $D_{OUT} = \text{High-Z}$)	-	1	mA		
		-	150	uA	5	
I _{CC6}	CAS-before-RAS Refresh Current ($t_{RC} = t_{RC \min}$)	50ns	-	190	mA	
		60ns	-	170		
		70ns	-	150		
I _{CC7}	Battery Back Up Operating Current(Standby with CBR Ref.) (CBR refresh, $t_{RC} = 125\mu s$, $t_{RAS} \leq 0.3\mu s$, $D_{OUT} = \text{High-Z}$, CMOS interface)	-	400	uA	4,5	
I _{CC8}	Standby Current $\overline{RAS} = V_{IH}$ \overline{UCAS} , $\overline{LCAS} = V_{IL}$ $D_{OUT} = \text{Enable}$	-	5	mA	1	
I _{CC9}	Self-Refresh Mode Current (\overline{RAS} , \overline{UCAS} or $\overline{LCAS} \leq 0.2V$, $D_{OUT} = \text{High-Z}$)	-	250	uA	5	
I _{LI0}	Input Leakage Current Any Input ($0V \leq V_{IN} \leq 4.6V$)	-10	10	uA		
I _{LI0}	Output Leakage Current (D_{OUT} is Disabled, $0V \leq V_{OUT} \leq 4.6V$)	-10	10	uA		

Note: 1. I_{CC} depends on output load condition when the device is selected.

I_{CC(max)} is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.
3. Address can be changed once or less while \overline{LCAS} and $\overline{UCAS} = V_{IH}$.
4. $\overline{UCAS} = L$ (≤ 0.2) and $\overline{LCAS} = L$ (≤ 0.2) while $\overline{RAS} = L$ (≤ 0.2).
5. L-version.

Capacitance ($V_{CC} = 3.3V \pm 0.3V$, $T = 25C$)

	Parameter	Min	Max	Unit	
C	Input Capacitance (Address)	-	5	pF	1
C	Input Capacitance (Clocks)	-	7	pF	1
C	Output Capacitance (Data-In/Out)	-	7	pF	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. UCAS and LCAS = V_{IH} to disable D_{OUT} .AC Characteristics ($V_{CC} = 3.3V \pm 0.3V$, $T_A = 0 \sim +70C$, Note 1, 2, 18, 19, 20)

Test Conditions

Input rise and fall times : 2 ns

Input levels : $V_{IL} = 0V$, $V_{IH} = 3V$

Input timing reference levels : 0.8V, 2.0V

Output timing reference levels : 0.8V, 2.0V

Output load : 1TTL gate + C_L (100 pF)

(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GM71V(S)18163 C/CL-5		GM71V(S)18163 C/CL-6		GM71V(S)18163 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	84	-	104	-	124	-	ns	
t_{RP}	RAS Precharge Time	30	-	40	-	50	-	ns	
t_{CP}	CAS Precharge Time	8	-	10	-	13	-	ns	
t_{RAS}	RAS Pulse Width	50	10,000	60	10,000	70	10,000	ns	
t_{CAS}	CAS Pulse Width	8	10,000	10	10,000	13	10,000	ns	
t_{ASR}	Row Address Set up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	8	-	10	-	10	-	ns	
t_{ASC}	Column Address Set-up Time	0	-	0	-	0	-	ns	21
t_{CAH}	Column Address Hold Time	8	-	10	-	13	-	ns	21
t_{RCD}	RAS to CAS Delay Time	12	37	14	45	14	52	ns	3
t_{RAD}	RAS to Column Address Delay Time	10	25	12	30	12	35	ns	4
t_{RSH}	RAS Hold Time	10	-	13	-	13	-	ns	
t_{CSH}	CAS Hold Time	35	-	40	-	45	-	ns	23
t_{CRP}	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	22
t_{ODD}	OE to D_{IN} Delay Time	13	-	15	-	18	-	ns	5
t_{DZO}	OE Delay Time from D_{IN}	0	-	0	-	0	-	ns	6
t_{DZC}	CAS Delay Time from D_{IN}	0	-	0	-	0	-	ns	6
t_r	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	7

Read Cycle

Symbol	Parameter	GM71V(S)18163 C/CL-5		GM71V(S)18163 C/CL-6		GM71V(S)18163 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{RAC}	Access Time from $\overline{\text{RAS}}$	-	50	-	60	-	70	ns	8,9
t _{CAC}	Access Time from $\overline{\text{CAS}}$	-	13	-	15	-	18	ns	9,10,17
t _{AA}	Access Time from Address	-	25	-	30	-	35	ns	9,11,17
t _{OAC}	Access Time from $\overline{\text{OE}}$	-	13	-	15	-	18	ns	9
t _{RCS}	Read Command Setup Time	0	-	0	-	0	-	ns	21
t _{RCH}	Read Command Hold Time to $\overline{\text{CAS}}$	0	-	0	-	0	-	ns	12,22
t _{RRH}	Read Command Hold Time to $\overline{\text{RAS}}$	5	-	5	-	5	-	ns	12
t _{RAL}	Column Address to $\overline{\text{RAS}}$ Lead Time	25	-	30	-	35	-	ns	
t _{CAL}	Column Address to $\overline{\text{CAS}}$ Lead Time	15	-	18	-	23	-	ns	
t _{CLZ}	$\overline{\text{CAS}}$ to Output in Low-Z	0	-	0	-	0	-	ns	
t _{OH}	Output Data Hold Time	3	-	3	-	3	-	ns	27
t _{OHO}	Output Data Hold Time from $\overline{\text{OE}}$	3	-	3	-	3	-	ns	
t _{OFF}	Output Buffer Turn-off Time	-	13	-	15	-	15	ns	13,27
t _{OEZ}	Output Buffer Turn-off Time to $\overline{\text{OE}}$	-	13	-	15	-	15	ns	13
t _{CDD}	$\overline{\text{CAS}}$ to D_{IN} Delay Time	13	-	15	-	18	-	ns	5
t _{RCHR}	Read Command Hold Time from $\overline{\text{RAS}}$	50	-	60	-	70	-	ns	
t _{OHR}	Output Data hold Time from $\overline{\text{RAS}}$	3	-	3	-	3	-	ns	27
t _{OFR}	Output Buffer turn off to $\overline{\text{RAS}}$	-	13	-	15	-	15	ns	27
t _{WEZ}	Output Buffer turn off to $\overline{\text{WE}}$	-	13	-	15	-	15	ns	
t _{WDD}	$\overline{\text{WE}}$ to D_{IN} Delay Time	13	-	15	-	18	-	ns	
t _{RDD}	$\overline{\text{RAS}}$ to D_{IN} Delay Time	13	-	15	-	18	-	ns	

Write Cycle

Symbol	Parameter	GM71V(S)18163 C/CL-5		GM71V(S)18163 C/CL-6		GM71V(S)18163 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{WCS}	Write Command Setup Time	0	-	0	-	0	-	ns	14,21
t _{WCH}	Write Command Hold Time	8	-	10	-	13	-	ns	21
t _{WP}	Write Command Pulse Width	8	-	10	-	10	-	ns	
t _{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time	8	-	10	-	13	-	ns	
t _{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	8	-	10	-	13	-	ns	23
t _{DS}	Data-in Setup Time	0	-	0	-	0	-	ns	15,23
t _{DH}	Data-in Hold Time	8	-	10	-	13	-	ns	15,23

Read-Modify-Write Cycle

Symbol	Parameter	GM71V(S)18163 C/CL-5		GM71V(S)18163 C/CL-6		GM71V(S)18163 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{RWC}	Read-Modify-Write Cycle Time	111	-	136	-	161	-	ns	
t _{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	67	-	79	-	92	-	ns	14
t _{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	30	-	34	-	40	-	ns	14
t _{AWD}	Column Address to $\overline{\text{WE}}$ Delay Time	42	-	49	-	57	-	ns	14
t _{OEH}	$\overline{\text{OE}}$ Hold Time from $\overline{\text{WE}}$	13	-	15	-	18	-	ns	

Refresh Cycle

Symbol	Parameter	GM71V(S)18163 C/CL-5		GM71V(S)18163 C/CL-6		GM71V(S)18163 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{CSR}	$\overline{\text{CAS}}$ Setup Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	5	-	5	-	5	-	ns	21
t _{CHR}	$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	8	-	10	-	10	-	ns	22
t _{RPC}	$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time	5	-	5	-	5	-	ns	21

EDO Page Mode Cycle

Symbol	Parameter	GM71V(S)18163 C/CL-5		GM71V(S)18163 C/CL-6		GM71V(S)18163 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{HPC}	EDO Page Mode Cycle Time	20	-	25	-	30	-	ns	25
t _{RASP}	EDO Page Mode $\overline{\text{RAS}}$ Pulse Width	-	100,000	-	100,000	-	100,000	ns	16
t _{ACP}	Access Time from $\overline{\text{CAS}}$ Precharge	-	30	-	35	-	40	ns	9,17,22
t _{RHCP}	$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	30	-	35	-	40	-	ns	
t _{DOH}	Output data Hold Time from $\overline{\text{CAS}}$ low	3	-	3	-	3		ns	9
t _{COL}	$\overline{\text{CAS}}$ Hold Time referred $\overline{\text{OE}}$	8	-	10	-	13		ns	
t _{COP}	$\overline{\text{CAS}}$ to $\overline{\text{OE}}$ Setup Time	5	-	5	-	5		ns	
t _{RCHP}	Read command Hold Time from $\overline{\text{CAS}}$ Precharge	30	-	35	-	40		ns	

EDO Page Mode Read-Modify-Write Cycle

Symbol	Parameter	GM71V(S)18163 C/CL-5		GM71V(S)18163 C/CL-6		GM71V(S)18163 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{HPRWC}	EDO Page Mode Read-Modify-Write Cycle Time	57	-	68	-	79	-	ns	
t _{CPW}	$\overline{\text{WE}}$ Delay Time from $\overline{\text{CAS}}$ Precharge	45	-	54	-	62	-	ns	14,22

Refresh

Symbol	Parameter	GM71V(S)18163 C/CL-5		GM71V(S)18163 C/CL-6		GM71V(S)18163 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{REF}	Refresh period	-	16	-	16	-	16	ms	1024 cycles
t _{REF}	Refresh period (L -Series)	-	128	-	128	-	128	ms	1024 cycles

Self Refresh Mode (L-version)

Symbol	Parameter	GM71VS18163 CL-5		GM71VS18163 CL-6		GM71VS18163 CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RASS}	\overline{RAS} Pulse Width(Self-Refresh)	100	-	100	-	100	-	us	29
t_{RPS}	\overline{RAS} Precharge Time(Self-Refresh)	90	-	110	-	130	-	ns	
t_{CHS}	\overline{CAS} Hold Time(Self-Refresh)	-50	-	-50	-	-50	-	ns	

Notes :

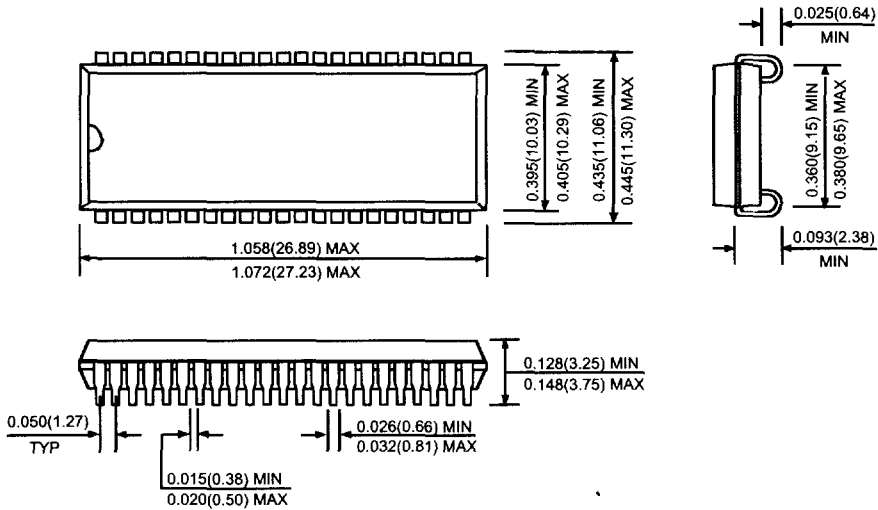
- AC measurements assume $t_T = 2$ ns.
- An initial pause of 200us is required after power followed by a minimum of eight initialization cycles (any combination of cycles containing \overline{RAS} -only refresh or \overline{CAS} -before- \overline{RAS} refresh).
- Operation with the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met, $t_{RCD}(\max)$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
- Operation with the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met, $t_{RAD}(\max)$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled exclusively by t_{AA} .
- Either t_{ODD} or t_{CDD} must be satisfied.
- Either t_{DZO} or t_{DZC} must be satisfied.
- $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$.
- Assumes that $t_{RCD} \leq t_{RCD}(\max)$ and $t_{RAD} \leq t_{RAD}(\max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
- Measured with a load circuit equivalent to 1TTL loads and 100pF.
- Assumes that $t_{RCD} \geq t_{RCD}(\max)$ and $t_{RAD} \leq t_{RAD}(\max)$.
- Assumes that $t_{RCD} \leq t_{RCD}(\max)$ and $t_{RAD} \geq t_{RAD}(\max)$.
- Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
- $t_{OFF}(\max)$ and $t_{OEZ}(\max)$ define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
- t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}(\min)$, the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(\min)$, $t_{CWD} \geq t_{CWD}(\min)$, and $t_{AWD} \geq t_{AWD}(\min)$, or $t_{CWD} \geq t_{CWD}(\min)$ $t_{AWD} \geq t_{AWD}(\min)$ and $t_{CPW} \geq t_{CPW}(\min)$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

15. These parameters are referred to \overline{UCAS} and \overline{LCAS} leading edge in early write cycles and to \overline{WE} leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines \overline{RAS} pulse width in EDO mode cycles.
17. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP} .
18. In delayed write or read-modify-write cycles, \overline{OE} must disable output buffer prior to applying data to the device. After \overline{RAS} is reset, if $t_{OE} > t_{CWL}$, the I/O pin will remain open circuit (high impedance): if $t_{OE} \leq t_{CWL}$, invalid data will be out at each I/O.
19. When both \overline{LCAS} and \overline{UCAS} go low at the same time, all 16-bits data are written into the device. \overline{LCAS} and \overline{UCAS} cannot be staggered within the same write/read cycles.
20. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
21. t_{ASC} , t_{CAH} , t_{RCS} , t_{WCS} , t_{WCH} , t_{CSR} and t_{RPC} are determined by the earlier falling edge of \overline{UCAS} or \overline{LCAS} .
22. t_{CRP} , t_{CHR} , t_{RCH} , t_{ACP} and t_{CPW} are determined by the later rising edge of \overline{UCAS} or \overline{LCAS} .
23. t_{CWL} , t_{DH} , t_{DS} and t_{CHS} should be satisfied by both \overline{UCAS} and \overline{LCAS} .
24. t_{CP} is determined by the time that both \overline{UCAS} and \overline{LCAS} are high.
25. $t_{HPC}(\text{min})$ can be achieved during a series of EDO page made write cycles or EDO mode write cycles. It both write and read operation are mixed in a EDO mode \overline{RAS} cycle(EDO mode mix cycle (1),(2)) minimum Value of \overline{CAS} cycle ($t_{CAS} + t_{CP} + 2t$) becomes greater than the specified t_{HPC} (min) value. The value of \overline{CAS} cycle time of mixed EDO mode is shown in EDO mode mix cycle (1) and (2).
26. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC}/V_{SS} line noise, which causes to degrade $V_{IH\text{min}}/V_{IL\text{max}}$ level.
27. Data output turns off and becomes high impedance from later rising edge of \overline{RAS} and \overline{CAS} . Hold time and turn off time are specified by the timing specification of later rising edge of \overline{RAS} and \overline{CAS} between t_{OHR} and t_{OH} , and between t_{OFR} and t_{OFF} .
28. EDO Hi-Z control by \overline{OE} or \overline{WE} . \overline{OE} rising edge disables data outputs. When \overline{OE} goes high during \overline{CAS} high, the data will not come out until next \overline{CAS} access. When \overline{WE} goes low during \overline{CAS} high, the data will not come out until next \overline{CAS} access.
29. Please do not use t_{RASS} timing, $10\mu\text{s} \leq t_{RASS} \leq 100\mu\text{s}$. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{RASS} \geq 100\mu\text{s}$, then \overline{RAS}
30. H or L (H : $V_{IH(\text{min})} \leq V_{IN} \leq V_{IH(\text{max})}$, L : $V_{IL(\text{min})} \leq V_{IN} \leq V_{IL(\text{max})}$)

Package Dimension

Unit: Inches (mm)

42 SOJ



16M-bit
 DRAM

44(50) TSOP II

