HM62V256 Series

Product Preview

32,768-Word x 8-Bit Low Voltage Operation CMOS Static RAM

HITACHI

Rev. 2
Sep. 10, 1993

Features

- Low voltage operation SRAM
  Operating Supply Voltage: 2.7 V to 3.6 V
- 0.8 µm Hi-CMOS process
- High speed
  Access time: 85/100 ns (max)
- Low power
  Standby: 0.60 µW (typ)
- Completely static memory
  No clock or timing strobe required
- Directly LVTTL compatible: All inputs and outputs

Ordering Information

Type No.	Access time	Package
HM62V256LFP-8T	85 ns	450 mil 28-pin plastic SOP (FP-28DA)
HM62V256LFP-10T	100 ns	
HM62V256LFP-8SLT	85 ns	
HM62V256LFP-10SLT	100 ns	
HM62V256LT-8	85 ns	8 mm x 14 mm 32-pin TSOP (normal type) (TFP-32DA)
HM62V256LT-10	100 ns	
HM62V256LT-8SL	85 ns	
HM62V256LT-10SL	100 ns	

Pin Description

Symbol	Function
A0 – A14	Address
I/O0 – I/O7	Input/output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground

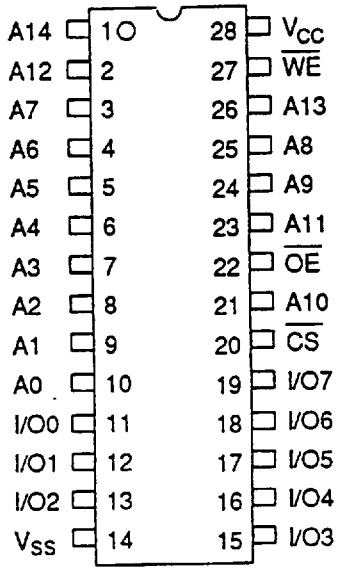
Product preview: This document contains information on a product under development. Hitachi reserves the right to change or discontinue the product without notice.

Hitachi semiconductor

ADE-203-136B (Z)

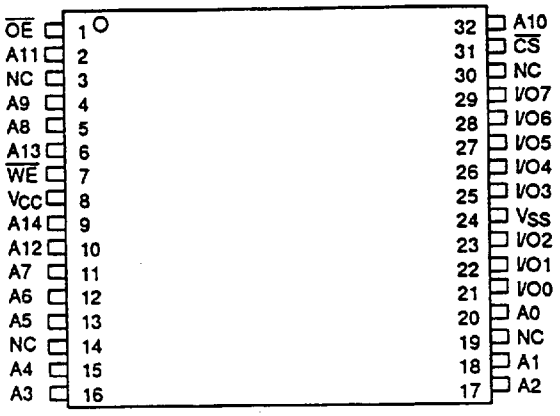
Pin Arrangement

HM62V256LFP Series



(Top View)

HM62V256LT Series



(Top View)

Function Table

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
X	H	X	Standby	I_{SB}, I_{SB1}	High-Z	—
H	L	H	Output disable	I_{CC}	High-Z	—
H	L	L	Read	I_{CC}	Dout	Read cycle (1)–(3)
L	L	H	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: 1. X: H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage*1	V_{CC}	−0.5 to 4.6	V
Terminal voltage*1	V_T	−0.5*2 to +V_{CC}+0.3	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to + 70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Note: 1. Relative to V_{SS}
2. V_T (min) = −3.0 V for pulse half-width ≤ 50 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	3.6	V
	V_{SS}	0	0	0	V
Input high(logic 1) voltage	V_{IH}	0.7V_{CC}	—	V_{CC}+0.3	V
Input low(logic 0) voltage	V_{IL}	−0.3*1	—	0.2V_{CC}	V

Note: 1. V_{IL} (min) = −3.0 V for pulse half-width ≤ 50 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 2.7 V to 3.6V, V_{SS} = 0 V)

Parameter		Symbol	Min	Typ*1	Max	Unit	Test conditions
Input leakage current		$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}
Output leakage current		$\|I_{LO}\|$	—	—	1	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current (DC)		I_{CCDC1}	—	—	15	mA	$\overline{CS}$ = V_{IL}, others = V_{IH}/V_{IL} $I_{I/O}$ = 0 mA
		I_{CCDC2}	—	—	10	mA	$\overline{CS}$ ≥ V_{CC} – 0.2 V, V_{IH} ≤ V_{CC} – 0.2 V, V_{IL} ≤ 0.2 V $I_{I/O}$ = 0 mA
Operating power supply current	HM62V256-8	I_{CCAC1}	—	—	27	mA	min cycle, duty = 100 %, $I_{I/O}$ = 0 mA $\overline{CS}$ = V_{IL}, others = V_{IH}/V_{IL}
	HM62V256-10		—	—	24		
		I_{CCAC2}	—	—	10	mA	Cycle time ≥ 1 µs, duty = 100 % $I_{I/O}$ = 0 mA, $\overline{CS}$ ≤ 0.2 V, V_{IH} ≥ V_{CC} – 0.2 V, V_{IL} ≤ 0.2 V
Standby V_{CC} current		I_{SB}	—	—	1	mA	$\overline{CS}$ = V_{IH}
		I_{SB1}	—	0.2	50	µA	Vin ≥ 0 V, $\overline{CS}$ ≥ V_{CC} – 0.2 V,
			—	0.2	10*2	µA	
Output low voltage		V_{OL}	—	—	0.2	V	I_{OL} = 20 µA
Output high voltage		V_{OH}	V_{CC}-0.2	—	—	V	I_{OH} = –20 µA

Note: 1. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and not guaranteed.
2. This characteristic is guaranteed only for L-SL version.

Capacitance (Ta = 25°C, f = 1.0 MHz)*1

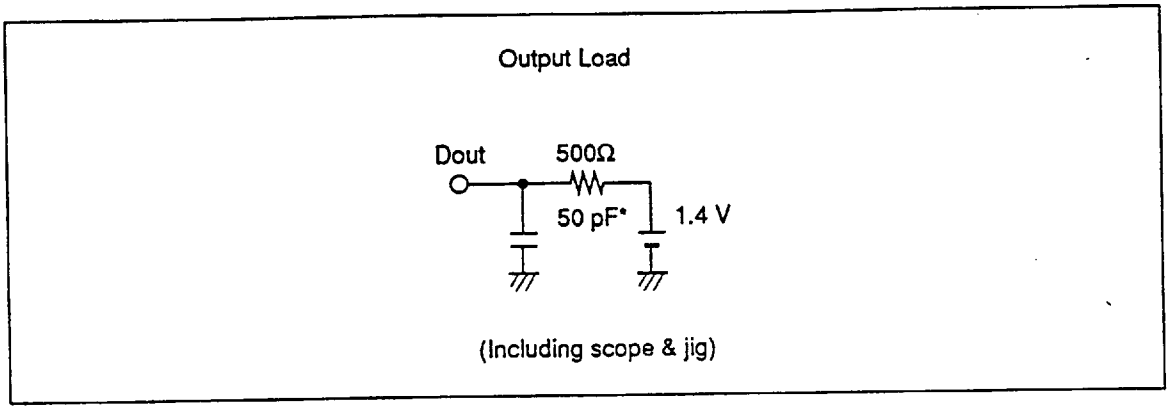
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	8	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 2.7 V to 3.6 V, unless otherwise noted.)

Test Conditions

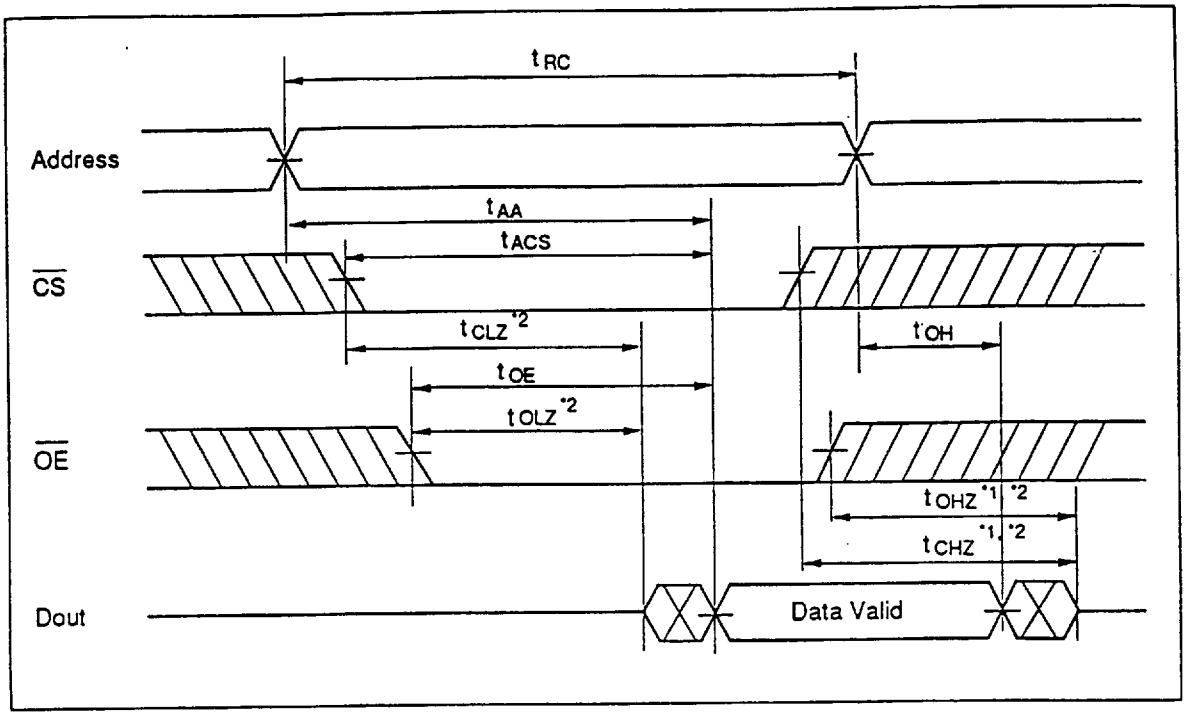
- Input pulse levels: 0.4 V to 2.4 V
- Input and output timing reference level: 1.4 V
- Input rise and fall times: 5 ns



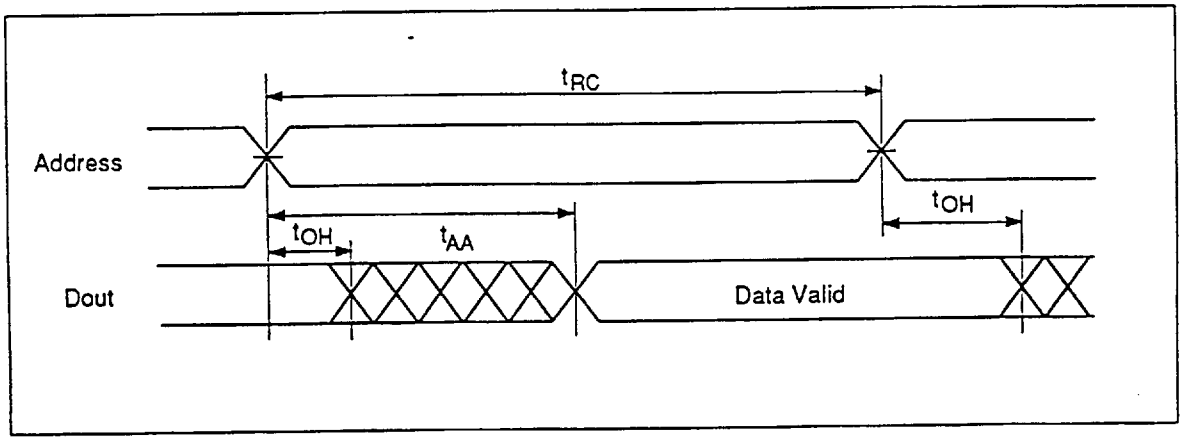
Read Cycle

		HM62V256-8		HM62V256-10			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t_{RC}	85	—	100	—	ns	
Address access time	t_{AA}	—	85	—	100	ns	
Chip select access time	t_{ACS}	—	85	—	100	ns	
Output enable to output valid	t_{OE}	—	45	—	50	ns	
Chip selection to output in low-Z	t_{CLZ}	10	—	10	—	ns	2
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	2
Chip deselection to output in high-Z	t_{CHZ}	0	30	0	35	ns	1, 2
Output disable to output in high-Z	t_{OHZ}	0	30	0	35	ns	1, 2
Output hold from address change	t_{OH}	10	—	10	—	ns	

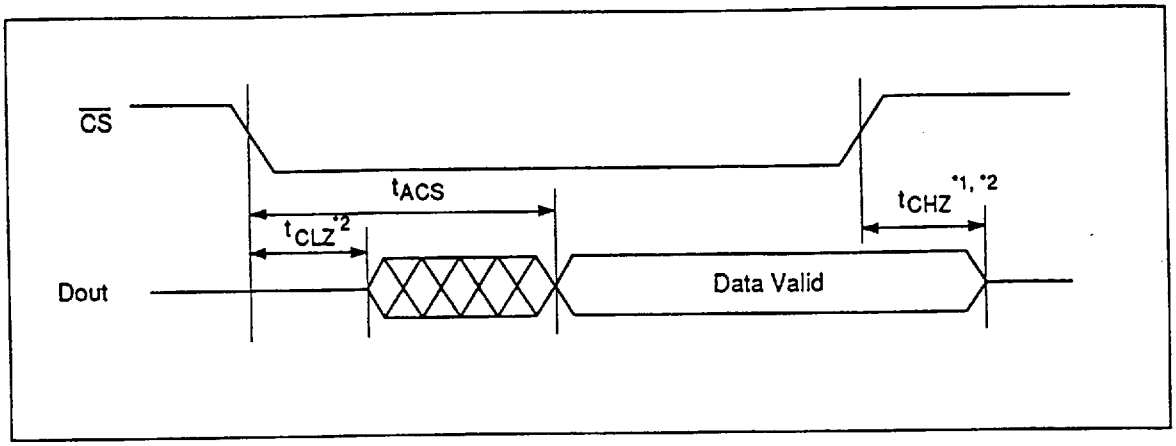
Read Timing Waveform (1)*3



Read Timing Waveform (2)*3 *4 *6



Read Timing Waveform (3)*3 *5 *6

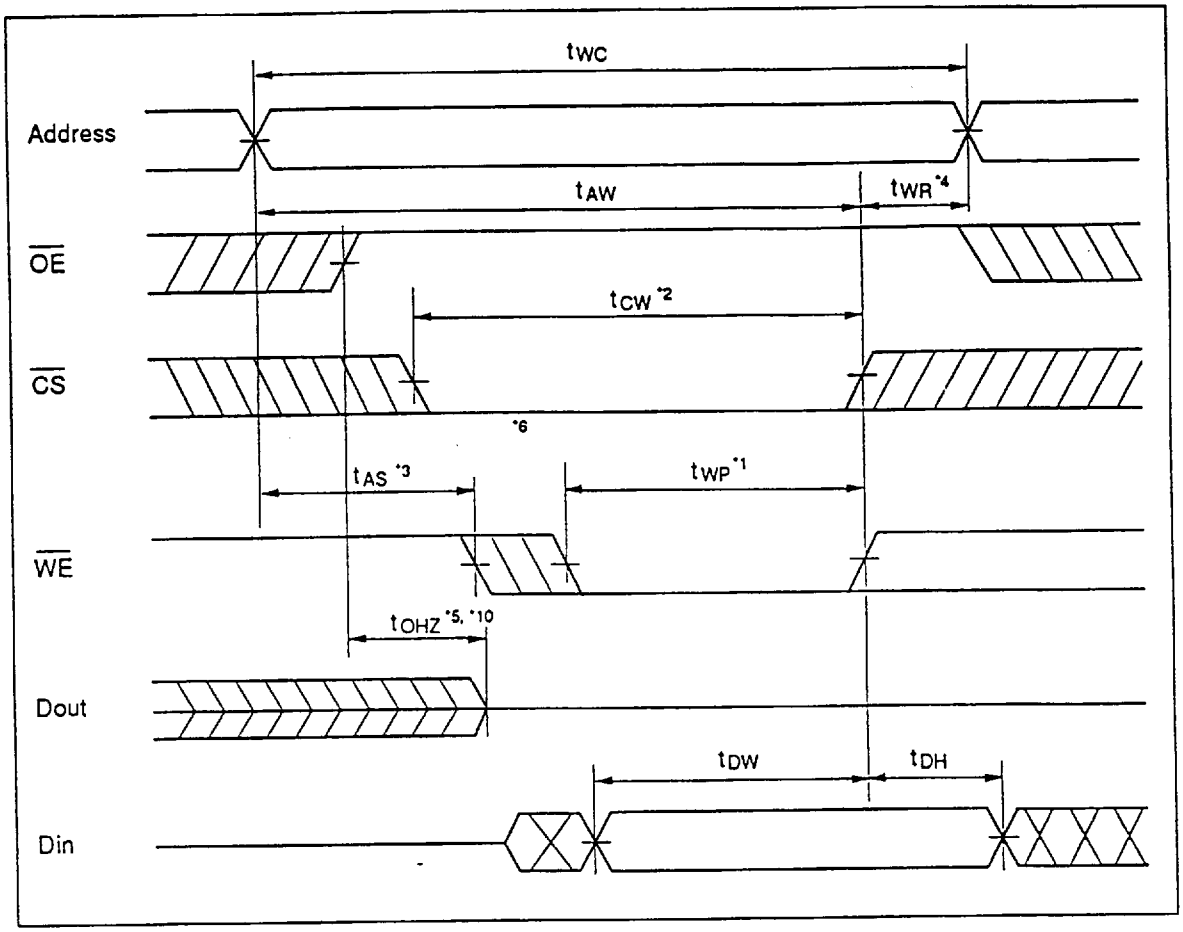


Notes: 1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not refered to output voltage levels.
2. This parameter is sampled and not 100 % tested.
3. $\overline{WE}$ is high for read cycle.
4. Device is continuously selected, $\overline{CS}$ = V_{IL}
5. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
6. $\overline{OE}$ = V_{IL}

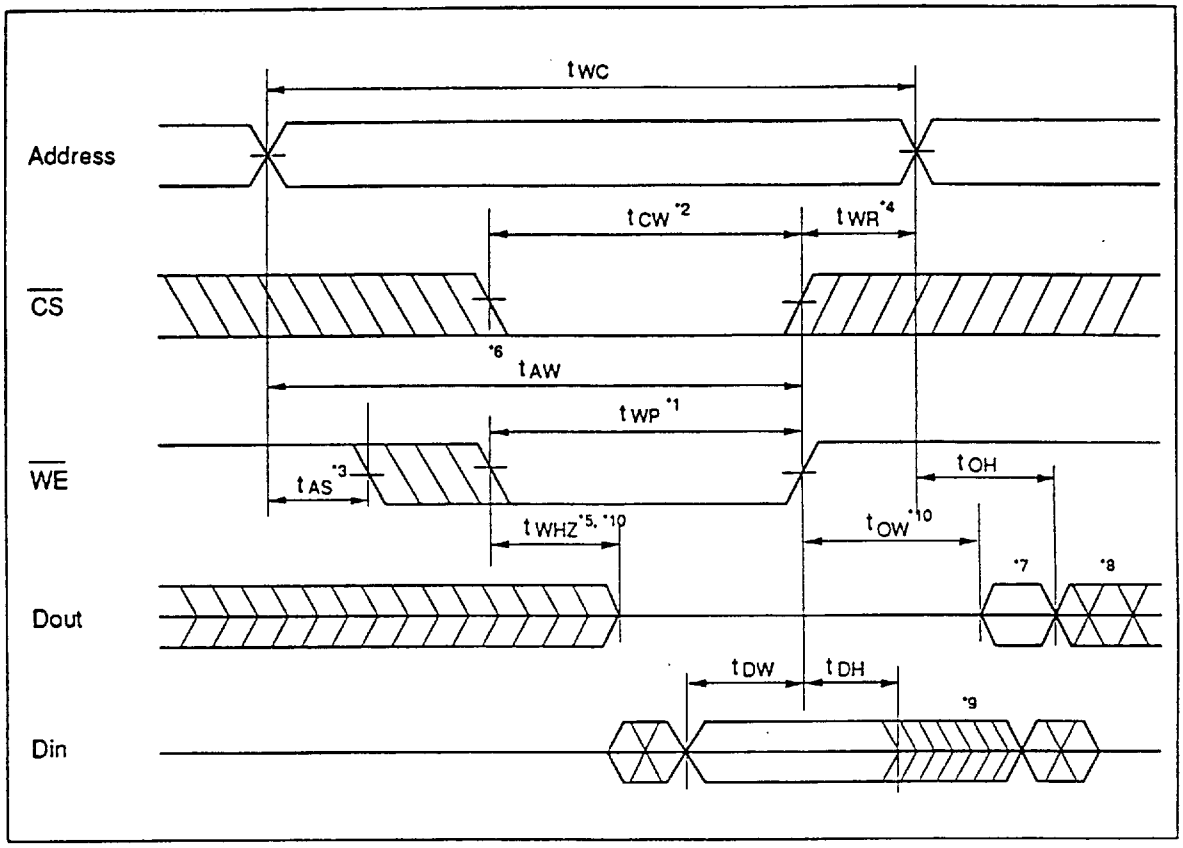
Write cycle

Parameter	Symbol	HM62V256-8 Min	HM62V256-8 Max	HM62V256-10 Min	HM62V256-10 Max	Unit	Notes
Write cycle time	t_{WC}	85	—	100	—	ns	
Chip selection to end of write	t_{CW}	75	—	80	—	ns	2
Address setup time	t_{AS}	0	—	0	—	ns	3
Address valid to end of write	t_{AW}	75	—	80	—	ns	
Write pulse width	t_{WP}	55	—	60	—	ns	1
Write recovery time	t_{WR}	0	—	0	—	ns	4
Write to output in high-Z	t_{WHZ}	0	30	0	35	ns	10, 11
Data to write time overlap	t_{DW}	35	—	40	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Output active from end of write	t_{OW}	10	—	10	—	ns	10
Output disable to output in high-Z	t_{OHZ}	0	30	0	35	ns	10, 11

Write Timing Waveform (1) ($\overline{OE}$ Clock)



Write Timing Waveform (2) ($\overline{OE}$ Low Fixed)

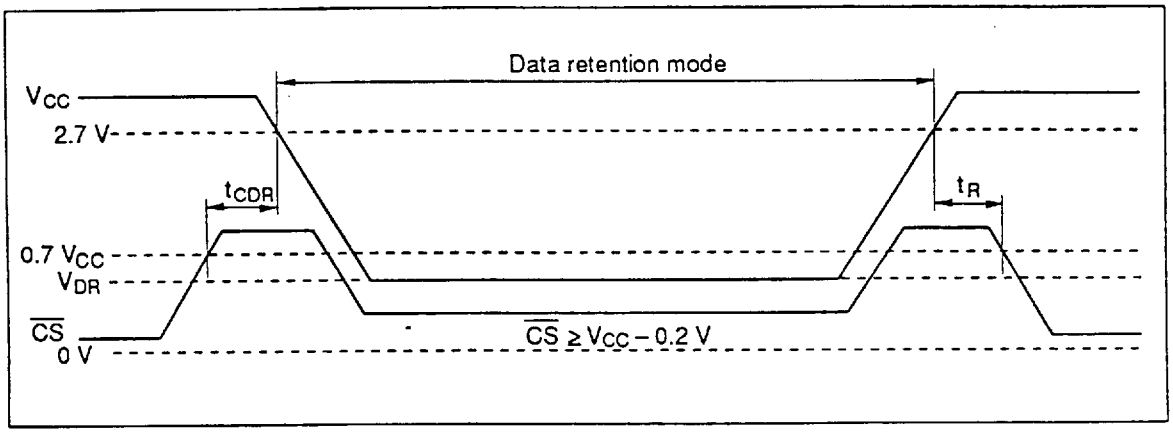


Notes:
1. A write occures during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CS}$ going low or $\overline{WE}$ going low. A write ends at the earlier transition of $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the earlier of $\overline{WE}$ or $\overline{CS}$ going high to the end of write cycle.
5. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
6. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
7. Dout is the same phase of the write data of this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the output must not be applied to them.
10. This parameter is sampled and not 100% tested.
11. t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achive the open circuit conditions and are not refered to output voltage levels.

Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	3.6	V	$\overline{CS} \geq V_{CC} - 0.2$ V, Vin ≥ 0 V
Data retention current	I_{CCDR}	—	—	27*2	µA	V_{CC} = 2.7 V, Vin ≥ 0 V, $\overline{CS} \geq V_{CC} - 0.2$ V
		—	—	7*3	ns	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*4	—	—	ns	

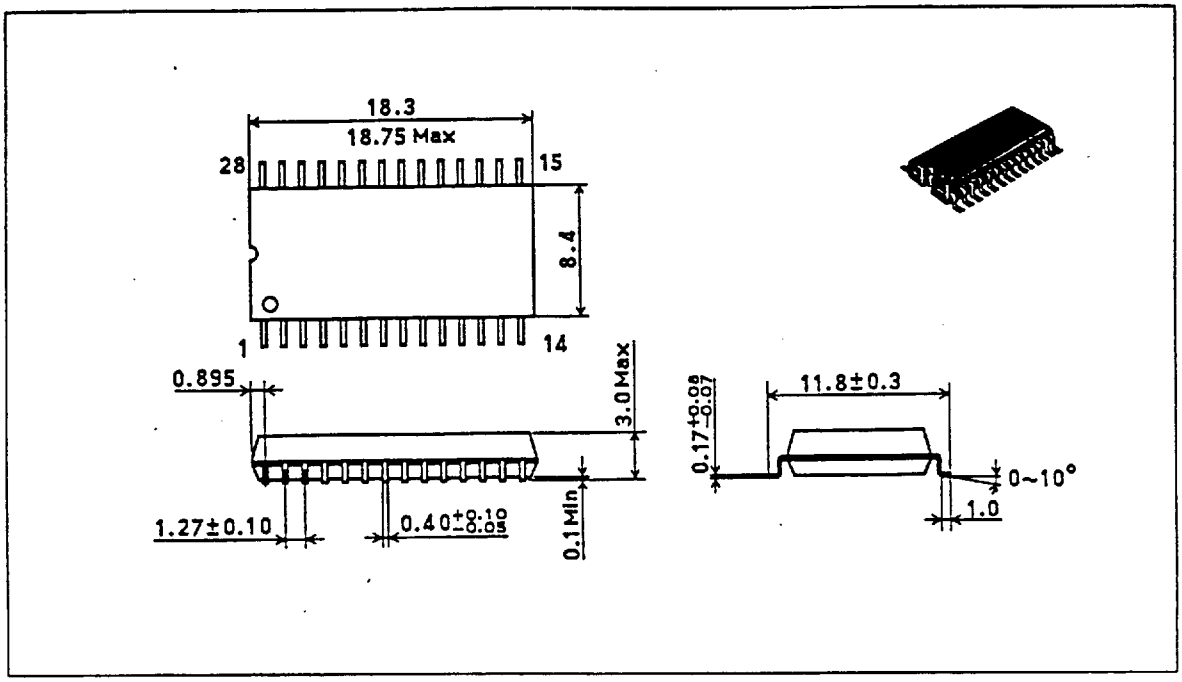
Low V_{CC} Data Retention Timing Waveform



Notes: 1. Typical values are at V_{CC} = 2.7 V, Ta = 25°C and not guaranteed.
2. 18 µA max. at Ta = 0 to 40°C.
3. 2.0 µA max. at Ta = 0 to 40°C. (only for L-SL version)
4. t_{RC} = read cycle time.
5. $\overline{CS}$ controls address buffer, $\overline{WE}$ buffer, $\overline{OE}$ buffer, and Din buffer. If $\overline{CS}$ controls data retention mode, other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

Package Dimentions

HM62V256LFP Series (FP-28DA)



HM62V256LT Series (TFP-32DA)