

# RAJ240080

R01DS0299EJ0010

Rev.0.01

## Integrated Li-ION Battery Management IC for 2-5 Series Cell

2016/8/10

### 1. Introduction

#### 1.1 Features

Fully integrated battery management product including battery capacity measurement and protection.

Supports 2-5 Li-Ion or Li-Polymer battery cells in series.

Ultra-low power Renesas RL78 CPU core

Built-in flash memory (block erase/write protection)

- Flash ROM: 64 KB
- Data flash: 4 KB

Internal SRAM: 5.5 KB

Current integrating circuit (18-bit  $\Delta\Sigma A/D$ )

15-bit  $\Delta\Sigma A/D$  converter (external 3 channels, internal 5 channels including simple temperature sensor)

High side N-ch FET control circuit for charge and discharge current protection

Overcurrent detection circuit (discharge short-circuit current (2 channels), charge/discharge overcurrent, and wake-up current)

Battery voltage detection circuit (5 cells)

Battery cell conditioning circuit (5 cells)

Pack+ terminal voltage detection circuit

FUSE control circuit

MCU built-in high speed on-chip clock generator

AFE on-chip oscillator clock (4.194 MHz)

MCU runaway detection circuit

MCU build-in watchdog timer

Series regulator (VREG2: 3.3 V, VREG1: 1.8 V)

Reset circuit (VREG2, VREG1 monitoring)

High speed on-chip clock oscillator

- High speed operation : 1 to 32 MHz
- Low speed operation : 1 to 8 MHz

I/O port: 22

• CMOS input/output: 16

• CMOS input: 2

• N-ch open drain: 2

• High voltage input: 1

• High voltage output: 1

Serial interface:

- I2C
- UART
- Simplified I2C

MCU 16-bit timer: 5 channels

MCU 12-bit interval timer: 1 channel

AFE timer (setting range: 125 ms to 64 s)

8 bits PWM signal generator

Intel® Dynamic Battery Power Technology support

Impedance measurement circuit

Built-in on-chip debug function

Self programming function support

Power supply voltage: VCC = 4.0 to 28 V

Operation ambient temperature: Ta = -20 to +85°C

Package Information:

Plastic mold QFP (9mm x 9mm x 1.5mm)

#### 1.2 Applications

- e-Bikes, e-Scooters, and Pedal-Assist Bicycles
- Power Tools, Battery Backup Systems (UPS)
- Telecom Power Systems

#### 1.3 Description

RAJ240080 is Renesas battery management IC which incorporates a variety of battery fuel gauge features. Embedded Renesas RL78 CPU core has multiple low power modes and achieve high performance in ultra-low power operation. RAJ240080 product consists of MCU device and AFE device in a single package. Fuel gauge control firmware is stored in embedded flash memory and controls embedded analog and digital circuits to execute battery voltage / current / temperature measurement, remaining capacity estimation, over current / voltage / temperature protection and other battery management operations.

---

## Table of Contents

<b>1. Introduction</b> .....	<b>1</b>
<b>1.1 Features</b> .....	<b>1</b>
<b>1.2 Applications</b> .....	<b>1</b>
<b>1.3 Description</b> .....	<b>1</b>
<b>2. Pin Assignment</b> .....	<b>4</b>
<b>2.1 Pin Assignment Diagram</b> .....	<b>4</b>
<b>2.2 Pin Function Table</b> .....	<b>5</b>
<b>2.3 Pin Equivalent Diagram</b> .....	<b>7</b>
<b>3. ELECTRICAL SPECIFICATIONS</b> .....	<b>11</b>
<b>3.1 Absolute Maximum Ratings</b> .....	<b>11</b>
<b>3.2 Power supply voltage condition</b> .....	<b>13</b>
<b>3.3 Oscillation circuit characteristics</b> .....	<b>13</b>
3.3.1 On-chip oscillator characteristics .....	13
<b>3.4 DC characteristics</b> .....	<b>14</b>
3.4.1 Pin characteristics .....	14
3.4.2 Supply current characteristics .....	16
<b>3.5 Peripheral function characteristics</b> .....	<b>17</b>
3.5.1 Serial array unit .....	17
3.5.2 Serial interface IICA .....	23
3.5.3 On-chip debug (UART) .....	25
3.5.4 Interrupt .....	25
<b>3.6 Analog front end characteristics</b> .....	<b>26</b>
3.6.1 A/D converter characteristics .....	26
3.6.2 Current integrating circuit characteristics .....	26
3.6.3 Overcurrent detection circuit characteristics .....	27
3.6.4 Series regulator circuit characteristics .....	28
3.6.5 Battery voltage detection circuit characteristics .....	28
3.6.6 Charge/discharge FET control circuit characteristics .....	29
3.6.7 Conditioning circuit characteristics .....	31
<b>3.7 Flash memory programming characteristics</b> .....	<b>31</b>
<b>4. Function Description</b> .....	<b>32</b>
<b>4.1 Overview</b> .....	<b>32</b>
<b>4.2 System block diagram</b> .....	<b>32</b>
<b>4.3 MCU Block Diagram</b> .....	<b>33</b>
<b>4.4 AFE Block Diagram</b> .....	<b>34</b>
<b>4.5 Feature List</b> .....	<b>35</b>
<b>4.6 Feature Description</b> .....	<b>37</b>
4.6.1 ADC Circuit .....	37
4.6.2 Battery Voltage detection circuit .....	40
4.6.3 Current Integrating Circuit .....	41

---

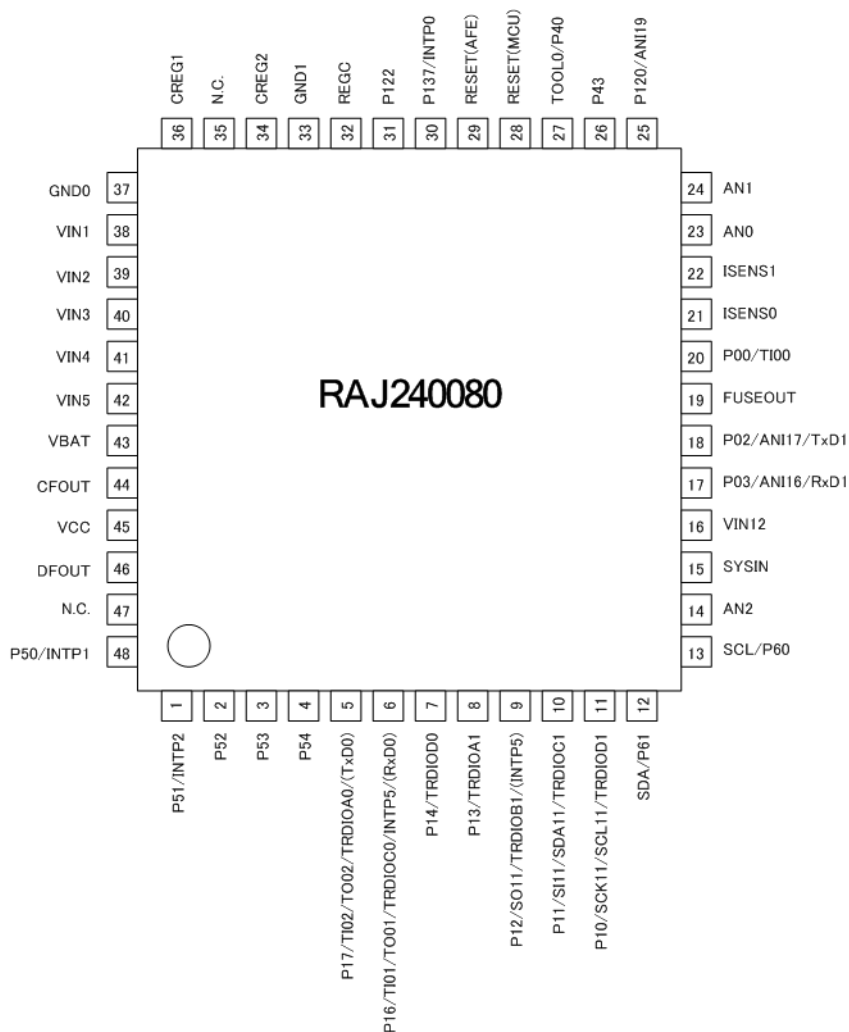
4.6.4	Current Integration Circuit in Impedance Measurement Mode .....	42
4.6.5	FET control circuit.....	44
4.6.6	Overcurrent Detection Circuit .....	45
4.6.7	Series Regulator.....	47
4.6.8	Reset Circuit .....	48
4.6.9	Serial Interface IICA .....	49
4.6.10	Serial Array Unit .....	50
4.6.11	Conditioning circuit .....	53
4.6.12	Fuse control circuit .....	53
4.6.13	High voltage port .....	55
4.6.14	MCU runaway detection Circuit.....	55
<b>5.</b>	<b>Application Guideline .....</b>	<b>58</b>
5.1	Typical Application Specification .....	58
5.2	Typical Application Circuit .....	59
5.3	Circuit Design Guideline.....	60
5.3.1	Cell voltage monitor circuit .....	60
5.3.2	Charger connect detection circuit.....	61
5.3.3	Current monitor.....	61
5.3.4	Fuse control.....	62
5.3.5	Protection FET control.....	62
5.3.6	Thermistor .....	63
5.3.7	System presence.....	64
5.3.8	Communication line.....	64
5.3.9	Power supply path.....	65
5.3.10	CREG1/CREG2/REGC capacitance .....	65
5.4	Layout Guidelines .....	66
5.4.1	Summary .....	66
5.4.2	ESD protections on each terminal (basic policy).....	67
5.4.3	Pack+, Pack- .....	67
5.4.4	How AGND and AGND2 must be connected to the ground .....	68
5.4.5	Bypass capacitor between VCC and GND0.....	68
5.4.6	ISENS0, ISENS1 .....	69
5.4.7	SMBus .....	69
5.4.8	Unused Pins .....	69
5.4.9	Cell GND .....	69
<b>6.</b>	<b>Packaging Information.....</b>	<b>70</b>

## 2. Pin Assignment

### 2.1 Pin Assignment Diagram

Package: 48 pin plastic mold QFP (9.0mm X 9.0mm)

(Top View)



**Cautions 1.** REGC pin connects to GND1 pin through a capacitor (0.47 to 1 $\mu$ F)

2. CREG1 pin connects to GND0 pin through a capacitor (1  $\mu$ F).

3. CREG2 pin connects to GND1 pin through a capacitor (2.2  $\mu$ F).

**Remarks 1.** Pin function refers to [2.2Pin Function Table].

2. The function shown above in ( ) is assigned by setting of peripheral I/O re-direction register 0 (PIOR0).

## 2.2 Pin Function Table

(1/1)

Number	Name	Type	Description
1	P51/INTP2	DIO(8-R)	Port 51 Leave open in output mode if not used.
2	P52	DIO(8-R)	Port 52 Leave open in output mode if not used.
3	P53	DIO(5-AN)	Port 53 Leave open in output mode if not used.
4	P54	DIO(5-AN)	Port 54 Leave open in output mode if not used.
5	P17/TI02/TO02/TRDIOA0/(TxD0)	DIO(5-BC)	Port 17 Leave open in output mode if not used.
6	P16/TI01/TO01/TRDIOC0/INTP5/(RxD0)	DIO(5-BC)	Port 16 Leave open in output mode if not used.
7	P14/TRDIOD0	DIO(5-AN)	Port 14 Leave open in output mode if not used.
8	P13/TRDIOA1	DIO(5-BB)	Port 13 Leave open in output mode if not used.
9	P12/SO11/TRDIOB1/(INTP5)	DIO(5-BB)	Port 12 Leave open in output mode if not used.
10	P11/SI11/SDA11/TRDIOC1	DIO(8-R)	Port 11 Leave open in output mode if not used.
11	P10/SCK11/SCL11/TRDIOD1	DIO(5-AN)	Port 10 Leave open in output mode if not used.
12	SDA/P61	DIO(13-R)	I2C Bus data I/O Input/Output
13	SCL/P60	DIO(13-R)	I2C Bus data I/O Input/Output
14	AN2	AIN	Analog Input
15	SYSIN	HVIN	System detection pin
16	VIN12	AIN	Charger connection monitoring
17	P03/ANI16/RxD1	DIO(11-V)	Port 03 Leave open in output mode if not used.
18	P02/ANI17/TxD1	DIO(11-U)	Port 02 Leave open in output mode if not used.
19	FUSEOUT	HVIO	Fuse FET control
20	P00/TI00	DIO(8-R)	Port 00 Leave open in output mode if not used.
21	ISENS0	AIN	Analog input for current integration circuit
22	ISENS1	AIN	Analog input for current integration circuit
23	AN0	AIN	Analog Input
24	AN1	AIN	Analog Input
25	P120/ANI19	DIO(11-U)	Port 120 Leave open in output mode if not used.
26	P43	DIO(5-AN)	Port 43 Leave open in output mode if not used.
27	TOOL0/P40	DIO(8-R)	Data Input/Output for tools
28	RESET(MCU)	DIN (2)	Reset Input
29	RESET(AFE)	OUT	Reset Output
30	P137/INTP0	DIN (2)	Port 137 Connect to GND1 through a resistor if not used.
31	P122	DIN (37-C)	Port 122 Connect to GND1 through a resistor if not used.
32	REGC	P	Regulator capacitor connection
33	GND1	P	Ground
34	CREG2	P	Regulator capacitor connection
35	NC	NC	No connect
36	CREG1	P	Regulator capacitor connection

37	GND0	P	Ground
38	VIN1	AIN	Battery voltage input
39	VIN2	AIN	Battery voltage input
40	VIN3	AIN	Battery voltage input
41	VIN4	AIN	Battery voltage input
42	VIN5	AIN	Battery voltage input
43	VBAT	AIN	Battery voltage input
44	CFOUT	HVO	Charge FET control
45	VCC	P	Power supply
46	DFOUT	HVO	Discharge FET control
47	NC	NC	No connect
48	P50/INTP1	DIO(5-AN)	Port 50 Connect to GND1 through a resistor if not used.

**HVO**    **high voltage output**

**HVIN**   **high voltage input**

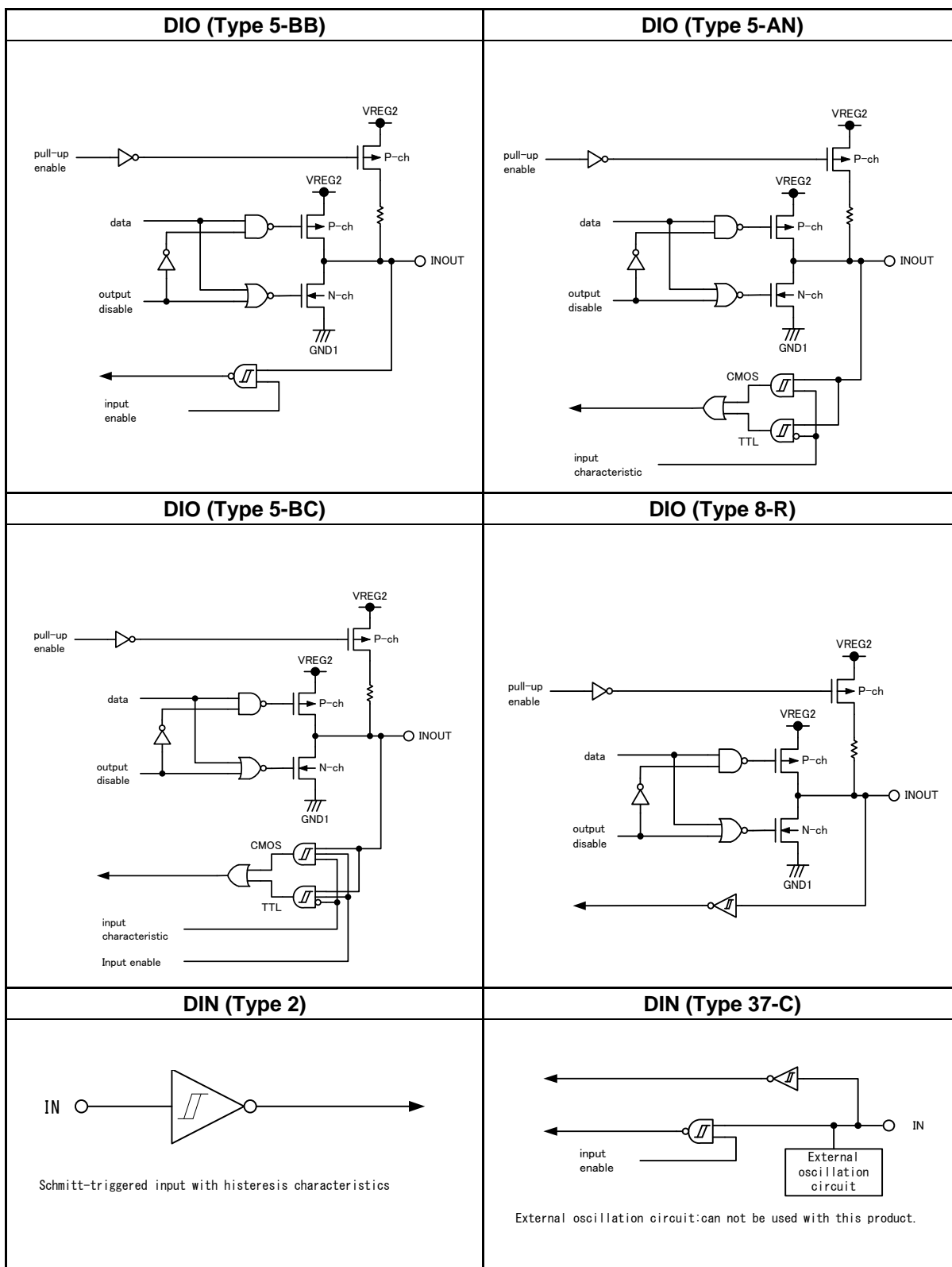
**HVIO**   **high voltage input/output**

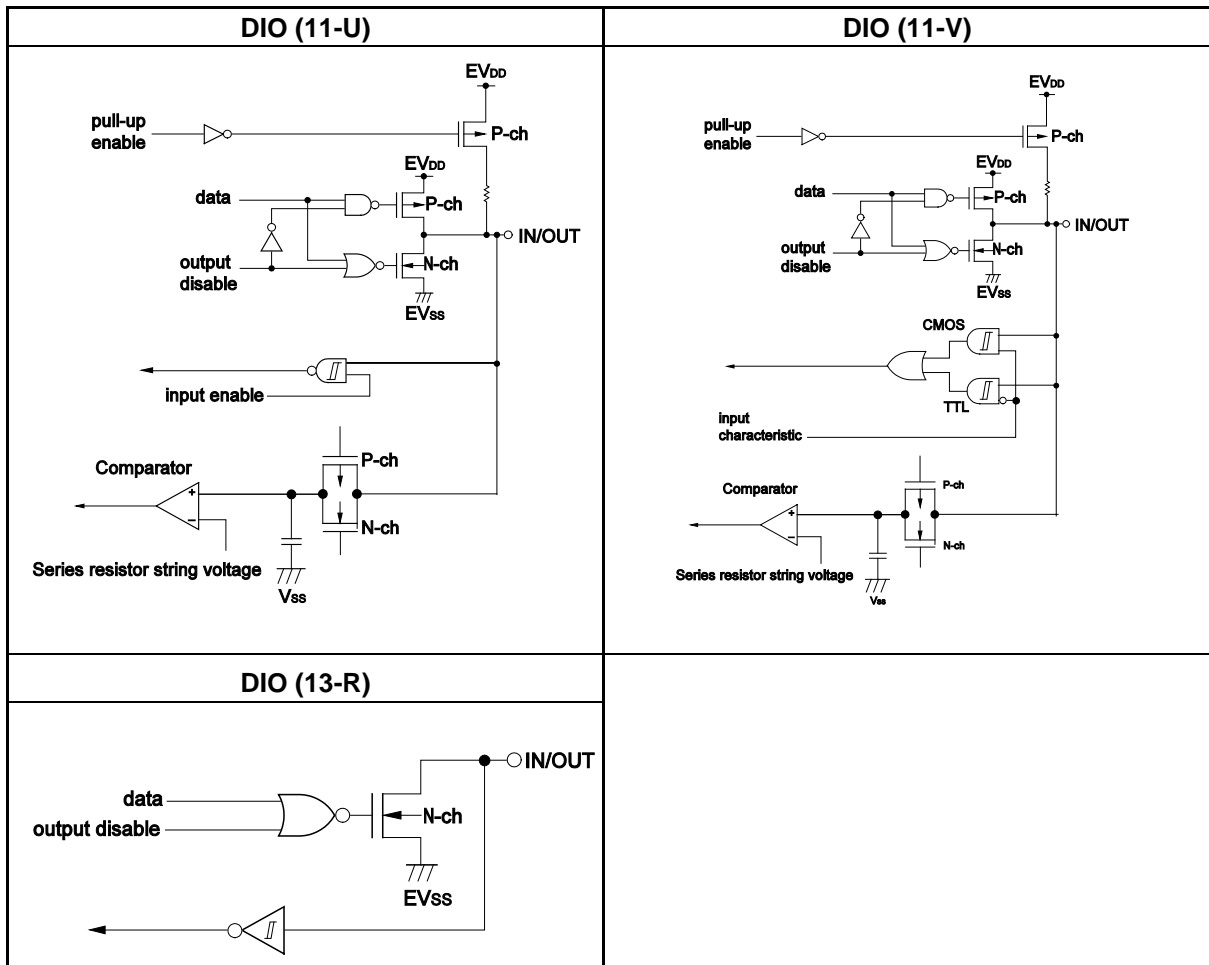
**P**        **power**

**DIO**     **digital I/O**

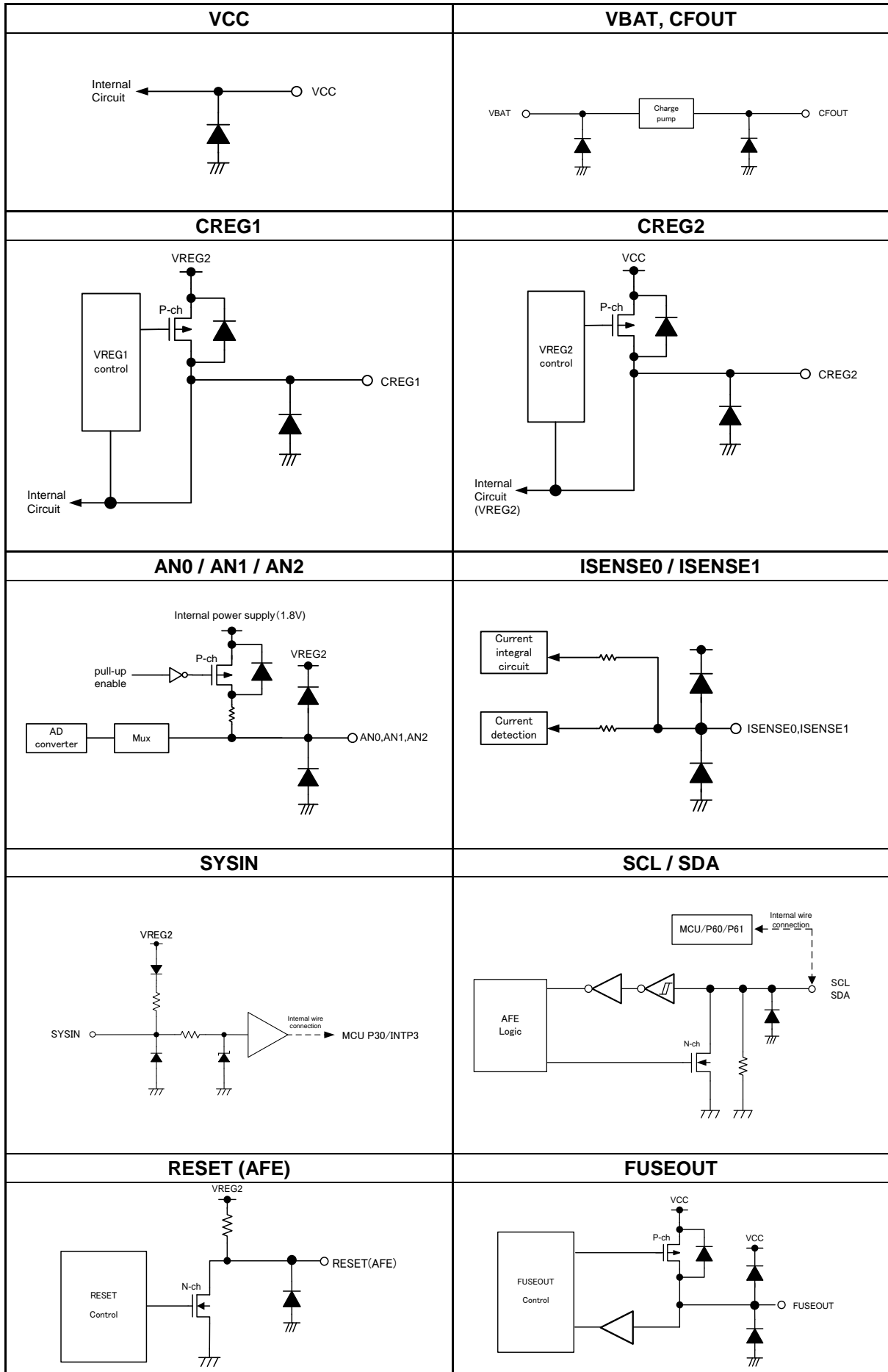
**AIN**     **analog input**

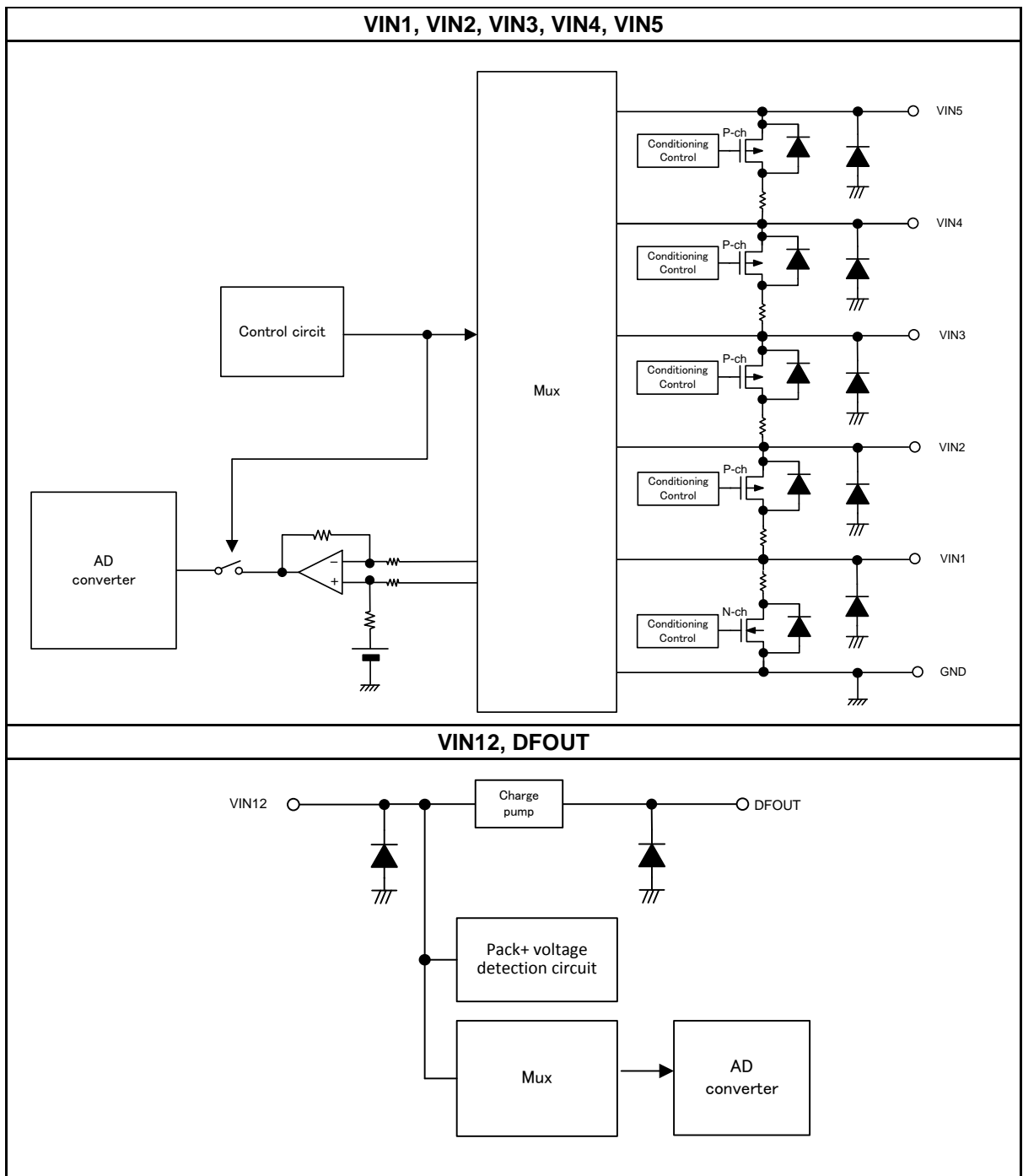
## 2.3 Pin Equivalent Diagram











### 3. ELECTRICAL SPECIFICATIONS

**Caution** This product has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

#### 3.1 Absolute Maximum Ratings

Absolute Maximum Ratings (TA = 25 °C)

Parameter	Symbols	Condition	Ratings	Unit	
Supply voltage	VCC		-0.5 to 35	V	
	GND0, GND1		-0.5 to 0.3	V	
CREG1 input voltage	VREG1	CREG1	-0.3 to 2.0 <sup>Note 2</sup>	V	
CREG2 input voltage	VREG2	CREG2	-0.3 to 5.5 <sup>Note 3</sup>	V	
REGC pin input voltage	VIREGC	REGC	-0.3 to 2.8 And -0.3 to VREG2 + 0.3 <sup>Note 1</sup>	V	
Input voltage	VI1	P00, P02, P03, P10 to P14, P16, P17, P43, P50 to P54, P120, P122, P137, TOOL0(P40), RESET(MCU)	-0.3 to VREG2 + 0.3	V	
	VI2	SDA(P61), SCL(P60) (N-ch open drain)	-0.3 to 5.5	V	
	Vin-H	VIN5, VIN4, VIN3, VIN2, VIN1, VIN12, SYSIN	-0.5 to 35	V	
	Vin-B	VIN5-VIN4, VIN4-VIN3, VIN3-VIN2, VIN2-VIN1, VIN1-GND0	-0.5 to 7	V	
Output voltage	VO1	P00, P02, P03, P10 to P14, P16, P17, P43, P50 to P54, P120, TOOL0(P40), SDA(P61), SCL(P60)	-0.3 to VREG2 + 0.3	V	
	VO-DH	DFOUT	-0.5 to 35	V	
	VO-CH	CFOUT	-0.5 to 35	V	
	VO-FH	FUSEOUT	-0.3 to VCC + 0.3 And -0.5 to 35	V	
Analog input voltage	VAI	AN0, AN1, AN2	-0.3 to 2.0	V	
	VIS	ISENS0, ISENS1	-0.3 to 2.0	V	
High-level output current	IOH	P02, P03, P10 to P17, P43, P50 to P54, P120	Per pin	-40	mA
			Total of all pins	-100	mA
	IOH-FH	FUSEOUT	-10	mA	
Low-level Output current	IOL	P02, P03, P10 to P17, P43, P50 to P54, P120	Per pin	40	mA
			Total of all pins	100	mA
Power consumption	Pd	Topr=25°C	300	mW	
Operating ambient Temperature	Topr		-20 to 85	°C	
Storage temperature	Tstg		-65 to 150	°C	

- 
- Notes 1.** Connect the REGC pin to GND1 via a capacitor (0.47 to 1 $\mu$ F). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.
- 2.** Connect the CREG1 pin to GND0 via a capacitor (1  $\mu$  F). This value regulates the absolute maximum rating of the CREG1 pin. Do not use this pin with voltage applied to it.
- 3.** Connect the CREG2 pin to GND1 via a capacitor (2.2  $\mu$  F). This value regulates the absolute maximum rating of the CREG2 pin. Do not use this pin with voltage applied to it.

VREG2 is power supply built-in IC.it is a 3.3V supply for IC.

**Caution.** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remark.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 3.2 Power supply voltage condition

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	VCC/VBAT		4.0	-	28	V
	GND0/GND1		-	0	-	V

## 3.3 Oscillation circuit characteristics

### 3.3.1 On-chip oscillator characteristics

( $T_A = -20$  to  $+85$  ° C,  $4.0\text{ V} \leq V_{CC} \leq 28\text{ V}$ ,  $GND0 = GND1 = 0\text{ V}$ )

Oscillator	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator Clock frequency <sup>Note 1</sup>	$f_{iH}$		-	8	-	MHz
Low-speed on-chip oscillator Clock frequency	$f_{iL}$		-	15	-	kHz
AFE on-chip oscillator Clock frequency <sup>Note 2</sup>	$f_{oco}$		-	4.194	-	MHz
AFE on-chip oscillator Clock frequency accuracy	-		-2	-	+2	%

**Notes 1.** High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H/010C2H) and bits 0 to 2 of the HOCODIV register.

**2.** This value is when it writes trimming data stored in flash memory to the OCOTRIM0 to OCOTRIM2 register.

## 3.4 DC characteristics

### 3.4.1 Pin characteristics

( $T_A = -20$  to  $+85$  °C,  $4.0\text{ V} \leq V_{CC} \leq 28\text{ V}$ ,  $V_{REG2} = 3.3\text{ V}$ ,  $GND0 = GND1 = 0\text{ V}$ )

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage High	VIH1	P02 to P03, P10 to P17, P43, P50 to P54, P120, P122, P137, TOOL0, RESET(MCU)	0.8 VREG2	-	VREG2	V	
	VIH2	SCL(P60), SDA(P61)	2.1	-	VREG2	V	
	VIH3	SYSIN	0.7 VREG2	-	VREG2	V	
	VIH4	FUSEOUT	2	-	VCC	V	
	VIH5	P01, P03, P04, P10, P14 to P17, P30, P50, P55 (TTL Input buffer)	2	-	VREG2	V	
Input voltage low	VIL1	P02 to P03, P10 to P17, P43, P50 to P54, P120, P122, P137, TOOL0, RESET(MCU)	0	-	0.2 VREG2	V	
	VIL2	SCL(P60), SDA(P61)	0	-	0.8	V	
	VIL3	SYSIN	0	-	0.3 VREG2	V	
	VIL4	FUSEOUT	0	-	0.5	V	
	VIL5	P01, P03, P04, P10, P14 to P17, P30, P50, P55 (TTL Input buffer)	0	-	0.5	V	
Output voltage High	VOH1	P02 to P03, P10 to P17, P43 P50, P55	IOL = -1.5mA VREG2 - 0.5	-	VREG2	V	
Output voltage Low	VOL1	P10 to P12, P16, P17, P40	IOL = 1.5mA	-	0.4	V	
	VOL2	SCL(P60), SDA(P61)	IOL = 3.0 mA	-	0.4	V	
FUSEOUT Output High Voltage	V <sub>OH-FUSE</sub>	External Pulldown 100 kΩ	VCC - 0.5	-	-	V	
Input leak current High	ILIH1	P02 to P03, P10 to P17, P43, P50 to P54, P120, P122, P137, TOOL0, RESET(MCU)	VI = VREG2	-	1	μA	
Input leak current Low	ILIL1	P02 to P03, P10 to P17, P43, P50 to P54, P120, P122, P137, TOOL0, RESET(MCU)	VI = GND1	-	-1	μA	
Pull-up resistor	RU	P02 to P03, P10 to P17, P43, P50 to P54, P120	VI = GND1, When input port	10	20	100	kΩ
	R <sub>UA</sub>	AN0, AN1	VI = GND1	7.5	(10)	12.5	kΩ
	R <sub>UA</sub>	RESET (MCU)	VI = GND1	-	(20)	-	kΩ

---

**Notes 1.** The maximum value of  $V_{IH}$  of pins P10, P11, and P17 is VREG2, even in N-ch open drain mode.

2. P10, P11, P17 do not output a high-level in N-ch open drain mode.

**Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. About pin characteristics of CFOUT, DFOUT, refer to [3.6.6 charge/discharge FET control circuit characteristics]

3. About pin characteristics of VIN1, VIN2, VIN3, VIN4, and VIN5 refer to [3.6.5 Battery voltage detection circuit characteristics]

4. The parenthetical values are for reference.

### 3.4.2 Supply current characteristics

( $T_A = -20$  to  $+85$  °C,  $4.0\text{ V} \leq V_{CC} \leq 28\text{ V}$ ,  $V_{REG2} = 3.3\text{ V}$ ,  $GND0 = GND1 = 0\text{ V}$ )

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Supply Current <sup>Note 1</sup>	ICC1	Normal operation mode	Low-speed	fHOCO = 8 MHz	-	( 2.0 )	-	mA
		<sup>Note 2</sup>	Operation	fIH = 8 MHz				
	ICC2	Wait mode <sup>Note 3</sup>	STOP mode	$T_A = +25$ ° C	-	( 150 )	-	µA
	ICC3	Power down mode	$V_{CC} \leq 14\text{ V}$		-	( 0.5 )	1	µA

**Notes 1.** This is the current which flows in VCC.

2. This value includes the operation currents of the integrating current circuit, overcurrent detection circuit, charge FET control and discharge FET control.
3. This value includes the operation currents of overcurrent detection circuit, charge FET control and discharge FET control.

**Remarks 1.** fHOCO: high-speed on-chip oscillator clock frequency (32 MHz max.)

2. fIH: high-speed on-chip oscillator clock frequency (32 MHz max.)
3. Temperature condition of the TYP. Value is  $T_A = 25$  °C.
4. The numerical value in a parenthesis is a reference value.



## 3.5 Peripheral function characteristics

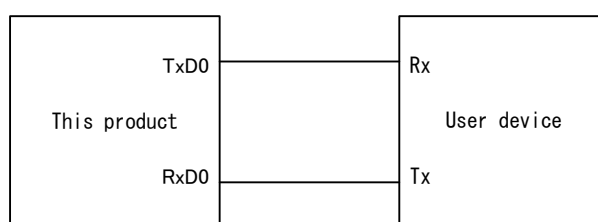
### 3.5.1 Serial array unit

(1) During communication at same potential (UART mode) (Dedicated baud rate generator output)

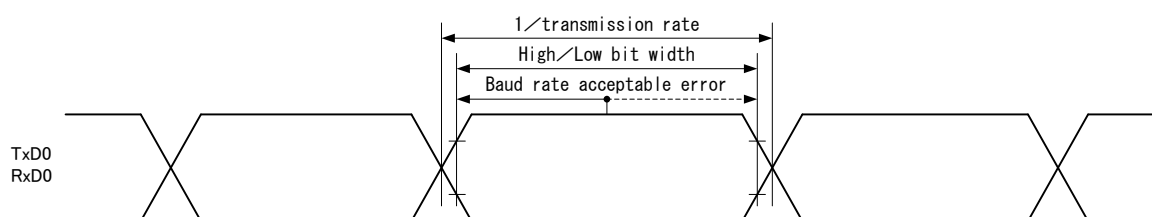
( $T_A = -20$  to  $+85$  ° C,  $4.0\text{ V} \leq V_{CC} \leq 28\text{ V}$ ,  $V_{REG2} = 3.3\text{ V}$ ,  $GND0 = GND1 = 0\text{ V}$ )

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transmission rate			-	-	$f_{MCK}/6$	bps

UART mode connection diagram (During communication at same potential)



UART mode bit width (During communication at same potential) (reference)



**Caution** Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**Remarks 1.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

**2.**  $f_{MCK}$ : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(2) During communication at same potential (CSI mode) (master mode ( $f_{MCK}/4$ ),  $\overline{SCKp}$ ...internal clock output)

( $T_A = -20$  to  $+85$  ° C,  $4.0 V \leq V_{CC} \leq 28 V$ ,  $V_{REG2} = 3.3 V$ ,  $GND0 = GND1 = 0 V$ )

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	$t_{KCY1}$		125 <sup>Note 1</sup>	-	-	ns
$\overline{SCKp}$ high-/low-level width	$t_{KH1}$ , $t_{KL1}$		$t_{KCY1}/2-18$	-	-	ns
SIp setup time (to $\overline{SCKp} \uparrow$ ) <sup>Note 2</sup>	$t_{SIK1}$		44	-	-	ns
SIp hold time (to $\overline{SCKp} \uparrow$ ) <sup>Note 2</sup>	$t_{KSI1}$		19	-	-	ns
Delay time from $\overline{SCKp} \downarrow$ to SOp output <sup>Note 3</sup>	$t_{KSO1}$	$C = 30 \text{ pF}$ <sup>Note 4</sup>	-	-	25	ns

**Notes 1.** The value must also be  $4/f_{CLK}$  or more.

**2.** When  $DAPmn = 0$  and  $CKPmn = 0$ , or  $DAPmn = 1$  and  $CKPmn = 1$ . The SIp setup time becomes “to  $\overline{SCKp} \downarrow$ ” when  $DAPmn = 0$  and  $CKPmn = 1$ , or  $DAPmn = 1$  and  $CKPmn = 0$ .

**3.** When  $DAPmn = 0$  and  $CKPmn = 0$ , or  $DAPmn = 1$  and  $CKPmn = 1$ . The SIp hold time becomes “from  $\overline{SCKp} \uparrow$ ” when  $DAPmn = 0$  and  $CKPmn = 1$ , or  $DAPmn = 1$  and  $CKPmn = 0$ .

**4** C is the load capacitance of the  $\overline{SCKp}$  and SOp output lines.

**Caution.** Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and  $\overline{SCKp}$  pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**Remarks 1.** p: CSI number (p=00), m: Unit number (m=0), n: Channel number (n=0)

g: PIM, POM number (g=1)

**2.**  $f_{MCK}$ : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register (SMRmn). m: Unit number

n: Channel number (mn= 0))

(3) During communication at same potential (CSI mode) (Slave mode,  $\overline{\text{SCKp}}$ ...external clock input)

( $T_A = -20$  to  $+85$  ° C,  $4.0 \text{ V} \leq \text{VCC} \leq 28 \text{ V}$ ,  $\text{VREG2} = 3.3 \text{ V}$ ,  $\text{GND0} = \text{GND1} = 0 \text{ V}$ )

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SCKp cycle time <sup>Note 4</sup>	$t_{\text{KCY2}}$	$16 \text{ MHz} < f_{\text{MCK}}$	$8/f_{\text{MCK}}$	-	-	ns
		$f_{\text{MCK}} \leq 16 \text{ MHz}$	$6/f_{\text{MCK}}$	-	-	ns
SCKp high-/low-level width	$t_{\text{KH2}}$ , $t_{\text{KL2}}$		$t_{\text{KCY2}}/2$	-	-	ns
Sip setup time (to $\overline{\text{SCKp}} \uparrow$ ) <sup>Note 1</sup>	$t_{\text{SIK2}}$		$1/f_{\text{MCK}} + 20$	-	-	ns
Sip hold time (to $\overline{\text{SCKp}} \uparrow$ ) <sup>Note 1</sup>	$t_{\text{KSI2}}$		$1/f_{\text{MCK}} + 31$	-	-	ns
Delay time from $\overline{\text{SCKp}} \downarrow$ to Sop output <sup>Note 2</sup>	$t_{\text{KSO2}}$	$C = 30 \text{ pF}$ <sup>Note 3</sup>	-	-	$2/f_{\text{MCK}} + 44$	ns

**Notes 1.** When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 0$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 1$ . The Sip setup time becomes “to  $\overline{\text{SCKp}} \downarrow$ ” when  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 1$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 0$ .

**2.** When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 0$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 1$ . The Sip hold time becomes “from  $\overline{\text{SCKp}} \uparrow$ ” when  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 1$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 0$ .

**3.** C is the load capacitance of the Sop output lines.

**Caution** Select the TTL input buffer for the Sip pin and  $\overline{\text{SCKp}}$  pin and the normal output mode for the Sip pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**Remarks 1.** p: CSI number (p=00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m=0, 1)

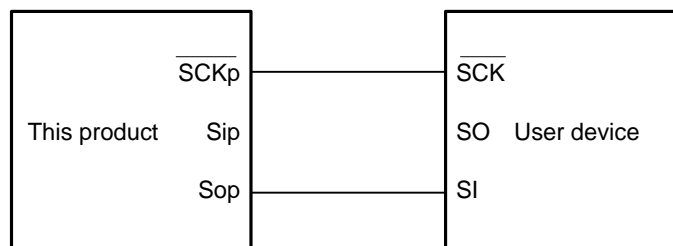
n: Channel number (n= 0 to 3), g: PIM, POM number (g=0, 1, 3 to 5, 14)

**2.**  $f_{\text{MCK}}$ : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register (SMRmn). m: Unit number

n: Channel number (mn= 00 to 03, 10 to 13))

CSI mode connection diagram (During communication at same potential)

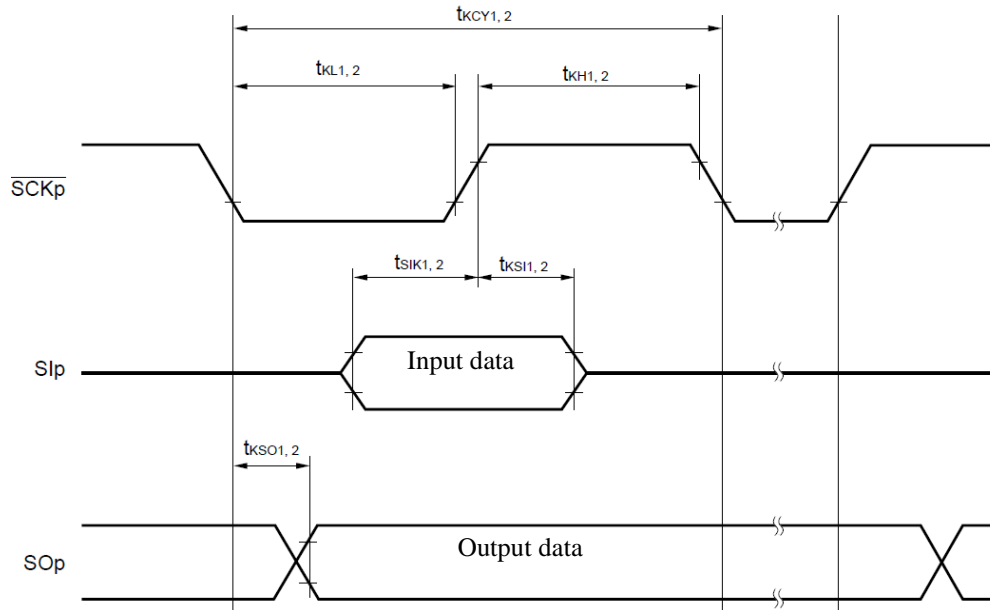


**Remarks 1.** P: CSI number (p=00, 01, 10, 11, 20, 21, 30, 31)

**2.** m: Unit number, n: channel number (mn= 00 to 03, 10 to 13)

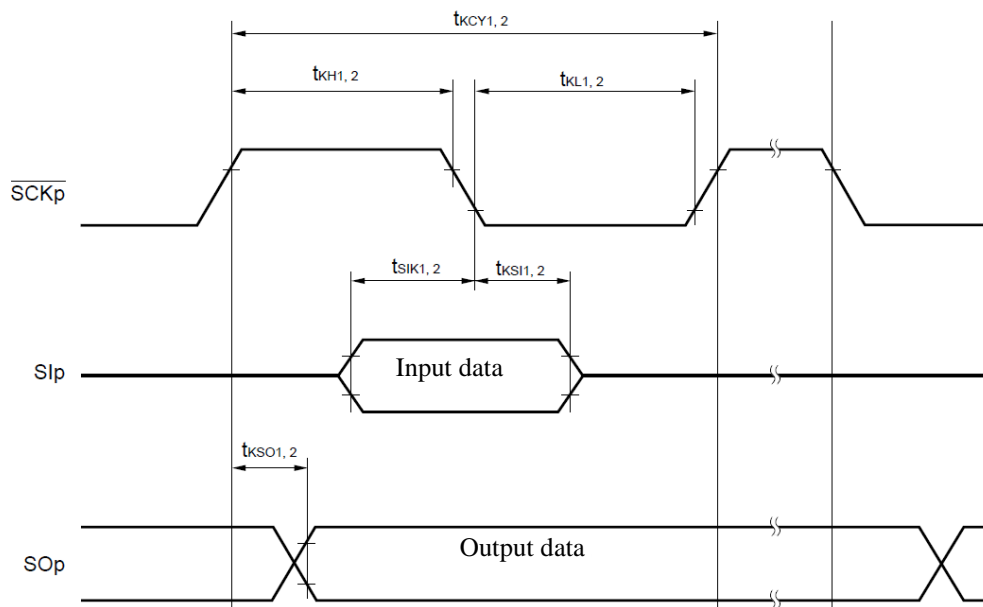
CSI mode serial transmission timing (During communication at same potential)

(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



CSI mode serial transmission timing (During communication at same potential)

(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



**Remarks 1.** p:CSI number (p=00, 01, 10, 11, 20, 21, 30, 31)

**2.** m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

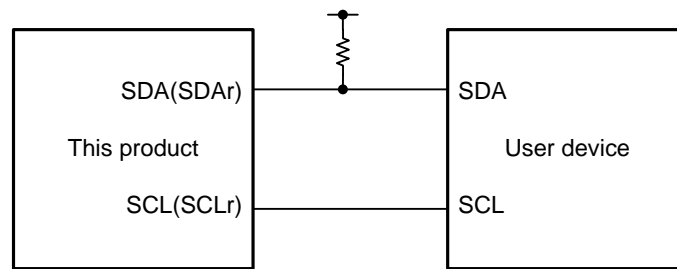
(4) During communication at same potential (simplified I<sup>2</sup>C mode)

(T<sub>A</sub> = -20 to +85 °C, 4.0 V ≤ V<sub>CC</sub> ≤ 28 V, V<sub>REG2</sub> = 3.3 V, GND<sub>0</sub> = GND<sub>1</sub> = 0 V)

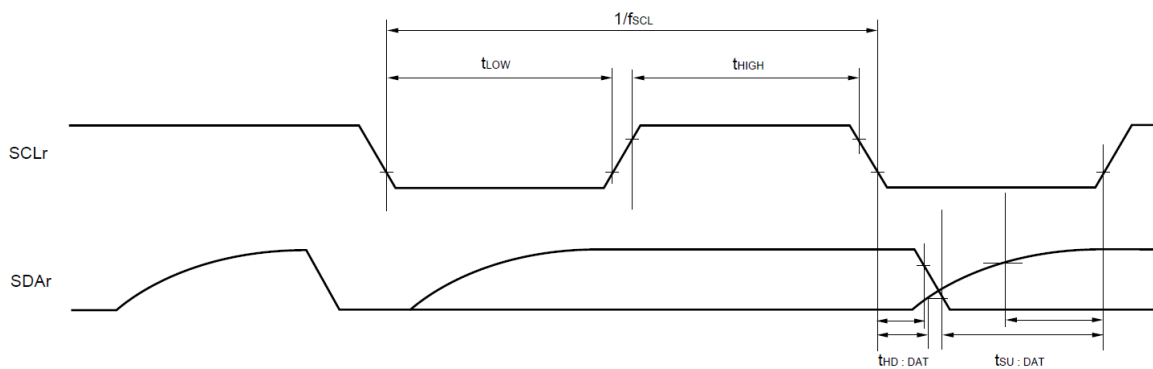
Item	Symbol	Condition	MIN.	MAX.	Unit
SCLr clock frequency	f <sub>SCL</sub>	C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	-	1000	kHz
Hold time when SCLr = "L"	t <sub>LOW</sub>	C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	475	-	ns
Hold time when SCLr = "H"	t <sub>HIGH</sub>	C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	475	-	ns
Data setup time(reception)	t <sub>SU:DAT</sub>	C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	1/f <sub>MCK</sub> +85 <b>Note</b>	-	ns
Data hold time(transmission)	t <sub>HD:DAT</sub>	C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	0	305	ns

**Note** set the f<sub>MCK</sub> value to keep the hold time of SCLr = "L" and SCLr = "H".

Simplified I<sup>2</sup>C mode connection diagram (During communication at same potential)



Simplified I<sup>2</sup>C mode serial transmission timing (During communication at same potential)



**Caution** Select the TTL input buffer and the N-ch open drain output (VREG2 tolerance) mode for the SDAr pin and the N-ch open drain output (VREG2 tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

- Remarks 1.**  $R_b[\Omega]$ : Communication line (SDAr) pull-up resistance,  $C_b[F]$ : Communication line (SDAr, SCLr) load capacitance
2. r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 3 to 5, 14), h: POM number (h = 0, 1, 3 to 5, 7, 14)
  3.  $f_{MCK}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).  
m: Unit number(m = 0, 1), n: Channel number (n = 0, 2, mn = 00 to 03, 10 to 13))

(5) Communication at different potential (2.5 V, 3 V) (UART mode, CSI mode, simplified I<sup>2</sup>C mode)

The serial array unit of this product do not connect (communicate) the device at different potential. Connecting device is same potential to VREG2 (CREG2 pin) certainly.

### 3.5.2 Serial interface IICA

( $T_A = -20$  to  $+85$  °C,  $4.0 V \leq V_{CC} \leq 28 V$ ,  $V_{REG2} = 3.3 V$ ,  $GND0 = GND1 = 0 V$ )

Item	Symbol	Condition	Standard Mode		Fast Mode		Fast Mode Plus		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	fSCL	Fast mode plus : fCLK $\geq$ 10 MHz	-	-	-	-	0	1000	kHz
		Fast mode : fCLK $\geq$ 3.5 MHz	-	-	0	400	-	-	kHz
		Standard mode : fCLK $\geq$ 1 MHz	0	100	-	-	-	-	kHz
Setup time of restart condition Note 1	tSU: STA		4.7	-	0.6	-	0.26	-	$\mu$ s
Hold time	tHD: STA		4.0	-	0.6	-	0.26	-	$\mu$ s
Hold time when SCLA0 = "L"	tLOW		4.7	-	1.3	-	0.5	-	$\mu$ s
Hold time when SCLA0 = "H"	tHIGH		4.0	-	0.6	-	0.26	-	$\mu$ s
Data setup time(reception)	tSU: DAT		250	-	100	-	50	-	ns
Data hold time(transmission) Note 2	tHD: DAT		0	3.45	0	0.9	0	-	$\mu$ s
Setup time of stop condition	tSU: STO		4.0	-	0.6	-	0.26	-	$\mu$ s
Bus-free time	tBMF		4.7	-	1.3	-	0.5	-	$\mu$ s

Notes 1. The first clock pulse is generated after this period when start/restart condition is detected.

- The maximum value (MAX) of t<sub>HD: DAT</sub> is during normal transfer and wait state is inserted in the  $\overline{ACK}$  (acknowledge) timing.

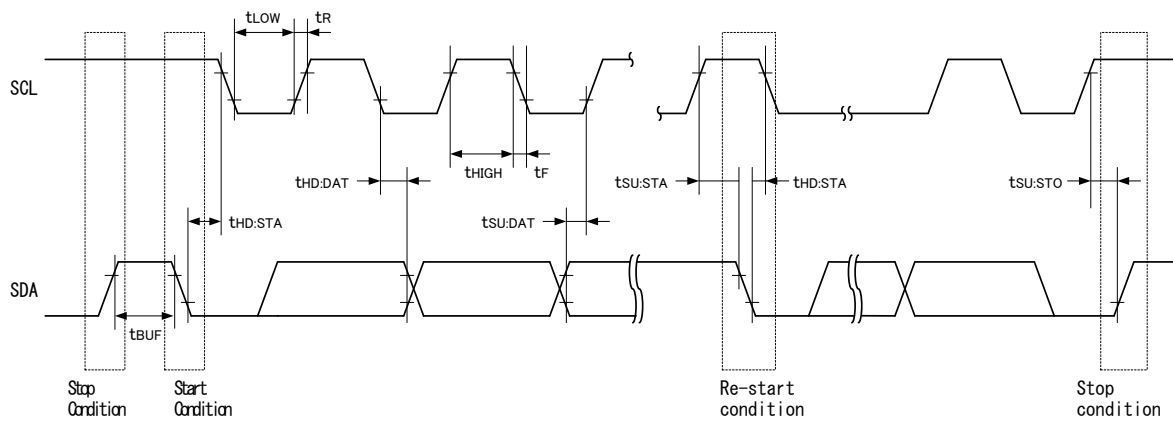
**Remark.** The maximum value of C<sub>b</sub> (communication line capacitance) and the value of R<sub>b</sub> (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C<sub>b</sub> = 400 pF, R<sub>b</sub> = 2.7 k $\Omega$

Fast mode: C<sub>b</sub> = 320 pF, R<sub>b</sub> = 1.1 k $\Omega$

Fast mode plus: C<sub>b</sub> = 120 pF, R<sub>b</sub> = 1.1 k $\Omega$

### IICA serial transfer timing





### 3.5.3 On-chip debug (UART)

( $T_A = -20$  to  $+85$  ° C,  $4.0\text{ V} \leq V_{CC} \leq 28\text{ V}$ ,  $V_{REG2} = 3.3\text{ V}$ ,  $GND0 = GND1 = 0\text{ V}$ )

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transmission rate			115.2 k	-	1 M	bps

### 3.5.4 Interrupt

( $T_A = -20$  to  $+85$  ° C,  $4.0\text{ V} \leq V_{CC} \leq 28\text{ V}$ ,  $V_{REG2} = 3.3\text{ V}$ ,  $GND0 = GND1 = 0\text{ V}$ )

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Interrupt input high-level width	$t_{INTH}$	INTP0, INTP5	1	-	-	$\mu\text{s}$
,low-level width	$t_{INTL}$					

## 3.6 Analog front end characteristics

### 3.6.1 A/D converter characteristics

( $T_A = -20$  to  $+85$  ° C,  $4.0\text{ V} \leq V_{CC} \leq 28\text{ V}$ ,  $V_{REG2} = 3.3\text{ V}$ ,  $V_{REG1} = 1.8\text{ V}$ ,  $GND0 = GND1 = 0\text{ V}$ )

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution	-		-	15	-	bit
Input voltage range	-		0	-	VREG1	V
Integral non-linearity error	-		-	-	±16	LSB
Conversion result(zero input) Note	-	VI=GND0	-	3266	-	LSB
Temperature dependency (zero input)	-	VI=GND0	-0.24	-	+0.24	LSB/° C
Conversion result (full-scale input) Note	-	VI= VREG1	-	29453	-	LSB
Temperature dependency (full-scale input)	-	VI= VREG1	-0.24	-	+0.24	LSB/° C
AN port input current	II (AD)		-	2.0	-	µA

**Note.** This value of A/D conversion result is a decimal value.

### 3.6.2 Current integrating circuit characteristics

( $T_A = -20$  to  $+85$  ° C,  $4.0\text{ V} \leq V_{CC} \leq 28\text{ V}$ ,  $V_{REG2} = 3.3\text{ V}$ ,  $GND0 = GND1 = 0\text{ V}$ )

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution	-		-	18	-	bit
Input voltage range	-	ISENS1-ISENS0 Sensing resistor: 5 mΩ	-0.1	-	0.1	V
Conversion time	-	f1=4,194,304 Hz	-	(250)	-	ms
Integral non-linearity error	-		-	-	0.02	%FSR
ISENS0, ISENS1 Input current	II (CC)		-	0.2	-	µA

**Remark.** The parenthetical values are for reference.

### 3.6.3 Overcurrent detection circuit characteristics

( $T_A = -20$  to  $+85$  ° C,  $4.0 \text{ V} \leq V_{CC} \leq 28 \text{ V}$ ,  $V_{REG2} = 3.3 \text{ V}$ ,  $GND0 = GND1 = 0 \text{ V}$ )

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Discharge short-circuit current 1 detection voltage error	-		-	-	±50	mV
Discharge short-circuit current 2 detection voltage error	-	25 mV to 100 mV setting	-	-	±12.5	mV
		125 mV to 250 mV setting	-	-	±25	mV
Discharge overcurrent detection voltage error	-	25 mV to 50mV setting	-	-	±10	mV
		55 mV to 100 mV setting	-	-	±25	mV
Charge overcurrent detection voltage error	-	-25 mV to -100 mV setting	-	-	±10	mV
		-125 mV to -250 mVsetting	-	-	±25	mV
Wakeup current detection voltage error <sup>Note1,Note2</sup>	-	Discharge side, 10 times mode ± 1A detection sense resistance 5mΩ	4.0	5.0	6.0	mV
Turbo boost current detection error <sup>Note2</sup>	-	10 times mode ± 1A detection sense resistance 5mΩ	4.0	5.0	6.0	mV
Discharge short-circuit current 1 detection time error	-		0	-	30.5	μs
Discharge short-circuit current 2 detection time error	-		0	-	30.5	μs
Discharge overcurrent detection time error	-		0	-	30.5	μs
Charge overcurrent detection time error	-		0	-	30.5	μs
Wakeup current detection time Error <sup>Note</sup>	-		58.6	-	62.5	ms

**Note1.** It is applied both to Charge wakeup detection and Discharge wakeup detection.

**Note2.** The error in the case where the calibration at each temperature. It does not include the error due to the temperature characteristics of the detection circuit.

### 3.6.4 Series regulator circuit characteristics

( $T_A = 25\text{ }^\circ\text{C}$  ,  $V_{CC} = 14\text{ V}$  ,  $GND0 = GND1 = 0\text{ V}$ )

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage	Vreg2o	$V_{CC}=14\text{ V}$ , $I_o=50\text{ }\mu\text{A}$ , after trimming	-	(3.3)	-	V
Drive current	VR2d	$V_{CC}=V_{IN5}\geq 4.0\text{ V}$ , $V_{REG2}\geq 3.0\text{ V}$	20	-	-	mA
Output voltage(VREG1)	Vreg1o	$V_{CC}=14\text{ V}$ , $I_o=10\text{ }\mu\text{A}$ , after trimming	1.755	-	1.845	V

**Note.** The sum of the I/O port High-level output current of the MCU of the operating current must be less than the drive current capability.

**Remark.** The parenthetical value is for reference.

### 3.6.5 Battery voltage detection circuit characteristics

( $T_A = 25\text{ }^\circ\text{C}$  ,  $V_{CC} = 14\text{ V}$  ,  $GND0 = GND1 = 0\text{ V}$ )

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Offset voltage	Voff	$V_{CC}=V_{IN5}\geq 2.0\text{ V}$ x (number of Battery cells)	-	(100)	-	mV
Voltage gain (VIN1 to 5)	Gamp1	$V_{CC}=V_{IN5}\geq 2.0\text{ V}$ x (number of Battery cells)	-	(0.28)	-	times
Voltage gain (VIN12)	Gamp2	$V_{CC}=V_{IN5}\geq 2.0\text{ V}$ x (number of Battery cells)	-	(0.06)	-	times
Maximum detection battery voltage (VIN1 to 5)	Vmo_max1		5.0	(6.0)	-	V
Maximum detection voltage (VIN12)	Vmo_max2		28.0	-	-	V
Input voltage	-	VIN5	0	-	28	V
	-	VIN4, VIN3, VIN2, VIN1	0	-	VIN5	V
	-	VIN5-VIN4, VIN4-VIN3, VIN3-VIN2, VIN2-VIN1, VIN1-GND	0	-	5	V
	-	VIN12	0	-	28	V

**Remark.** The parenthetical value is for reference.

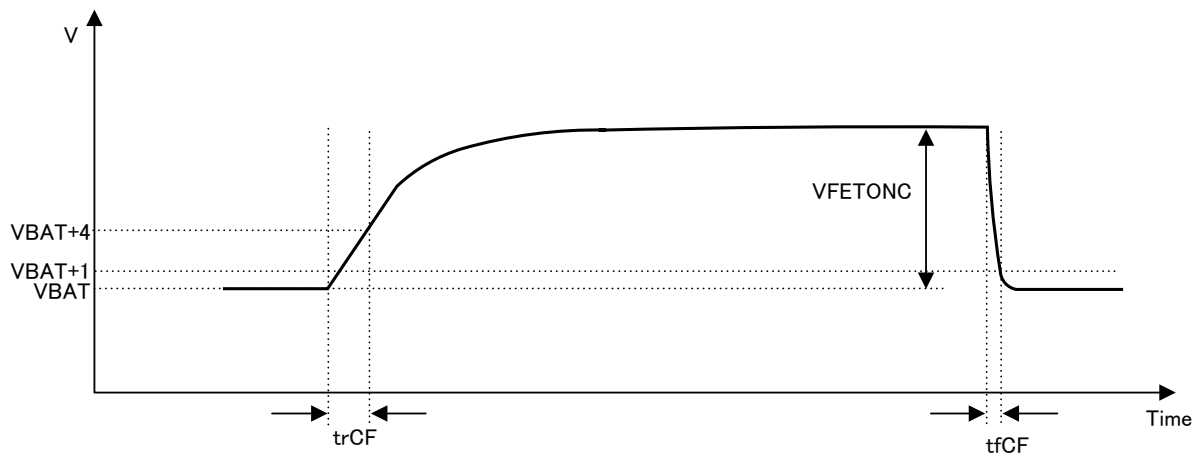
### 3.6.6 Charge/discharge FET control circuit characteristics

( $T_A = 25\text{ }^\circ\text{C}$  ,  $V_{CC} = 14\text{ V}$  ,  $GND0 = GND1 = 0\text{ V}$ )

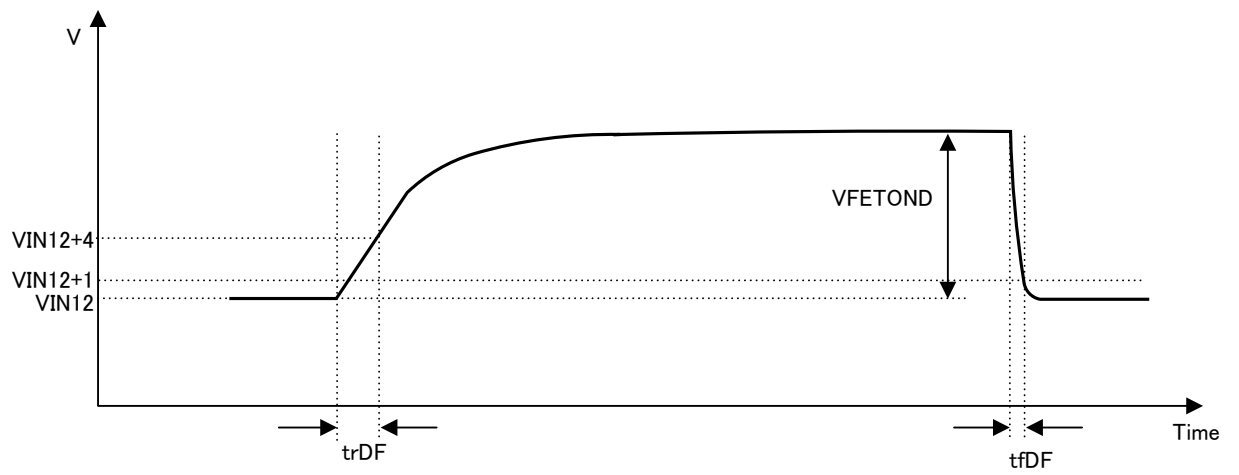
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CFOUT H output voltage	VFETONC1	CFOUT-VBAT, $4.0\text{ V} \leq V_{CC} < 6.0\text{ V}$ , $R_L = 10\text{ M}\Omega$	4	(7)	12	V
	VFETONC2	CFOUT-VBAT, $6.0\text{ V} \leq V_{CC}$ , $R_L = 10\text{ M}\Omega$	9	(10)	12	V
CFOUT L output voltage	VFETOFFC	CFOUT-VBAT, $V_{BAT} = 14\text{ V}$ , $R_L = 10\text{ M}\Omega$	-	(0)	0.2	V
CFOUT control time	trCF1	Lo (VBAT) → Hi (VBAT+4 V), $C_L = 4700\text{ pF}$ , $4.0\text{ V} \leq V_{CC} < 6.0\text{ V}$	-	(1000)	3000	$\mu\text{s}$
	trCF2	Lo (VBAT) → Hi (VBAT+4 V), $C_L = 4700\text{ pF}$ , $6.0\text{ V} \leq V_{CC}$	-	(200)	600	$\mu\text{s}$
	tfCF	Hi (VBAT+4 V) → Lo (VBAT+1 V), $C_L = 4700\text{ pF}$	-	(80)	200	$\mu\text{s}$
DFOUT H output voltage	VFETOND1	DFOUT-VIN12, $4.0\text{ V} \leq V_{CC} < 6.0\text{ V}$ , $R_L = 10\text{ M}\Omega$	4	(7)	12	V
	VFETOND2	DFOUT-VIN12, $6.0\text{ V} \leq V_{CC}$ , $R_L = 10\text{ M}\Omega$	9	(10)	12	V
DFOUT L output voltage	VFETOFFD	DFOUT-VIN12, $V_{IN12} = 14\text{ V}$ , $R_L = 10\text{ M}\Omega$	-	(0)	0.2	V
DFOUT control time	trDF1	Lo (VIN12) → Hi (VIN12+4 V), $C_L = 4700\text{ pF}$ , $4.0\text{ V} \leq V_{CC} < 6.0\text{ V}$	-	(1000)	3000	$\mu\text{s}$
	trDF2	Lo (VIN12) → Hi (VIN12+4 V), $C_L = 4700\text{ pF}$ , $6.0\text{ V} \leq V_{CC}$	-	(200)	600	$\mu\text{s}$
	tfDF	Hi (VIN12+4 V) → Lo (VIN12), $C_L = 4700\text{ pF}$ External constant of VIN12: $C = 0.01\text{ }\mu\text{F}$ , $R = 10\text{ k}\Omega$	-	(250)	400	$\mu\text{s}$

**Remark.** The parenthetical value is for reference.

CFOUT output timing characteristic



DFOUT output timing characteristic



### 3.6.7 Conditioning circuit characteristics

( $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{CC} = 14\text{ V}$ ,  $GND0 = GND1 = 0\text{ V}$ )

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
1cell ON resistance	RON1	VCC=VBAT=VIN5=17.5 V, VIN4=14V, VIN3=10.5 V, VIN2=7 V, VIN1=3.5 V 1cell conditioning SW: ON	-	(500)	-	$\Omega$
2cell ON resistance	RON2	VCC=VBAT= VIN5=17.5 V, VIN4=14V, VIN3=10.5 V, VIN2=7 V, VIN1=3.5 V 2cell conditioning SW: ON	-	(500)	-	$\Omega$
3cell ON resistance	RON3	VCC=VBAT= VIN5=17.5 V, VIN4=14V, VIN3=10.5 V, VIN2=7 V, VIN1=3.5 V 3cell conditioning SW: ON	-	(500)	-	$\Omega$
4cell ON resistance	RON4	VCC=VBAT= VIN5=17.5 V, VIN4=14V, VIN3=10.5 V, VIN2=7 V, VIN1=3.5 V 4cell conditioning SW: ON	-	(500)	-	$\Omega$
5cell ON resistance	RON5	VCC=VBAT= VIN5=17.5 V, VIN4=14V, VIN3=10.5 V, VIN2=7 V, VIN1=3.5 V 4cell conditioning SW: ON	-	(500)	-	$\Omega$

**Remark.** The parenthetical value is for reference.

### 3.7 Flash memory programming characteristics

( $T_A = -20\text{ to }+85\text{ }^\circ\text{C}$ ,  $4.0\text{ V} \leq V_{CC} \leq 28\text{ V}$ ,  $V_{REG2} = 3.3\text{ V}$ ,  $GND0 = GND1 = 0\text{ V}$ )

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit	
Number of code flash rewrites <sup>Note1,2,3</sup>	Cerwrr	Retained for 20 years	$T_a=85\text{ }^\circ\text{C}$	1,000	-	-	times
Number of data flash rewrites <sup>Note1,2,3</sup>		Retained for 1 years	$T_a=25\text{ }^\circ\text{C}$	-	1,000,000	-	
		Retained for 5 years	$T_a=85\text{ }^\circ\text{C}$	100,000			
		Retained for 20 years	$T_a=85\text{ }^\circ\text{C}$	10,000	-	-	

**Note1.** 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until rewrite after the rewrite.

**Note2.** When using flash memory programmer and Renesas Electronics self programming library.

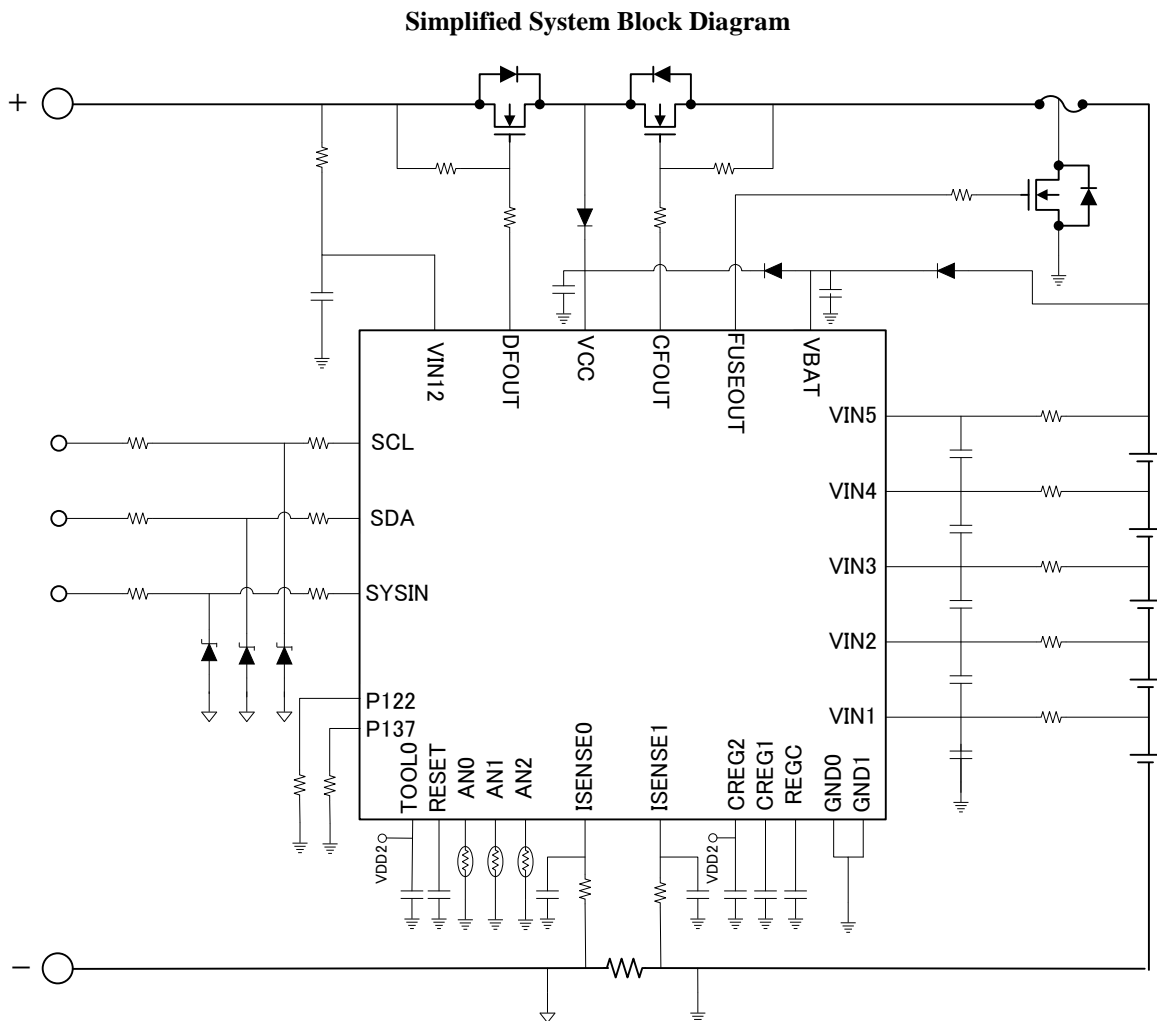
**Note3.** The one that shows the characteristics of the flash memory, this characteristic is the result of the reliability test.

## 4. Function Description

### 4.1 Overview

RAJ240080 is Renesas Battery Management IC which incorporates advanced battery fuel gauge features such as primary and secondary protection, voltage and current measurement, current integration, host communication interface and etc. RAJ240080 product consists of MCU block and AFE block in a single package and accomplish redundant protection mechanism by independent two blocks. Fuel gauge control firmware and data are stored in embedded flash memory and controls embedded analog and digital hardware circuits to achieve optimum battery management operation including high accuracy remaining capacity estimation and battery safety.

### 4.2 System block diagram

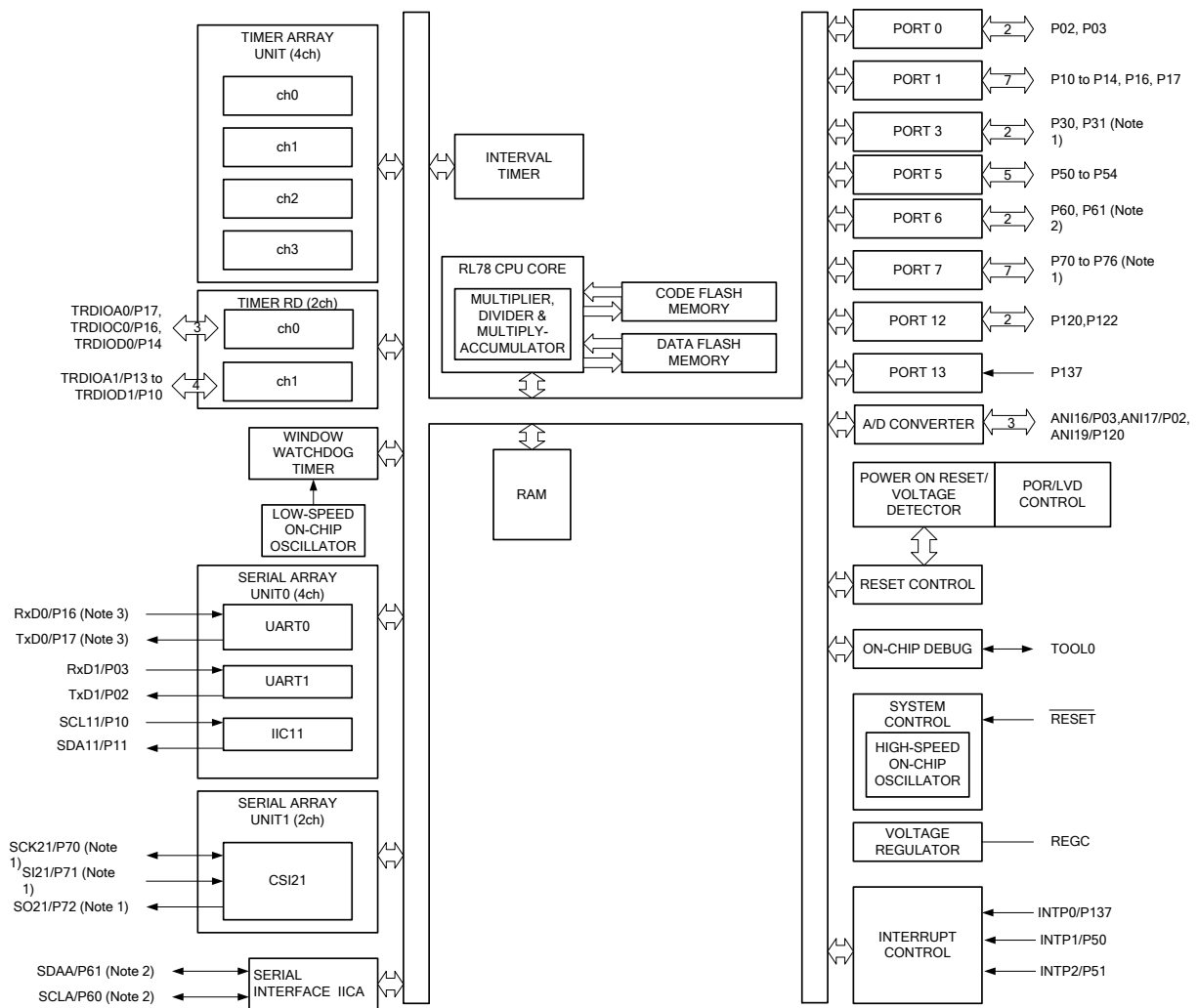


**Note** This example of a peripheral circuit does not guarantee the operation of this IC. Evaluate the operation adequately with actual applications, and then determine the circuits and constants.



### 4.3 MCU Block Diagram

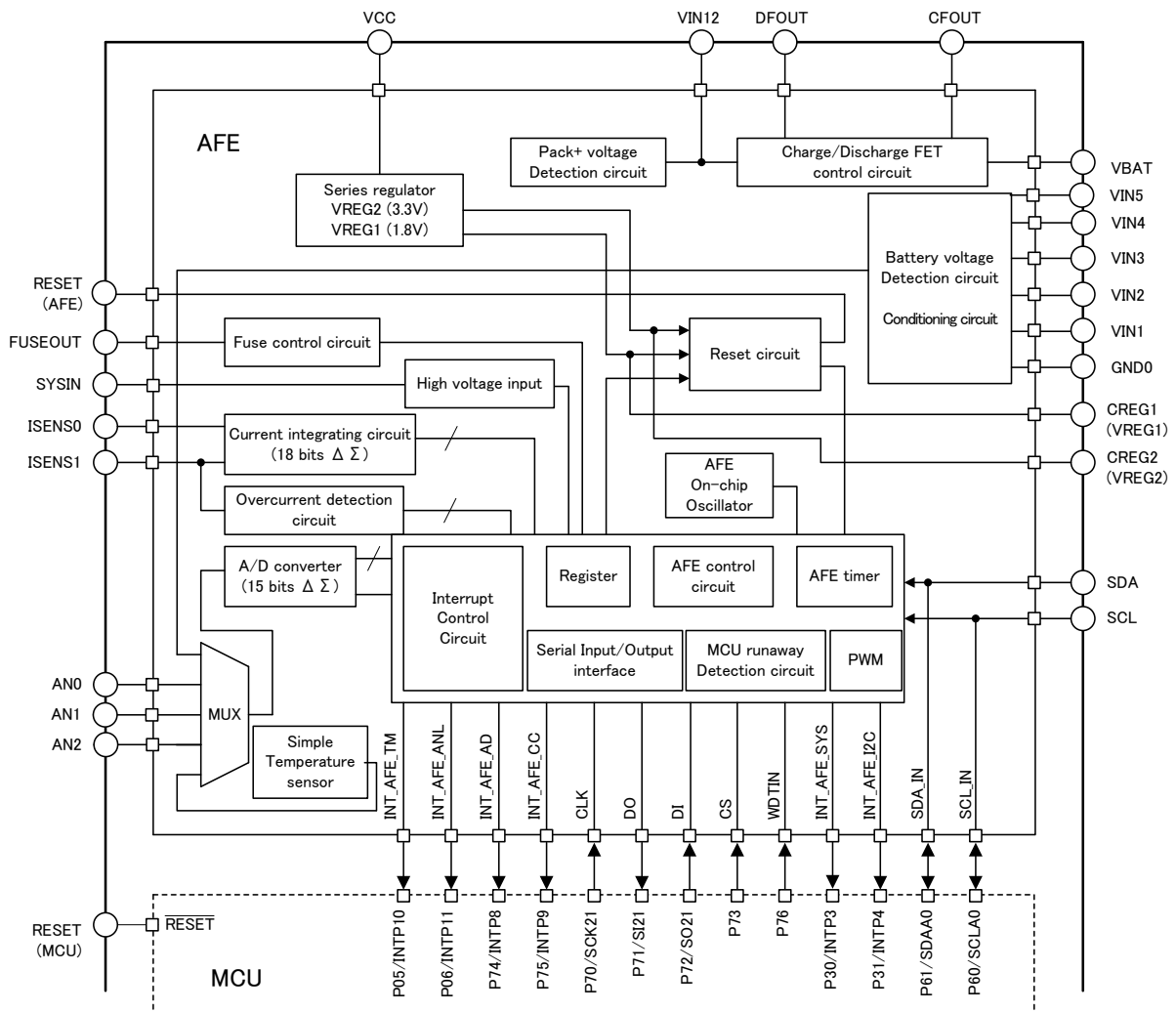
MCU Internal Block Diagram



- Notes 1. P30,P31,P70 to P76 are connected to AFE chip in the package.And do not connected to any pin.  
 2. P60/SDAA0 is connected to SDA pin and P61/SCLA0 is connected to SCL pin respectively.  
 3. Each interrupt request of AFE are assigned P05/INTP10,P06/INTP11. To use external interrupt function of P05,P06(INTP10,INTP11),it set the PIOR01 bit in the PIOR0 register to 1 and it's enabled peripheral I/O re-direction function. When setting the PIOR01 bit to 1,P16,P17 can be used as UART function(RxD0,TxD0)

## 4.4 AFE Block Diagram

### AFE Internal Block Diagram



## 4.5 Feature List

Note following function overview is when setting peripheral I/O re-direction register 0 (PIOR0) to 02H” .

(1/2)

Item		Description
Code flash memory		64 KB
Data Flash memory		4 KB
RAM		5.5 KB
Main system clock	High speed on-chip Oscillator clock(fIH)	High speed operation:1 to 32 MHz Low speed operation:1 to 8 MHz
Low speed on-chip oscillator clock		15 kHz (TYP.)
General purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
minimum instruction execution time		0.03125 μs(Internal high speed oscillation clock: fIH = 32 MHz)
Instruction set		<ul style="list-style-type: none"> <li>• data transmission (8/16 bits)</li> <li>• Addition and subtraction/logical operations (8/16 bits)</li> <li>• Multiplication (8×8 bits, 16×16 bits), Division (16÷16 bits, 32÷32 bits)</li> <li>• Rotate, barrel shift, bit manipulation (set, reset, test, Boolean operation) etc</li> </ul>
I/O Port	CMOS input/output	16
	CMOS input	2
	I <sup>2</sup> C bus input/output	2
	High voltage port	Output only: 1 Input only: 1
Timer	16 bits timer	5 channels (TAU: 4 channels, Timer RD:2 channel)
	Watchdog timer	1 channel
	12 bits interval timer	1 channel
Serial interface		<ul style="list-style-type: none"> <li>• UART: 2 channel</li> <li>• CSI: 1 channel/simple I<sup>2</sup>C:1 channel</li> <li>• CSI: 1 channel</li> </ul>
	I <sup>2</sup> C bus	1 channel
Vector interrupt source	Internal	10
	External	9 (6 sources is connected to AFE in the chip)
Reset		<ul style="list-style-type: none"> <li>• reset by RESET pin (reset circuit output of AFE, connect to RESETOUT)</li> <li>• internal reset by watchdog timer</li> <li>• internal reset by illegal instruction execution <sup>Note 1</sup></li> <li>• internal reset by RAM parity error</li> <li>• internal reset by illegal memory access</li> </ul>
On-chip debug function		Support

**Note 1:** It occurs when executes instruction code of “FFH”.

Reset by illegal instruction execution is not occurred emulation by on-chip debug emulator.

Item	Description
PWM	8 bits×1
A/D converter	15-bit resolution ( $\Delta\Sigma$ method) ×2 channels + internal 5 channels
Current integrating circuit	1 channel:18 bits resolution
Current integrating circuit for impedance measurement	1 channel:11 bits resolution
Overcurrent detection circuit	discharge short-circuit current detection 1, discharge short-circuit current detection 2, discharge overcurrent detection, charge overcurrent detection, wake-up current detection (discharge, charge),turbo boost current detection
Simple temperature sensor	1 channel
Charge/Discharge FET control circuit	N-ch FET driver for charge control N-ch FET driver for discharge control
Battery voltage detection circuit	Battery voltage gain: 0.28 times Offset voltage: 0.1 V
Pack+ voltage detection circuit	Battery Pack+ pin monitor gain:0.06 times
Fuse control circuit	Fuse control function
Series regulator <sup>Note1</sup>	VREG2:power supply for MCU (3.3 V)
High accuracy Power supply	VREG1(CREG1 pin):A/D converter, current integrating circuit (1.8 V)
Reset circuit	Series regulator output monitoring (VREG1, VREG2)
Conditioning circuit	5 cell support (On-resistor:500Ω)
MCU runaway detection circuit	20 bits×1(2 / 4 / 8 [s] to be selected)
On-chip oscillator <sup>Note2</sup>	4.194 MHz (TYP.)
AFE timer	2 channels AFE timer A(setting range:125 ms to 64 s) AFE timer B(setting range:30.52 us to 125 ms)
Serial input/output interface	Communication between AFE and MCU (4-wire)
Power supply voltage	VCC=4.0 to 28 V
Operation ambient temperature	-20 to 85 [°C]
Package	48 pin QFP

**Note1.** Series regulator stabilization time is 10ms after AFE power on.

**Note2.** 2ms wait is need for stabilization after On-chip oscillator is started.

## 4.6 Feature Description

### 4.6.1 ADC Circuit

15-bit delta-sigma ADC is implemented to measure instantaneous analog signal levels, such as voltage, current, temperature and etc. The multiplexer selects one of 8 channels to measure each signal. Appropriate channel of the multiplexer must be selected to measure desirable analog signal. ADC conversion results are stored in A/D data registers after the conversion.

ADC circuit block has a feature to execute multiple ADC conversions automatically. The multiplexer selects designated channel and ADC conversions are executed as specified in ADC automatic mode control register. An interrupt is asserted upon ADC conversion and the conversion result is stored in A/D data registers periodically.

Impedance measurement mode for Turbo-boost is an optional feature to measure voltage and current simultaneously. This optional feature was designed to measure battery impedance upon Turbo-boost operation and to calculate available maximum power.

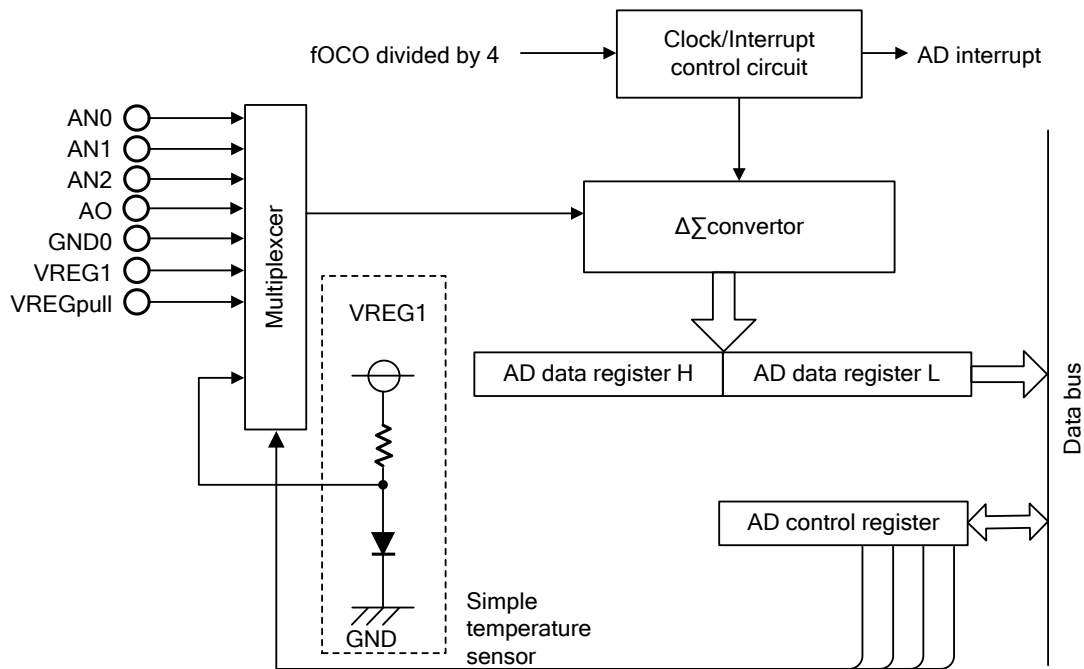
Table 4-1 A/D converter performance shows A/D converter performance, Figure 4-1 Block Diagram of A/D Converter shows Block Diagram of A/D Converter.

**Table 4-1 A/D converter performance**

Item	Performance
A/D conversion method	$\Delta\Sigma$ conversion
Analog input voltage	0 V to VREG1
Operating clock $\phi_{AD}$	fOCO divided by 4: 1.048576 MHz (fOCO=AFE on-chip oscillator)
Resolution	15 bits
Conversion accuracy	Integral non-linearity error : $\pm 16$ LSB
Analog input channel	AN0, AN1, AN2 Battery voltage detection circuit output (AO) Simple temperature sensor VREG1, VREGpull, GND
A/D conversion start condition	Software trigger
Conversion rate per pin	1024 $\phi_{AD}$ cycles: 1 ms mode <sup>Note</sup> 2048 $\phi_{AD}$ cycles: 2 ms mode <sup>Note</sup> 4096 $\phi_{AD}$ cycles: 4 ms mode <sup>Note</sup> 8192 $\phi_{AD}$ cycles: 8 ms mode <sup>Note</sup>

**Note** One of the modes is selected by the bits ADTIME0 to ADTIME1 in the ADCON1 register.

**Figure 4-1 Block Diagram of A/D Converter**



GND0 GND  
 VREG1 High accuracy internal power supply for A/D 1.8V Equivalent to CREG1 terminal output voltage  
 AO Output of Battery voltage detection circuit

Dedicated multiplexer provides 8 channels for A/D conversion to measure signal voltage level. Select “battery voltage detect circuit output (AO)” and configure battery voltage detection circuit of AFE to measure battery voltage levels. A/D converter multiplexer selection and conversion period can be configured in following registers.

**AD control register (ADCON)**

This register can control A/D converter operation enable, A/D conversion start, current integrating for impedance measurement operation enable and also can select a channel of AD conversion.

ADCON register can access by sending or receiving serial data to serial input-output interface using 3-wire serial I/O of MCU (CSI21). The register value is 00H by a reset signal from reset circuit

**Figure 4-2 AD control register (ADCON) format**

AFE address: 50H After Reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADCON	ADST	ADSLP	IMPST	0	ADSEL3	ADSEL2	ADSEL1	ADSEL0

ADSEL3	ADSEL 2	ADSEL 1	ADSEL 0	Select a channel of A/D conversion
0	0	0	0	AN0
0	0	0	1	AN1
0	0	1	0	AN2
0	0	1	1	Setting prohibited
0	1	0	0	Setting prohibited
0	1	0	1	Setting prohibited
0	1	1	0	Battery voltage detect circuit output (AO)
0	1	1	1	Sample temperature sensor

1	0	0	0	Setting prohibited
1	0	0	1	Setting prohibited
1	0	1	0	GND0 <sup>Note 2</sup>
1	0	1	1	CREG1 <sup>Note 3</sup>
1	1	0	0	Setting prohibited
1	1	0	1	VREG1_pull <sup>Note 4</sup>
1	1	1	0	Setting prohibited
1	1	1	1	Setting prohibited

IMPST	Current integrating for impedance measurement operation start control
0	Stop
1	Start

ADSLP	A/D conversion operation enable <sup>Note 5</sup>
0	Disable
1	Enable

ADST	A/D conversion operation control <sup>Notes 1, 5</sup>
0	Stop
1	Start

- Note 1.** This bit is automatically 0 after A/D conversion is completed. If repeat operation, set 1 to this bit after written 0.
- Note 2.** This one is used as reference GND (GND0 pin, 0 V) of A/D converter
- Note 3.** This one is used as reference internal power (CREG1 pin 1.8 V) of A/D converter
- Note 4.** This is used as internal power for thermistor pull-up resistor
- Note 5.** When ADSLP bit and ADST bit set 1 simultaneously AD conversion starts 60[us] later.

### AD control register 1 (ADCON1)

This register can select an A/D conversion time. And also can select current integrating circuit for impedance measurement conversion time at the same time.

ADCON1 register can access by sending or receiving serial data to serial input-output interface using 3-wire serial I/O of MCU (CSI21).

The register value is 00H by a reset signal from reset circuit

Figure 4-3 AD control register 1 (ADCON1) format

AFE address: 51H After Reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADCON1	0	0	0	0	0	0	ADTIME1	ADTIME0

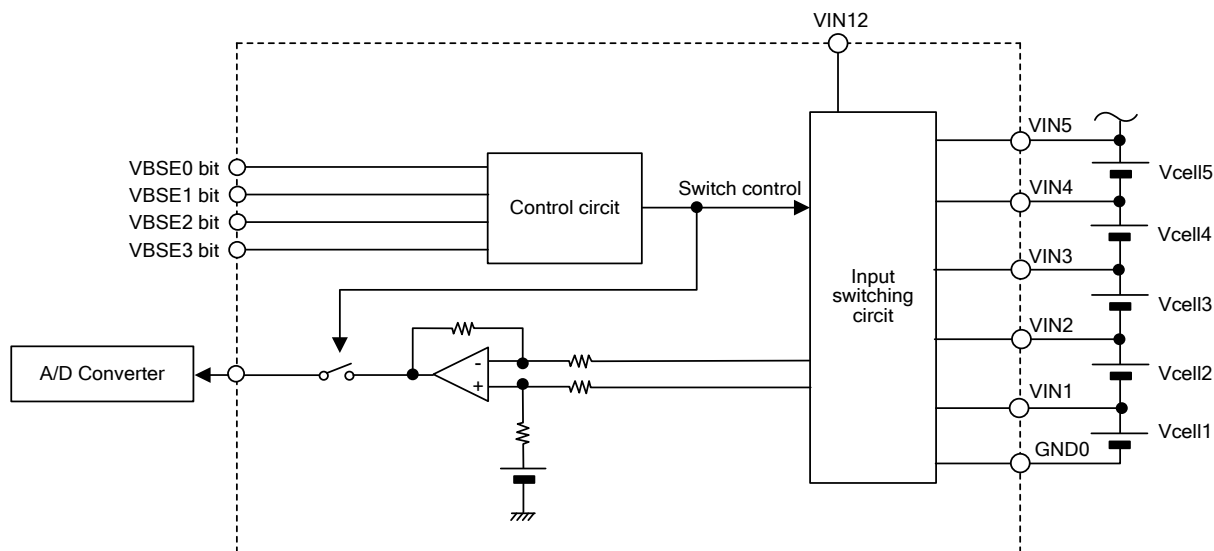
ADTIME1	ADTIME0	A/D conversion time
0	0	1 ms
0	1	2 ms
1	0	4 ms
1	1	8 ms

## 4.6.2 Battery Voltage detection circuit

The battery voltage detection circuit can detect the battery cell voltage and the voltage of the Pack + pin. Input signals can be selected by setting VBSE0 to VBSE3 bits in the VBSE register and are connected to A/D converter input. This signal can be measured an analog value attenuated by a predetermined gain using A/D converter by selecting “Battery voltage detect circuit output (AO)” A/D converter multiplexer.

Figure 4-4 Block Diagram of Battery Voltage detection circuit shows the Block Diagram of Battery Voltage detection circuit

Figure 4-4 Block Diagram of Battery Voltage detection circuit



### Analog output control Register (VBSE)

This register can be selected an analog output of battery voltage detection circuit that output to A/D converter.

VBSE register can access by sending or receiving serial data to serial input-output interface using 3-wire serial I/O of MCU (CSI21).

The register value is 00H by a reset signal from reset circuit.

Figure 4-5 Analog output control Register (VBSE) format

AFE address: 02H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
VBSE	0	0	0	0	VBSE3	VBSE 2	VBSE 1	VBSE 0

VBSE3	VBSE 2	VBSE 1	VBSE 0	Battery voltage detection circuit output
0	0	0	0	HiZ output
0	0	0	1	VBAT1 output
0	0	1	0	VBAT2 output
0	0	1	1	VBAT3 output
0	1	0	0	VBAT4 output
0	1	0	1	VBAT5 output
0	1	1	0	VBAT1 offset output
0	1	1	1	VBAT2 offset output
1	0	0	0	VBAT3 offset output
1	0	0	1	VBAT4 offset output



1	0	1	0	VBAT5 offset output
1	0	1	1	VIN12 voltage output
1	1	0	0	VIN12 voltage offset output
1	1	0	1	SMBus I/O mode 10 minutes timer history <sup>Note</sup>
1	1	1	0	Setting prohibited
1	1	1	1	Setting prohibited

**Note.** After SMBus I/O mode start up, if one of the command of the Flash write-erase and read isn't received and 10 minutes passed, AFE register of VBSE (02h bit3-0) is set to b1101 as a history of elapsed 10 minutes, software reset is done. History of the 10 minutes had elapsed can be seen from the user program. AFE register (VBSE: 02h bit3-0) is reset to the b0000 by AFE initialization. After referring to the history of the 10 minutes had elapsed, AFE register in the user program, it is need to initialize to (VBSE 02h bit3-0) the b0000. It is recommend to refer to the "RAJ240XXX flash memory SMBus input and output mode" for more information.

### 4.6.3 Current Integrating Circuit

The current integrating circuit measures the current flowing in a sense resistor by converting the potential difference across the terminals of the resistor connected between the ISENS1 and ISENS0 pins to a digital value. Analog signals are input from the ISENS1 and ISENS0 pins.

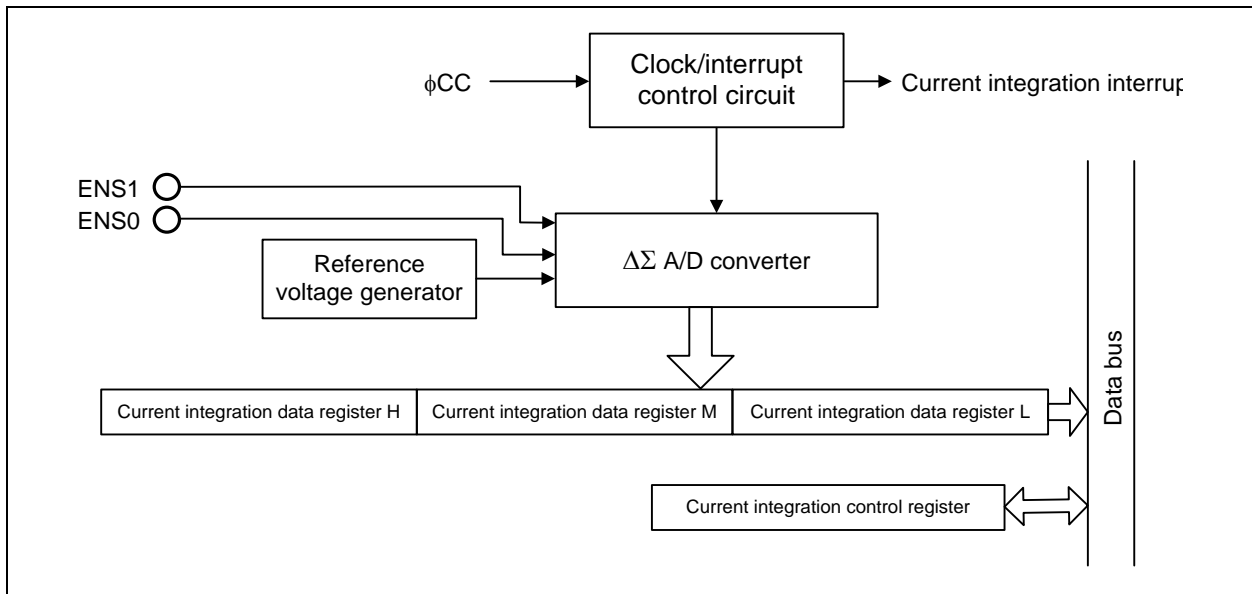
Table 4-2 Current integrating Circuit Performance list shows current integrating circuit performance.

Figure 4-6 Current integrating circuit block diagram shows current integrating circuit block diagram, Figure 4-7 Operation timing of Current integrating circuit shows operation timing of Current integrating circuit.

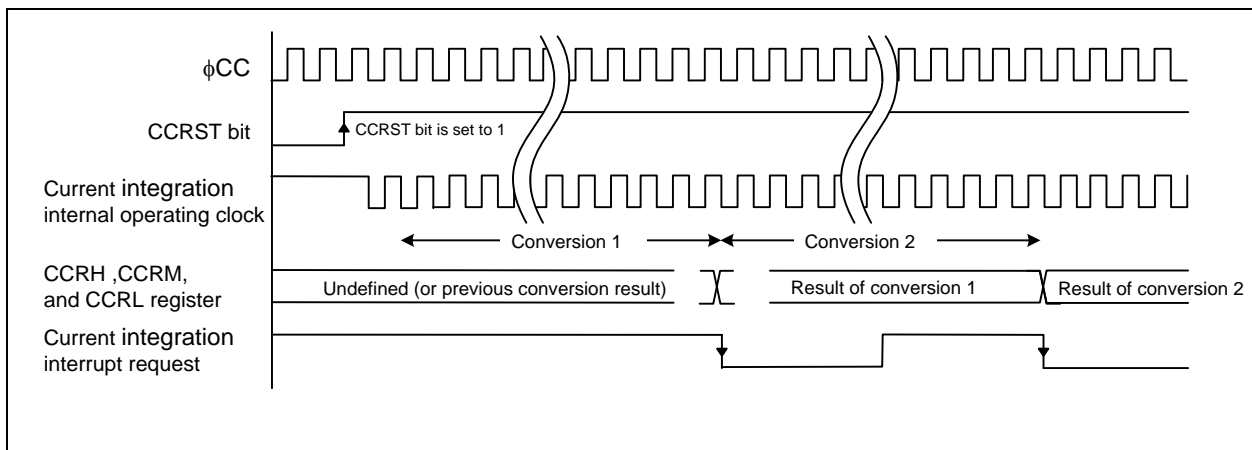
**Table 4-2 Current integrating Circuit Performance**

Item	Performance
Conversion method	$\Delta\Sigma$ conversion
Analog input voltage	-0.1 V to 0.1 V
Operating clock $\phi_{CC}$	fOCO divided by 32: 131.072 kHz (fOCO=AFE on-chip oscillator)
Resolution	18bit
Conversion accuracy	Integral non-linearity error: $\pm 0.02\%$ FSR
Analog input pin	Potential difference between ISENS1 and ISENS0 pins
Conversion time per cycle	250 ms (32,768 $\phi_{CC}$ cycle)

**Figure 4-6** Current integrating circuit block diagram



**Figure 4-7** Operation timing of Current integrating circuit



#### 4.6.4 Current Integration Circuit in Impedance Measurement Mode

The current integrating circuit for impedance measurement measures current of the sense resistor connected between the pins ISENS1 and ISENS0 by converting the voltage of that into digital values. This circuit can measure the impedance value because it can measure the current with the A/D converter synchronously. Analog signals are input from the ISENS1 and ISENS0 pins.

Table 4-3 Current integrating Circuit for impedance Measurement Performance shows Current integrating Circuit for impedance Measurement Performance,

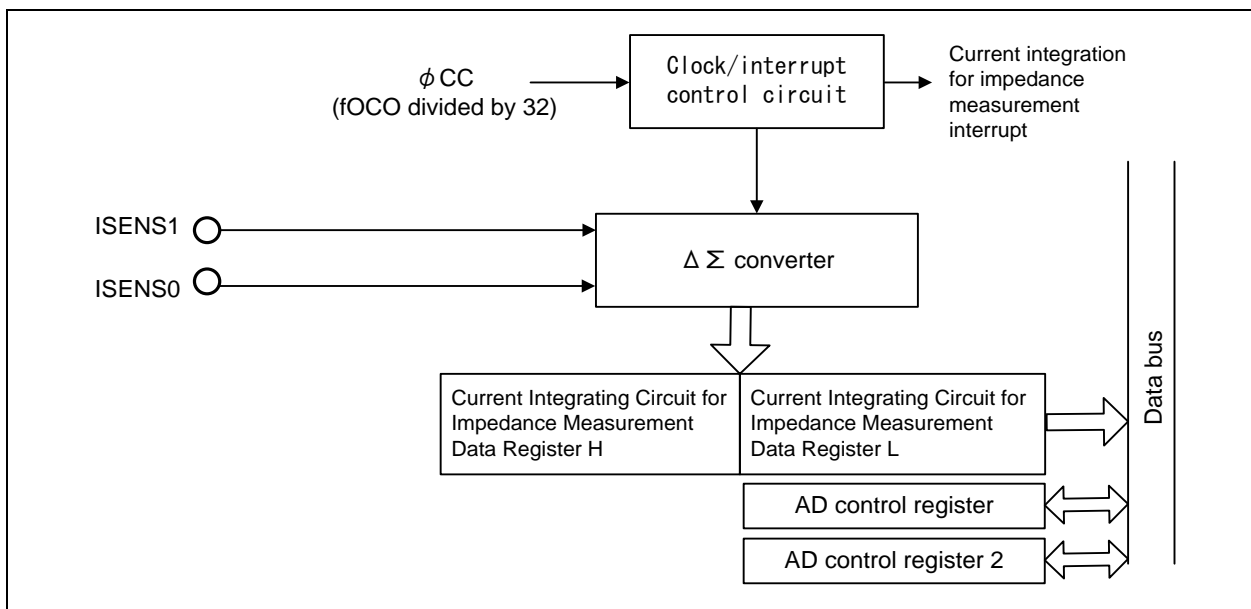
Figure 4-8 Current integrating circuit for impedance measurement block diagram shows current integrating circuit for impedance measurement block diagram, Figure 4-9 Operation timing of current integrating circuit for impedance measurement shows operation timing of current integrating circuit for impedance measurement.

**Table 4-3** Current integrating Circuit for impedance Measurement Performance

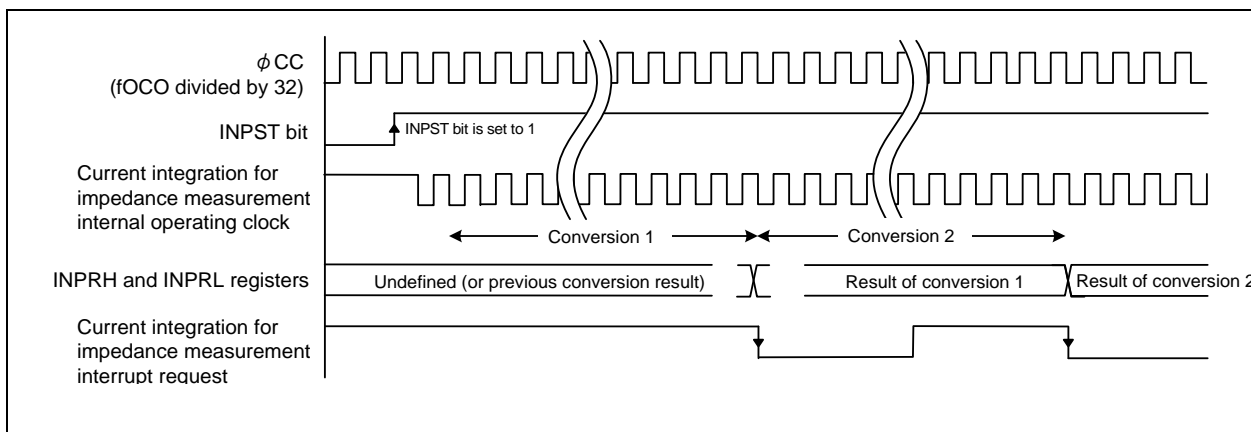
Item	Performance
Conversion method	$\Delta\Sigma$ conversion
Analog input voltage	-0.1 V to 0.1 V
Operating clock $\phi_{CC}$	fOCO divided by 32: 131.072 kHz (fOCO=AFE on-chip oscillator)
Resolution	Conversion time 1 ms(note 1): 7 bits Conversion time 2 ms(note 1): 8 bits Conversion time 4 ms(note 1): 9 bits Conversion time 8 ms(note 1): 10 bits
Analog input pin	Potential difference between ISENS1 and ISENS0 pins
Conversion time per cycle (note 1) <sup>Note</sup>	1 ms, 2 ms, 4 ms, 8 ms

**Note** The conversion time varies with the setting of the ADTIME1 bit and the ADTIME0 bit in the ADCON1 register.

**Figure 4-8** Current integrating circuit for impedance measurement block diagram



**Figure 4-9** Operation timing of current integrating circuit for impedance measurement



#### 4.6.5 FET control circuit

The FET control circuit has two on-chip voltage step-up circuits, so that products are able to control N-ch FETs as switches to control charging and discharging.

##### FET ON/OFF control

It can control the ON/OFF of charge FET, discharge FET by setting the FETC bit, FETD bit in the FCON register to 1.

##### Forced FET OFF Function

When the AFE identifies a short-circuit overcurrent, overcharge, or overdischarge state, It can turn off the FET forcibly.

Forced OFF Function of discharge FET is set the BCFETEN bit in the BCDCON register or the SCFETEN bit in the SCDCON register or the DOCFETEN bit in the DOCDCON register to 1 to enable a FET control.

Forced OFF function of charge FET is set the COCFETEN bit in the COCDCON register to 1 to enable a FET control.

The state of forced FET OFF function is judged by reading the AFECON3 register.

In discharge FET control, read the DFDATMON bit in the AFECON3 register, in charge FET control, read the CFDATMON bit in the AFECON3 register respectively.

When the DFDATMON bit is “1”, the DFOUT pin becomes VIN12 level.

When the CFDATMON bit is “1”, the CFOUT pin becomes VBAT level

When the forced FET OFF function is available (forced OFF) the FETC bit, FETD bit in the FCON register values are invalid, it enables the forced FET OFF function control.

Table 4-4 FCON register value and relationship of the FET forced OFF function and DFOUT/CFOUT pin control list shows the relations between FCON register value and FET forced OFF function and DFOUT/CFOUT pin control.

**Table 4-4 FCON register value and relationship of the FET forced OFF function and DFOUT/CFOUT pin control**

DFOUT control			CFOUT control		
DFDAT MON bit	FETD bit	DFOUT pin	CFDAT MON bit	FETC bit	CFOUT pin
0	0	OFF	0	0	OFF
0	1	ON	0	1	ON
1	0	VIN12 level	1	0	VBAT level
1	1		1	1	

Charge FET ON function when turbo boost current is detected

It is possible to forcibly do ON the charge FET that is OFF state when turbo boost current is detected. The charge FET forcibly ON function is enabled to set the TBCFETEN bit in the WUDCON2 register to 1

When turbo boost current detection is enabled.

#### 4.6.6 Overcurrent Detection Circuit

The overcurrent detection circuit detects overcurrent such as short-circuit current that flows through the detection.

Resistor connected between pins ISENS1 and ISENS0, and turns off the battery pack charge/discharge control FET to stop charging/discharging.

The overcurrent detection circuit incorporates discharge short-circuit current circuit 1, discharge short-circuit current circuit 2, discharge overcurrent circuit, and charge overcurrent circuit, for which detection voltage and detection time can be set independently.

In addition, the overcurrent detection circuit also incorporates a wakeup current detection circuit to generate an interrupt in case a current of 200 mA to 1 A flow through the detection resistor in power-down mode where the current integrating circuit is disabled when a battery is charging or discharging. Additionally, the overcurrent detection circuit also incorporates an automatically measurement function of cell voltage, a detection circuit has function that charge FET is ON.

Analog signals are input from the ISENS1 pin.

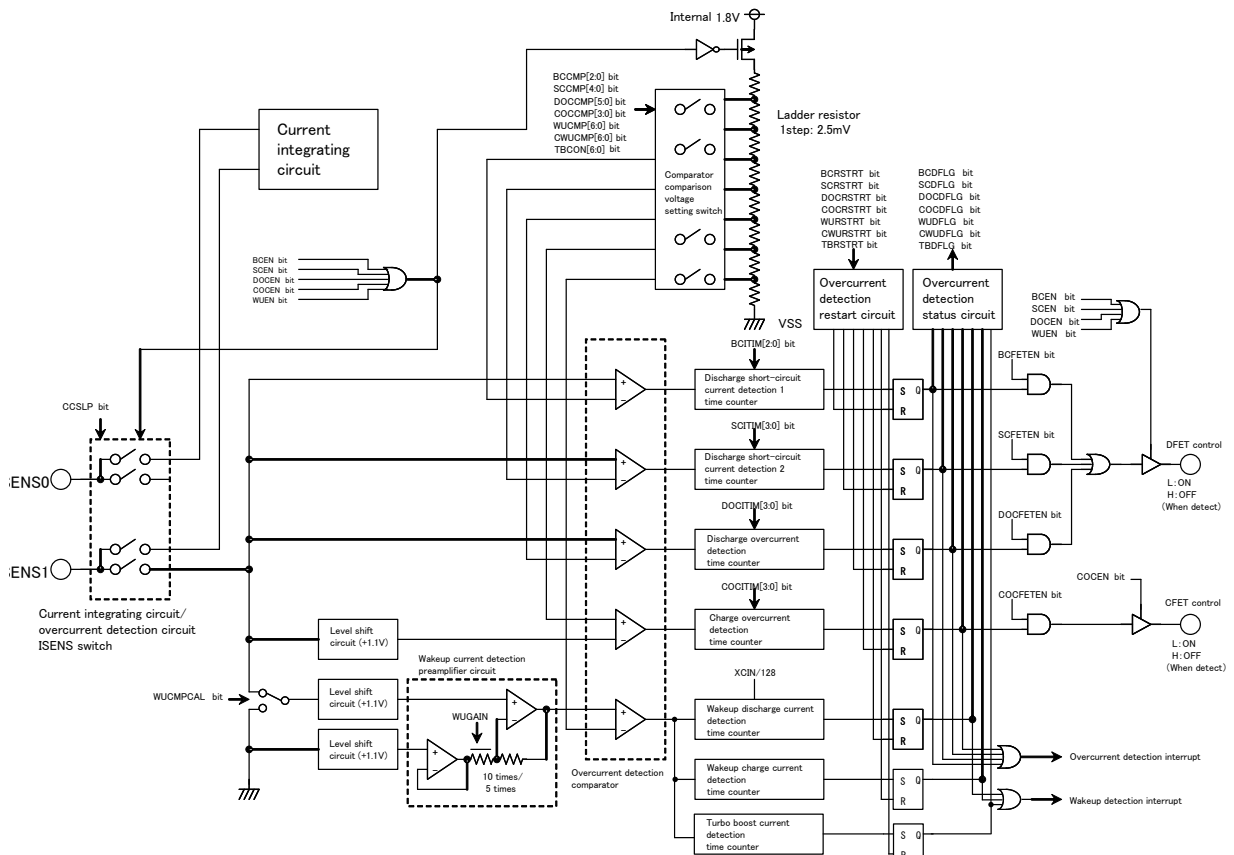
Table 4-5 Overcurrent Detection Circuit Performance list shows Overcurrent Detection Circuit Performance, Figure 4-10 Block Diagram of Overcurrent Detection Circuit shows Block Diagram of Overcurrent Detection Circuit.

**Table 4-5** Overcurrent Detection Circuit Performance

Item	Performance	
Analog input pin	ISENS1	
Operating clock	f32K (AFE on-chip oscillator divided by 128)	
Detection voltage Setting range (setting interval)	Discharge short-circuit current1	0.1 V to 0.8 V (0.1 V)
	Discharge short-circuit current 2	25 mV to 100 mV (12.5 mV)    setting range 1
		100 mV to 250 mV (25 mV)    setting range 2
	Discharge overcurrent	25 mV to 50 mV (2.5 mV)    setting range 1
		50 mV to 100 mV (5 mV)    setting range 2
	Charge overcurrent	-25 mV to -100 mV (12.5 mV)    setting range 1
-100 mV to -250 mV (25 mV)    setting range 2		
Wakeup current	-145 mV to 145 mV (2.5 mV)	
Turbo boost current	-145 mV to 145 mV (2.5 mV)	
Detection time Setting range (setting interval)	Discharge short-circuit current1	0 $\mu$ s to 427 $\mu$ s (61 $\mu$ s)
	Discharge short-circuit current 2	0 $\mu$ s to 915 $\mu$ s (61 $\mu$ s)
	Discharge overcurrent	0.916 ms to 30.212 ms (1.95 ms)
	Charge overcurrent	0 $\mu$ s to 915 $\mu$ s (61 $\mu$ s)
	Wakeup current	62.5 ms (It takes 244 $\mu$ s to perform calibration)
	Turbo boost current	488 $\mu$ s
Detection voltage error	Discharge short-circuit current1	$\pm$ 50 mV
	Discharge short-circuit current 2	$\pm$ 10 mV ( setting range 1) / $\pm$ 25 mv (setting range 2)
	Discharge, charge overcurrent	$\pm$ 10 mV (setting range 1) / $\pm$ 25 mv (setting range 2)
	Wakeup current	$\pm$ 20 %(10 times mode, sense resistor 5m $\Omega$ , $\pm$ 1A detection)
	Turbo boost current	$\pm$ 20 %(10 times mode, sense resistor 5m $\Omega$ , $\pm$ 1A detection)
Wakeup current detection circuit Input scaling factor	10 times, 5 times, 2 times	

**Caution.** If there is the same value in both setting range 1 and 2, setting range 1 is valid.

**Figure 4-10 Block Diagram of Overcurrent Detection Circuit**



**Remarks**  
 1. In order to output over-current detection interruption at the time of detection, be sure to set BCINTEN bit, SCINTEN bit, DOCINTEN bit, or COCINTEN bit to 1, and permit an interruption output.  
 2. In order to output the wake-up current detection interruption at the time of detection, be sure set WUINTEN bit or CWUINTEN bit to 1, and permit an interruption output.  
 3. Since the wake-up current detection function and the turbo boost current detection function are sharing one comparator, they serve as exclusion use in one of functions.  
 Be sure set up in the TBMODESEL bit of WUDCON2 register.

---

#### 4.6.7 Series Regulator

The RAJ240080 Group incorporates a low-dropout 1.8 V and 3.3 V output series regulator. The 1.8 V regulator is used as the power source of A/D converter, current integrating circuit. The 3.3 V regulator is used as 3.3 V power supply.

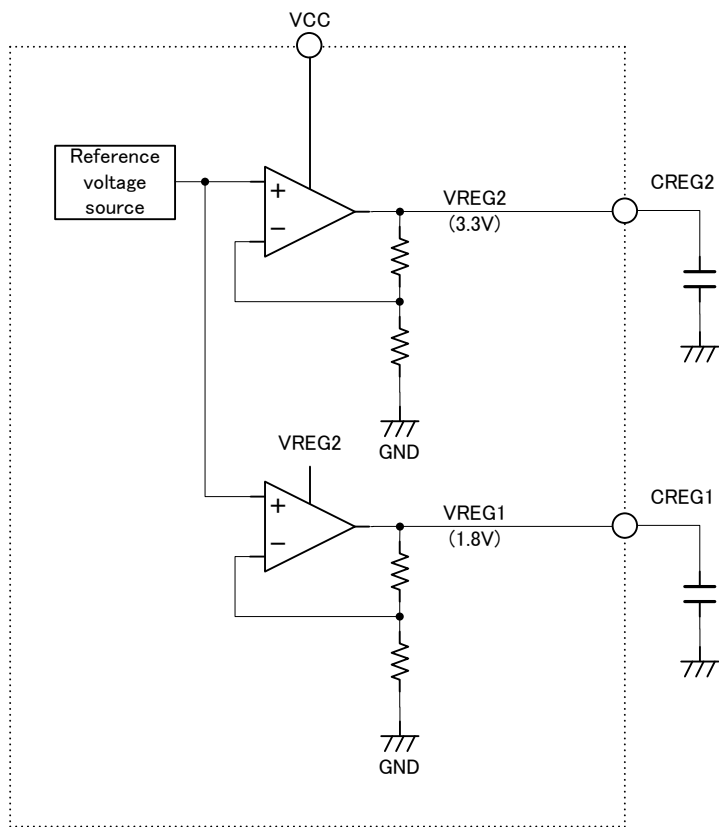
Figure 4-11 Block Diagram of Series Regulator shows the Block Diagram of Series Regulator.

Pch MOS transistors are used for output control. No external resistor or equivalent is required because output voltages are adjusted in the IC.

Attach a 2.2  $\mu\text{F}$  capacitor to the VREG2 output and a 1.0  $\mu\text{F}$  capacitor to the VREG1 to suppress input and load fluctuations.

The settling time after input, output, and load fluctuations should be 10 ms as a standard value.

**Figure 4-11 Block Diagram of Series Regulator**



#### 4.6.8 Reset Circuit

The reset circuit makes RESET (AFE) pin high level or low level by an output of power-on reset circuit or a reset request from MCU runaway detection circuit.

The reset circuit monitors 3.3 V and 1.8 V output voltage of the regulator circuit (VREG2, VREG1).

When the reset circuit detects voltage more than the reference value RESET (AFE) pin output becomes high level. When the reset circuit detects voltage lower than the reference value, the RESET (AFE) pin output signal becomes low level.

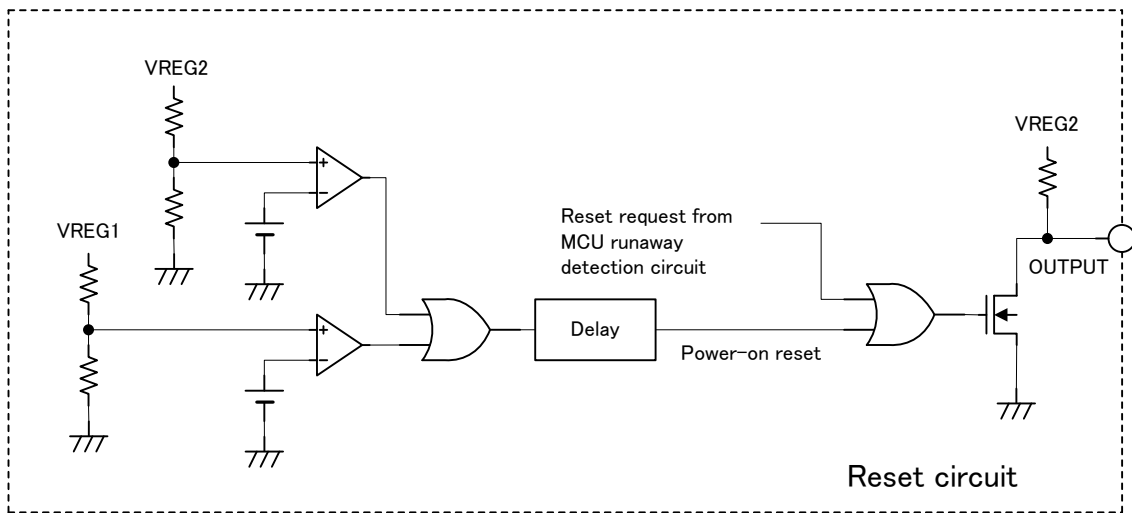
The reset circuit comprises comparators, a reference voltage, a Delay circuit, bleeder resistors, and N-ch transistor.

The reset circuit output is N-ch transistor, RESET (AFE) output is high or low level depend on pull-up resistor built-in RESET (AFE) pin. The reset circuit provides hysteresis for the detection voltage and the cancel voltage. RESET (AFE) pin connects to RESET (MCU) pin and it uses as MCU hardware reset.

Figure 4-12 Block Diagram of Reset circuit shows the Block Diagram of Reset circuit.

**Figure 4-12 Block Diagram of Reset circuit**





### 4.6.9 Serial Interface IICA

Serial interface IICA has the following three modes.

#### (1) Operation stop mode

This mode is used when serial transfers are not performed. It can therefore be used to reduce power consumption.

#### (2) I<sup>2</sup>C bus mode (multimaster supported)

This mode is used for 8-bit data transfers with several devices via two lines: a serial clock (SCLA0) line and a serial data bus (SDAA0) line.

This mode complies with the I<sup>2</sup>C bus format and the master device can generate “start condition”, “address”, “transfer direction specification”, “data”, and “stop condition” data to the slave device, via the serial data bus. The slave device automatically detects these received status and data by hardware. This function can simplify the part of application program that controls the I<sup>2</sup>C bus.

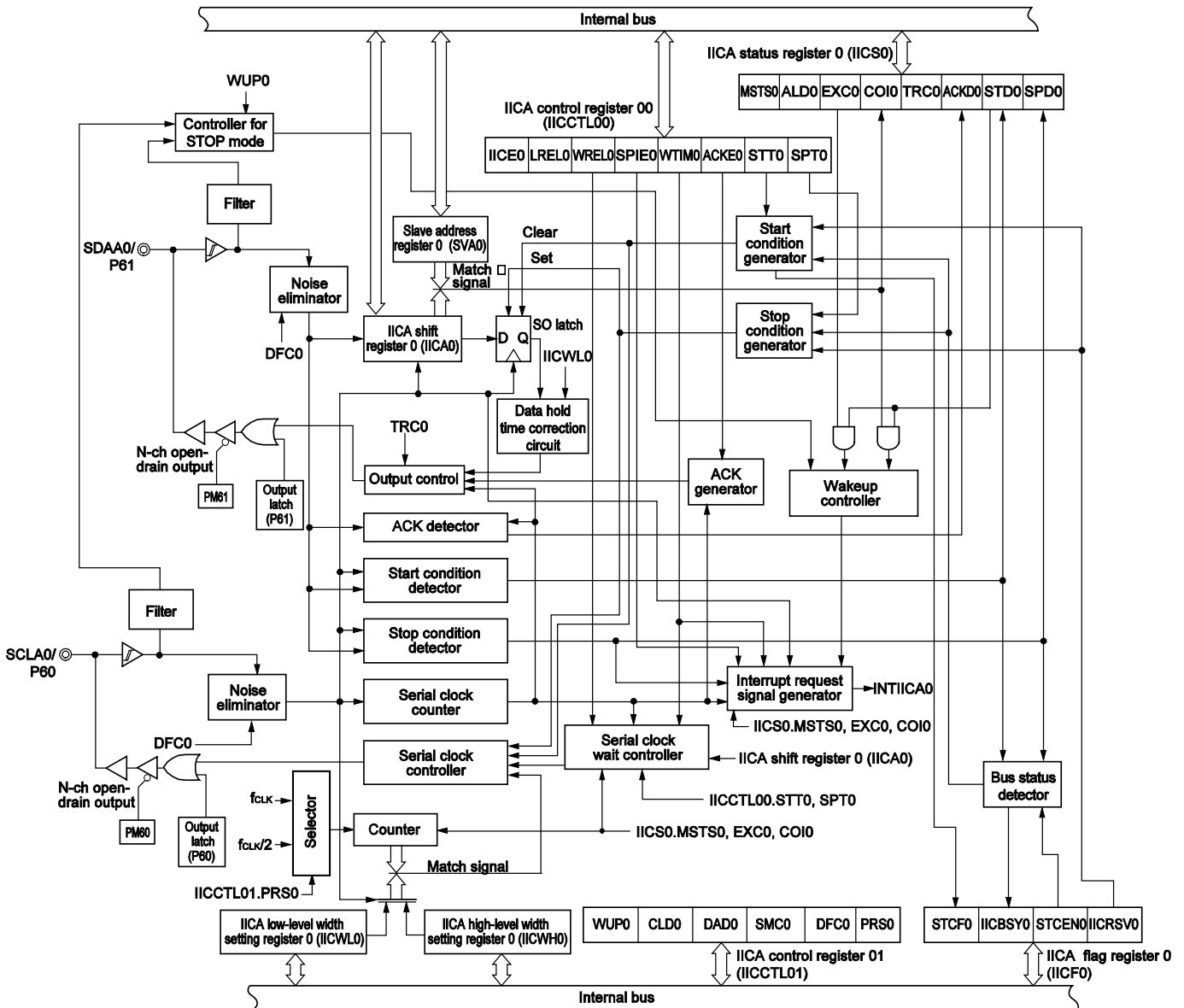
Since the SCLA0 and SDAA0 pins are used for open drain outputs, serial interface IICA requires pull-up resistors for the serial clock line and the serial data bus line.

#### (3) Wakeup mode

The STOP mode can be released by generating an interrupt request signal (INTIICA0) when an extension code from the master device or a local address has been received while in STOP mode. This can be set by using the WUP0 bit of IICA control register 01 (IICCTL01).

Figure 4-13 Block Diagram of Serial Interface IICA shows a block diagram of serial interface IICA.

**Figure 4-13** Block Diagram of Serial Interface IICA



### 4.6.10 Serial Array Unit

Serial array unit has four serial channels. Each channel can achieve 3-wire serial (CSI), UART, and simplified I<sup>2</sup>C communication.

#### (1) 3 wire serial I/O (CSI11, CSI21)

Data is transmitted or received in synchronization with the serial clock ( $\overline{SCK}$ ) output from the master channel.

3-wire serial communication is clocked communication performed by using three communication lines: one for the serial clock ( $\overline{SCK}$ ), one for transmitting serial data (SO), one for receiving serial data (SI).

---

**[Data transmission/reception]**

- Data length of 7 or 8 bits
- Phase control of transmit/receive data
- MSB/LSB first selectable
- Level setting of transmit/receive data

**[Clock control]**

- Master/slave selection
- Phase control of I/O clock
- Setting of transfer period by prescaler and internal counter of each channel
- Maximum transfer rate
  - During master communication: Max.  $f_{CLK}/4$  <sup>Note</sup>
  - During slave communication: Max.  $f_{MCK}/6$  <sup>Note</sup>

**[Interrupt function]**

- Transfer end interrupt/buffer empty interrupt

**[Error detection flag]**

- Overrun error

It cannot be corresponding to SNOOZE mode in this product.

**Note** Use the clocks within a range satisfying the  $\overline{SCK}$  cycle time ( $t_{CKCY}$ ) characteristics (see 3 ELECTRICAL SPECIFICATIONS).

**(2) UART (UART0)**

This is a start-stop synchronization function using two lines: serial data transmission (TxD) and serial data reception (RxD) lines. By using these two communication lines, each data frame, which consist of a start bit, data, parity bit, and stop bit, is transferred asynchronously (using the internal baud rate) between the microcontroller and the other communication party. Full-duplex UART communication can be performed by using a channel dedicated to transmission (even-numbered channel) and a channel dedicated to reception (odd-numbered channel). The LIN-bus can be implemented by using timer array unit with an external interrupt (INTP0).

**[Data transmission/reception]**

- Data length of 7, 8, or 9 bits
- Select the MSB/LSB first
- Level setting of transmit/receive data and select of reverse
- Parity bit appending and parity check functions
- Stop bit appending

**[Interrupt function]**

- Transfer end interrupt/buffer empty interrupt
- Error interrupt in case of framing error, parity error, or overrun error

**[Error detection flag]**

- Framing error, parity error, or overrun error

It cannot be corresponding to LIN-bus and SNOOZE mode in this product.

**(3) Simplified I<sup>2</sup>C (IIC11)**

This is a clocked communication function to communicate with two or more devices by using two lines: serial clock (SCL) and serial data (SDA). This simplified I<sup>2</sup>C is designed for single communication with a device such as EEPROM, flash memory, or A/D converter, and therefore, it functions only as a master.

Make sure by using software, as well as operating the control registers, that the AC specifications of the start and stop conditions are observed.

---

**[Data transmission/reception]**

- Master transmission, master reception (only master function with a single master)
- ACK output function and ACK detection function
- Data length of 8 bits (When an address is transmitted, the address is specified by the higher 7 bits, and the least significant bit is used for R/W control.)
- Manual generation of start condition and stop condition

**[Interrupt function]**

- Transfer end interrupt

**[Error detection flag]**

- Parity error (ACK error), or overrun error

**[Functions not supported by simplified I<sup>2</sup>C]**

- Slave transmission, slave reception
- Arbitration loss detection function
- Wait detection functions

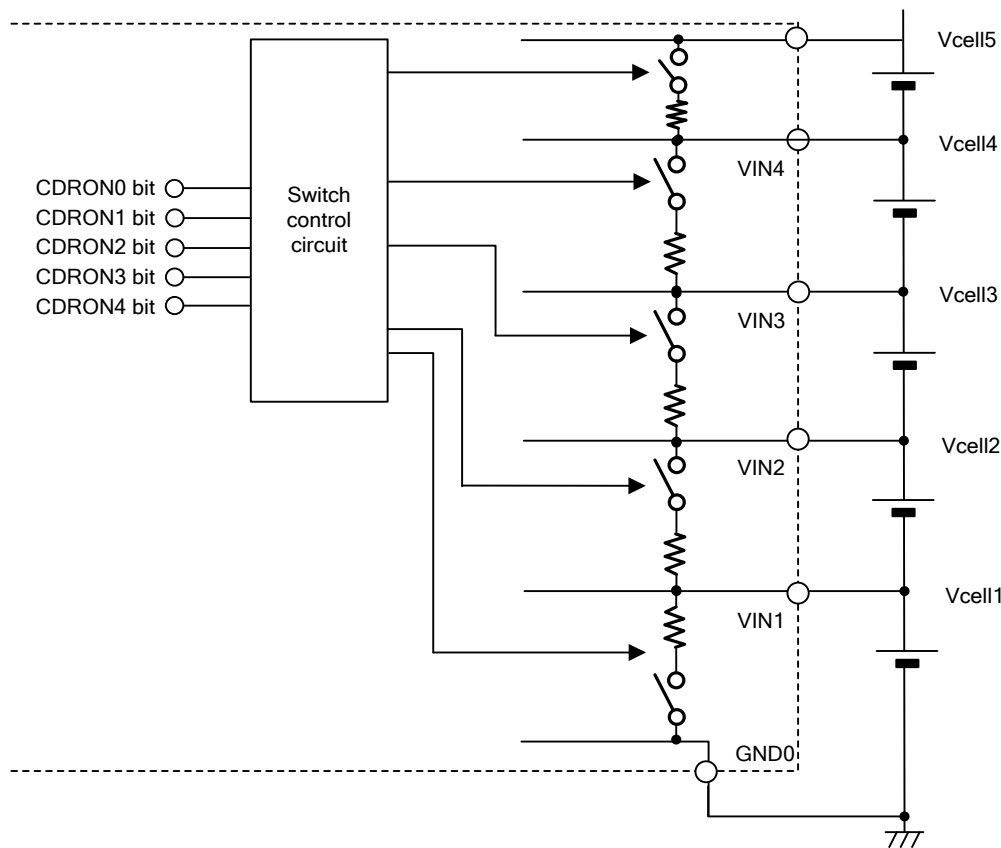
#### 4.6.11 Conditioning circuit

The conditioning circuit is equipped with a function to internally discharge each cell of the battery connected. This function can decrease the voltage of an overcharged battery, which increases the safety of the battery pack. In addition, voltages between connected battery cells can be the same voltage, allowing full charge of all cells. This enables the battery pack to be used for a long period. The MCU selects a cell for self-discharge. Conditioning control is enabled by controlling the switches with the serial data from the MCU.

The conditioning circuit comprises MOS switches and logic circuit. Any battery cell (Vcell1 to Vcell5) can be set for self-discharge by setting the CDRON0 to CDRON 4 bit in the COND register.

Figure 4-14 Block Diagram of Conditioning Circuit shows the Block Diagram of Conditioning Circuit.

Figure 4-14 Block Diagram of Conditioning Circuit



#### 4.6.12 Fuse control circuit

The fuse control circuit is used for a system controlling a fuse used for cutting charge/discharge path at the time of the abnormality. In addition, this fuse control circuit is able to read the failure mode identification register data from MCU after the fuse was cut off. It is possible to identify the failure mode.

Figure 4-15 Example for the Fuse Control System shows Example for the Fuse Control System.

##### (1) Fuse control

When abnormal state is detected by MCU write the FUSECUT0, FUSECUT1 bit in the AFECON2 register to 11b, FUSEOUT pin becomes High level, and turn on the fuse cutting FET.

##### (2) The failure mode identification

It can read a state of FUSEOUT pin by reading the FUSEMON bit in the AFECON3 register.

The FUSEOUT pin becomes HiZ level when VCC level output can't be controlled by fuse control function. Therefore it can detect a state that the fuse cutting FET is ON by the fuse cutting FET by reading the FUSEMON bit.

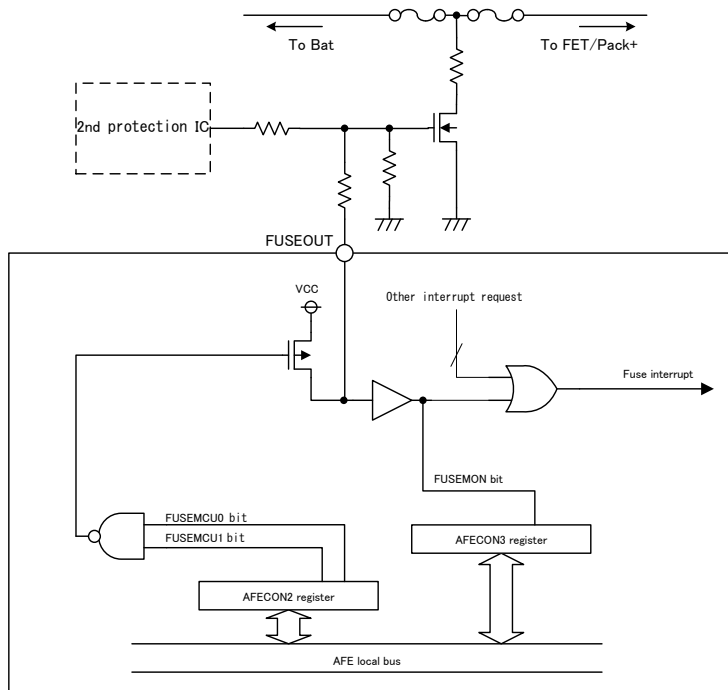
Input of FUSEOUT pin connects to P06/INTP11 of MCU internally, when FUSEOUT pin becomes VCC level it can detect external interrupt of MCU.

By INTP11 interrupt during fuse cut off, write the values of FUSECUT0, FUSECUT1, and FUSEMON bit in the flash memory. To read that written data from flash memory after fuse was cut off, it is possible to identify the failure mode.

The Interrupt request pin of FUSEOUT that connects to P06/INTP11 of MCU internally is the INT\_AFE\_ANL (abnormal interrupt).

**Note.** INT\_AFE\_ANL is shared many AFE causes of interrupt. Therefore, confirm a cause of FUSEOUT pin by reading the FUSEIR bit in the INTIR register.

**Figure 4-15 Example for the Fuse Control System**



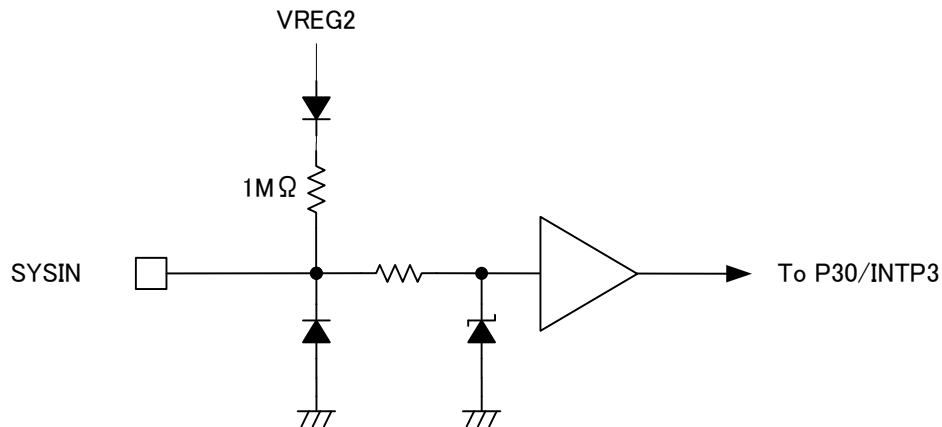
### 4.6.13 High voltage port

This product contains the high voltage port. Mounted high voltage port in this product is SYSIN pin.

SYSIN pin is able to use as input pin of system presence function which is recognized to connect up battery pack to main system.

SYSIN pin output connects P30/INTP3 of MCU in package, when L level inputs it can detect external interrupt (INTP3). Figure 4-16 Block diagram of SYSIN pin shows Block diagram of SYSIN pin.

Figure 4-16 Block diagram of SYSIN pin



### 4.6.14 MCU runaway detection Circuit

MCU runaway detection circuit can be detected a MCU runaway. It can be monitoring CPU runaway independently of MCU watchdog timer.

MCU runaway detection circuit comprises pre-scaler to be divided AFE on-chip oscillator and 16 bits counter. It can be selected the overflow time from 2, 4, and 8 [s]

Table 4-6 MCU runaway detection circuit specification list shows MCU runaway detection circuit specification,

Figure 4-17 Block Diagram of MCU runaway detection circuit shows Block Diagram of MCU runaway detection circuit.

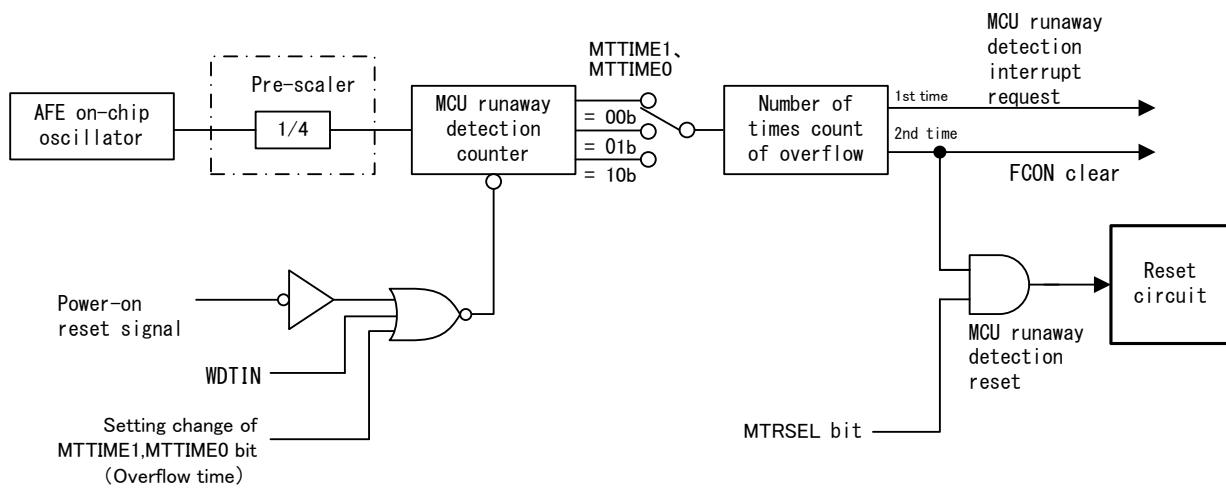
**Table 4-6 MCU runaway detection circuit specification**

Item	Specification
Overflow time	2, 4, 8 [s]
Count source	AFE on-chip oscillator divided by 4
Counter bit length	19 bits
Operation of the overflow	(1)overflow for first time <ul style="list-style-type: none"> <li>▪ set the WDTIR bit to 1</li> </ul> (2)Overflow for second time <ul style="list-style-type: none"> <li>when the MTRSEL bit is "0"               <ul style="list-style-type: none"> <li>▪ clear the FETC bit and the FETD bit to 0</li> </ul> </li> <li>when the MTRSEL bit is "1"               <ul style="list-style-type: none"> <li>▪ clear the FETC bit and the FETD bit to 0</li> <li>▪ MCU runaway detection reset is generated.</li> </ul> </li> </ul>
Refresh conditions	<ul style="list-style-type: none"> <li>▪ P76 of MCU is applied to H pulse to WDTIN pin <sup>Note</sup>.</li> <li>▪ Power-on reset</li> <li>▪ Overflow time change</li> </ul>

**Note** the P76 of MCU is connected to WDTIN inside package. Also the WDTIN incorporated the pull-down resistor.



**Figure 4-17 Block Diagram of MCU runaway detection circuit**



MTTIME1, MTTIME0, MTRFRSH : Bit of AWDTCON register  
 FCON : FET driver control register  
 WDTIN : Refresh signal input ( The contact port between MCU and AFE).

---

## 5. Application Guideline

### 5.1 Typical Application Specification

Typical specification example of Li-ION battery management unit is shown below.

Battery cell assembly	: 5S1P (5 cells in series and 1 cell in parallel)
Host interface	: System Management Bus (SMBus) Specification, version 1.1.
Primary protection	: charge FET and discharge FET
Secondary protection	: Fuse blow by FGIC (RAJ240080) or a secondary protection device.
RSOC display	: 4 LEDs

Connector pins:

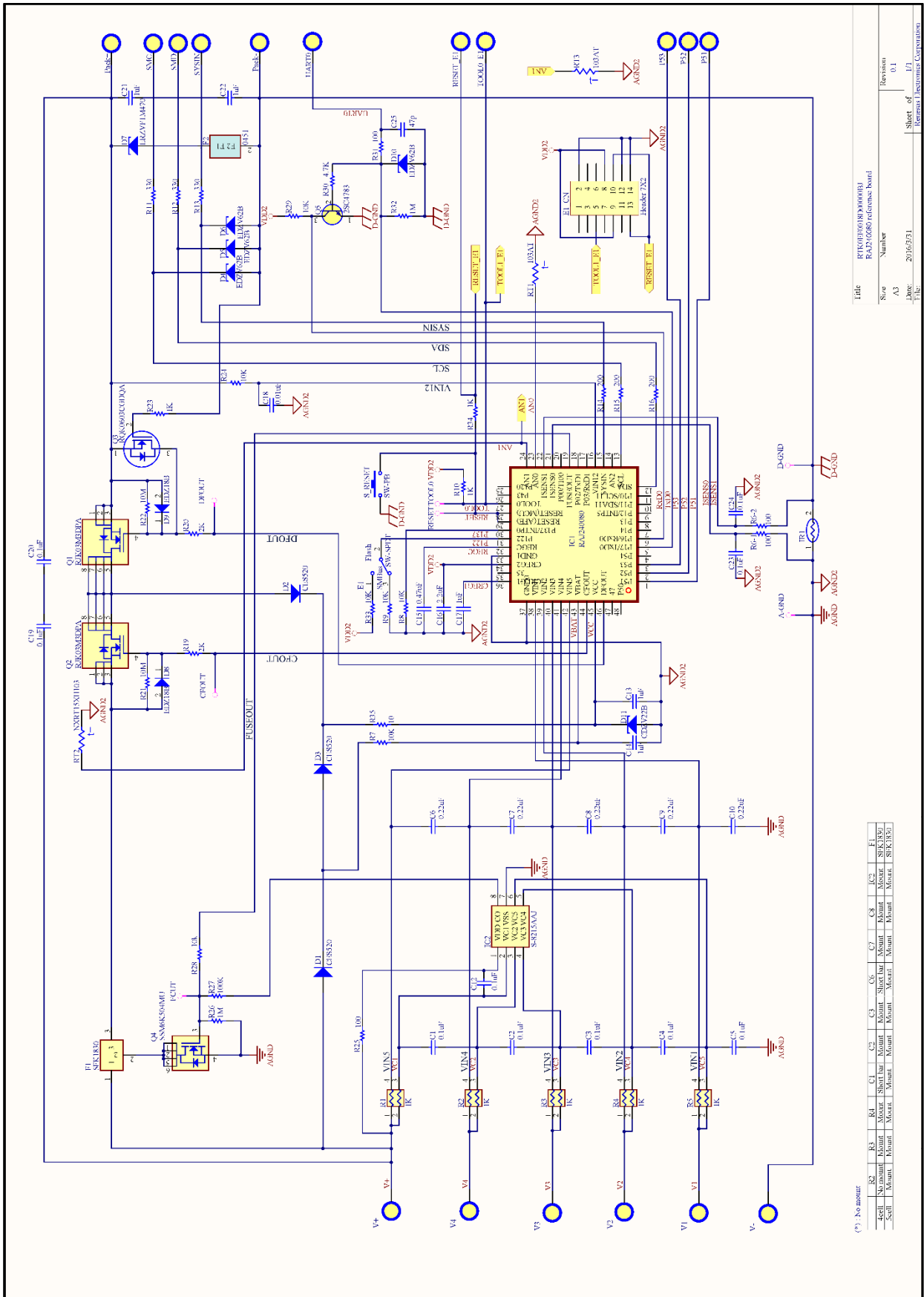
Pack+	Positive battery pack terminal
SMC	SMBus clock
SMD	SMBus data
SYSIN	Battery insertion detection
Pack-	Negative battery pack terminal

External reverse charge protection circuit

Battery temperature measurement with two thermistors

## 5.2 Typical Application Circuit

### Typical Application Circuit Schematic

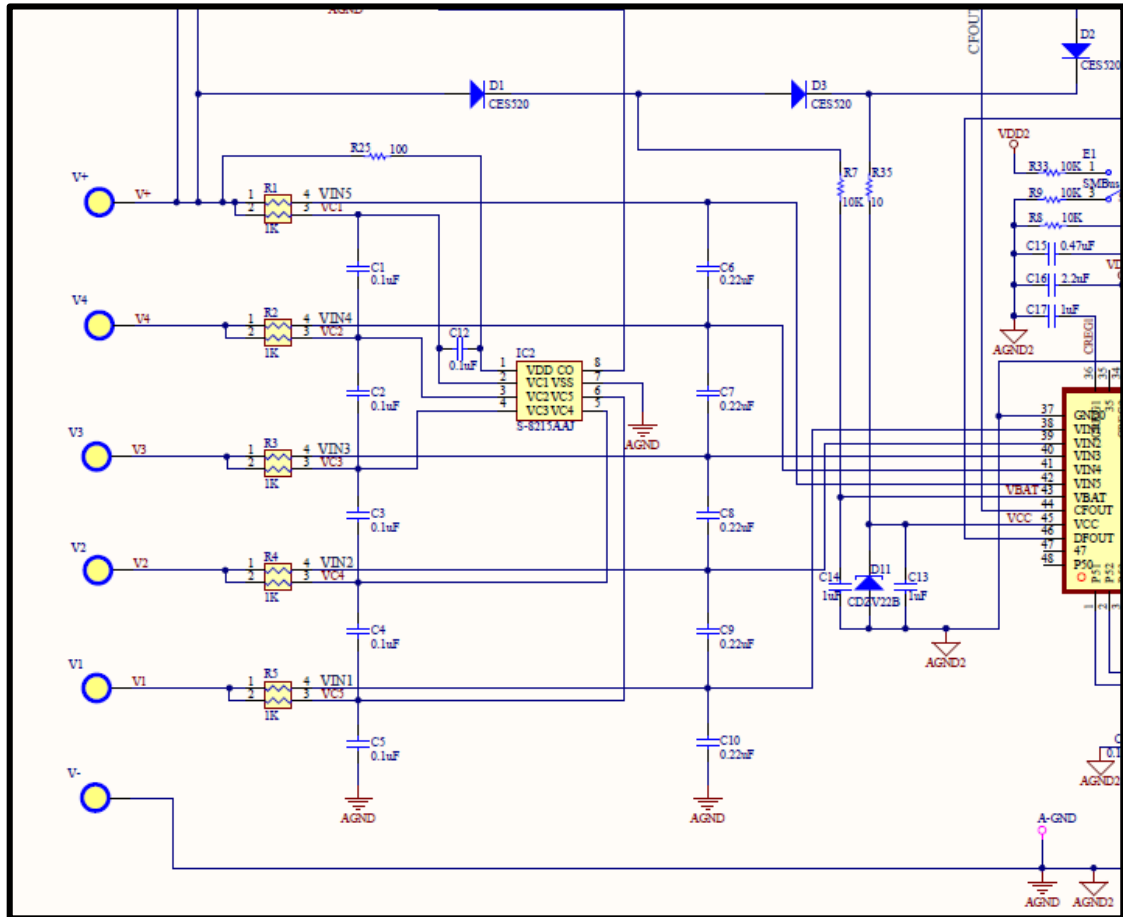


Title		Part Number		Revision	
RKA24080-10000001		RKA24080-reference board		01	
Doc. No.	2016/03/31	Sheet of	1/1		
Revision History					
No.	Reason	Author	Check	Appr.	Date
1	Initial Release				

## 5.3 Circuit Design Guideline

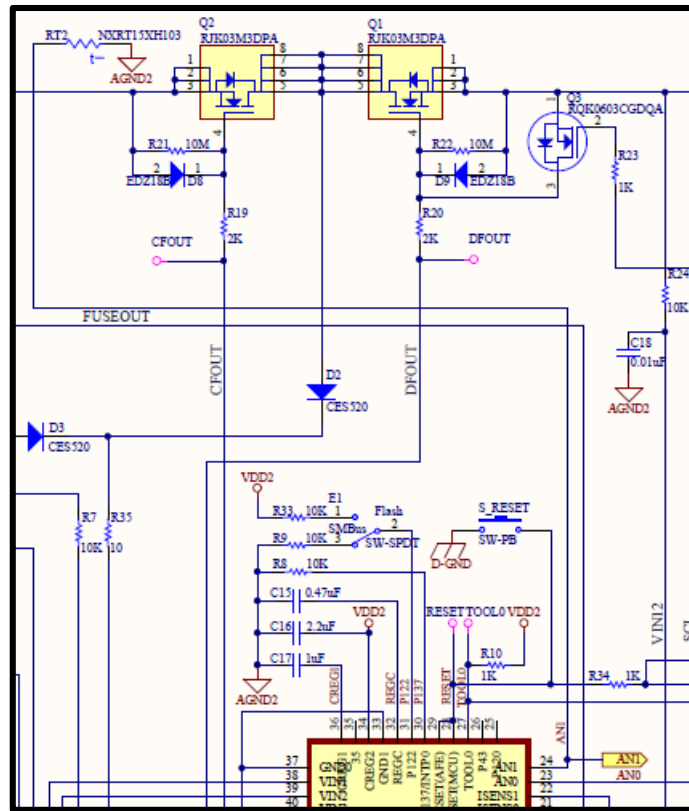
### 5.3.1 Cell voltage monitor circuit

- Provide input filter independently for RAJ240080 and 2nd protection IC.
- Place resistors around  $1\text{k}\Omega$  to VIN1 – VIN5 as they works also as surge protection.  $0.22\mu\text{F}$  is recommended for C6-C9, so cut-off frequency become  $0.7\text{ kHz}$  with  $1\text{k}\Omega$ .
- Higher cut-off frequency can be set if it's OK with voltage detection accuracy.



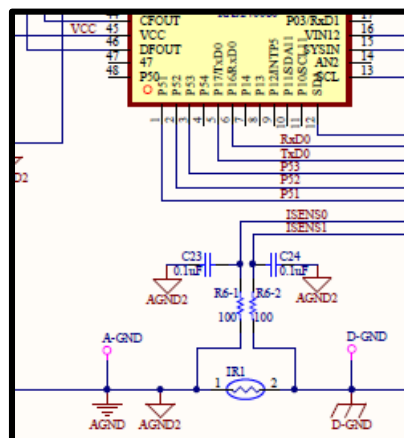
### 5.3.2 Charger connect detection circuit

- R24 plays a role for current limit when charger is reverse-charged. 10kΩ is recommendable, but when it is too large, charger connect detection circuit may operate erroneously.
- C18 works for stable charger connect detection and D-FET boost operation. 0.01μF is recommendable. If it is too large, OFF time when short-circuited will be long, if it is too small, boosted voltage may fluctuate.



### 5.3.3 Current monitor

- Potential difference on sense resistor is monitored by current integration circuit.
- Put Low Pass Filter (100 Ω, 0.1μF) for input stage.
- Sense traces should be shielded for detecting small voltage difference.

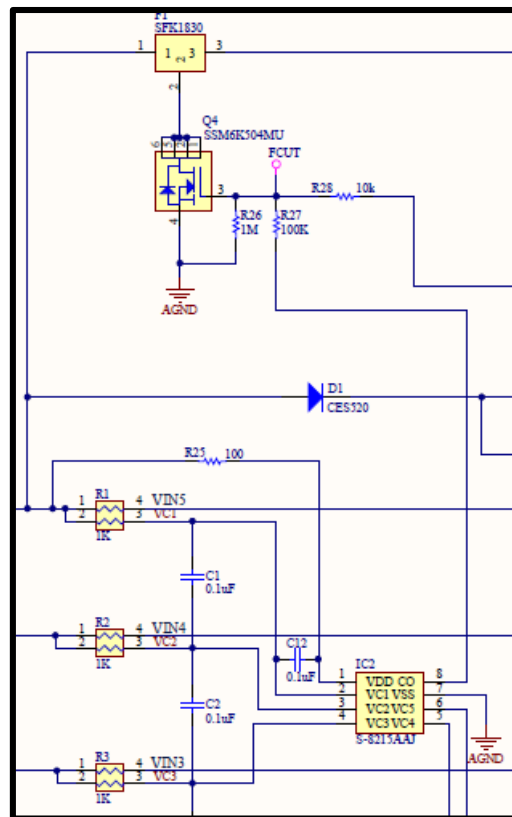


### 5.3.4 Fuse control

SPC is used for fuse.

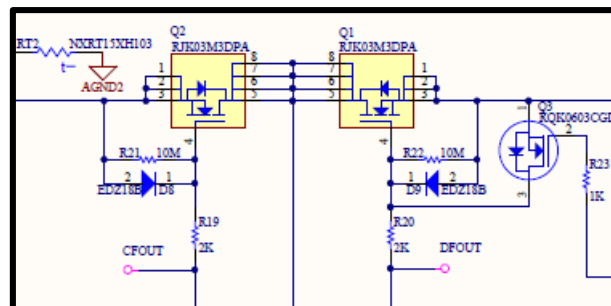
The fuse is blown by the following three paths.

1. RAJ240080 drives FUSEOUT pin high to make Q4 ON.
2. When 2nd protection IC detects overcharge voltage, CO becomes high to make Q4 ON.



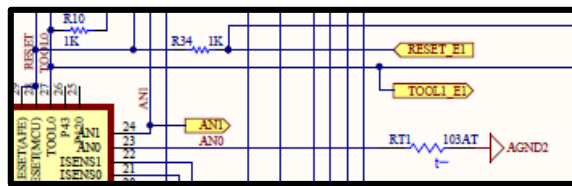
### 5.3.5 Protection FET control

- Q3 is located between gate and source of Q1 to make D-FET off when charger is reversely connected.
- R23 is for Q3 gate protection. (1kΩ is recommended.)
- R19/R20 are for gate protection and C-FET/D-FET noise reduction. (2kΩs is recommended.)
- R21/R22 are for fixing C-FET/D-FET gate voltage when FET is off. 10MΩs is recommended to prevent voltage drop.

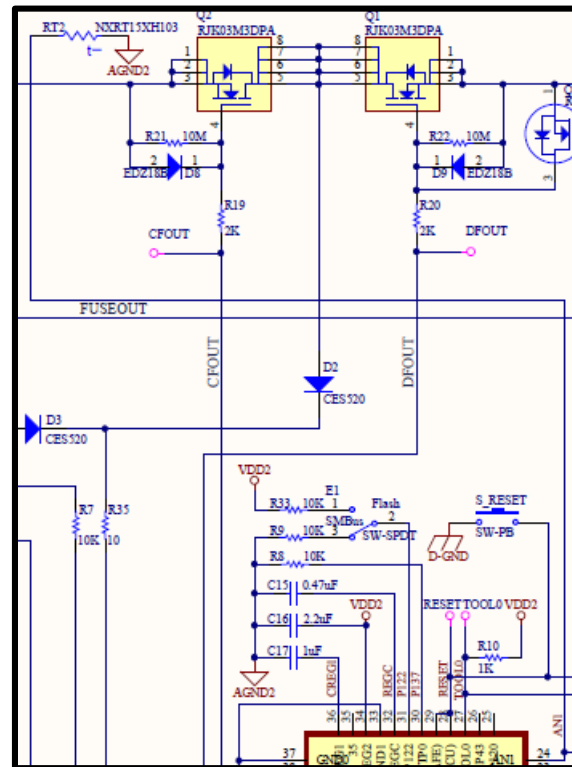


### 5.3.6 Thermistor

- ADC voltage measurement pins (AN0/AN1) are provided for thermistor use.



AN0 pin



AN1 pin

### 5.3.7 System presence

Connect R13 (330 Ω) and R14 (200 Ω) for ESD protection at SYSIN input.

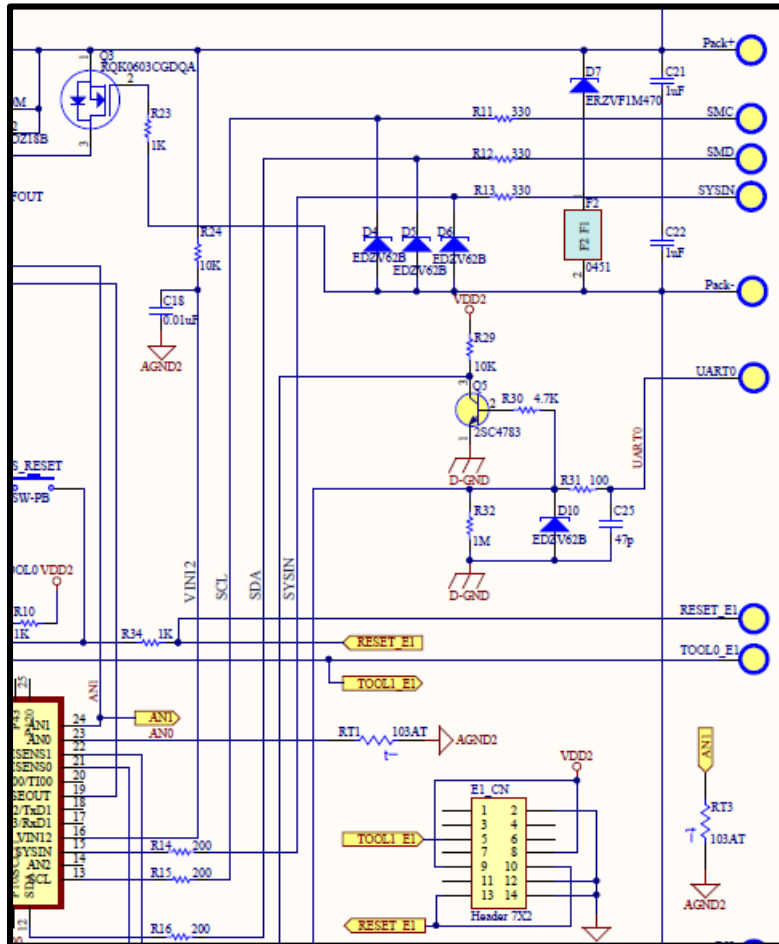
Connect zener diode to protect against short-circuit with Pack+.

Zener diode must be the one with its zener voltage less than 6.5V, an absolute maximum rating of CREG2.

Recommended: EDZV6.2B (Rohm)

### 5.3.8 Communication line

- Put 330Ω (resistor R11/R12) at input stage of SCL/SDA.

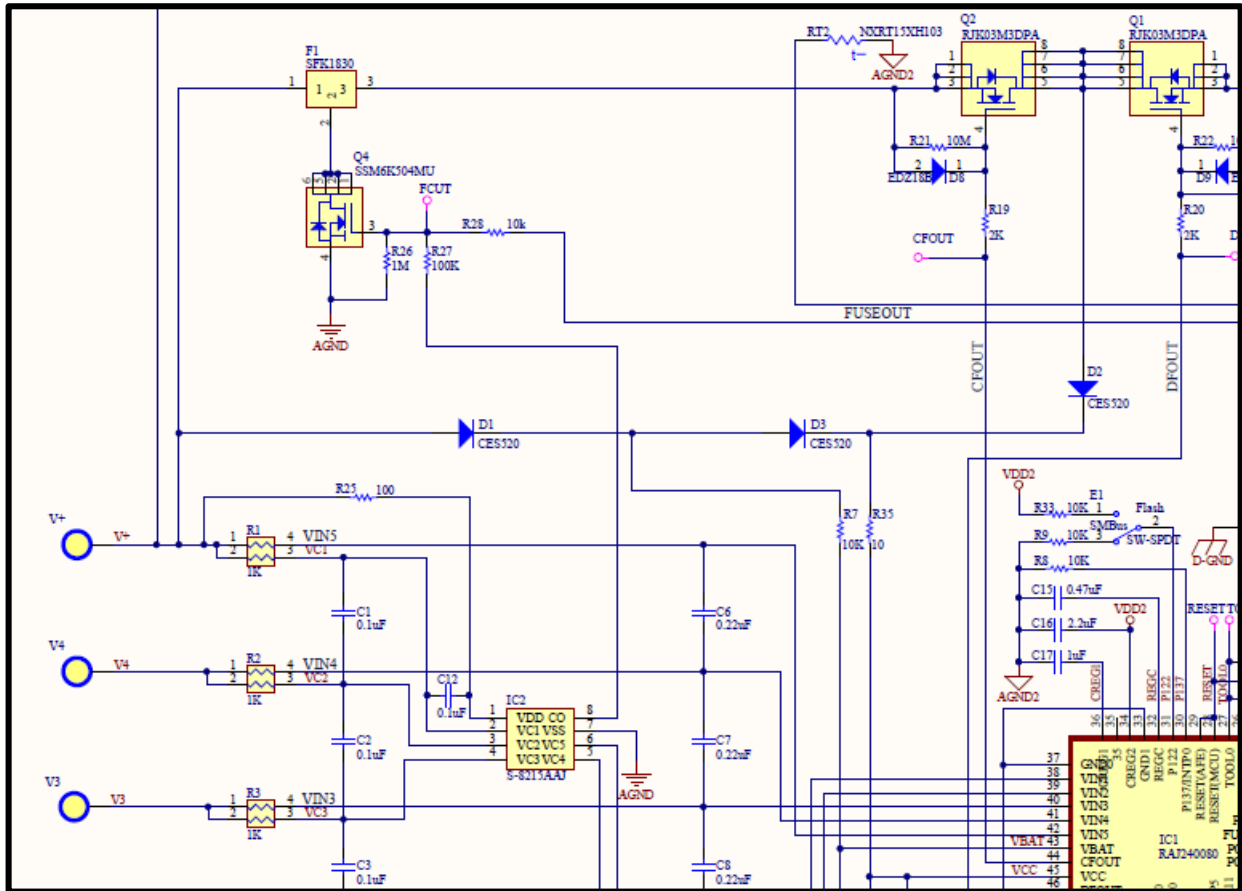




### 5.3.9 Power supply path

Power supply is provided to VCC through the following two paths.

1. Higher voltage out of battery and charger is provided as power supply.
2. Power supply is provided from battery side when fuse is blown.



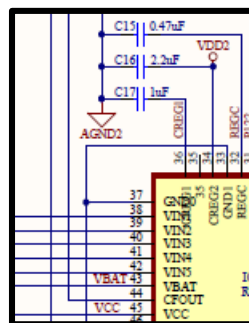
### 5.3.10 CREG1/CREG2/REGC capacitance

The following decoupling capacitor must be located as adjacent to each terminal as possible.

C17: CREG1/AGND2 (1 $\mu$ F is recommended.)

C16: CREG2/AGND2 (2.2 $\mu$ F is recommended.)

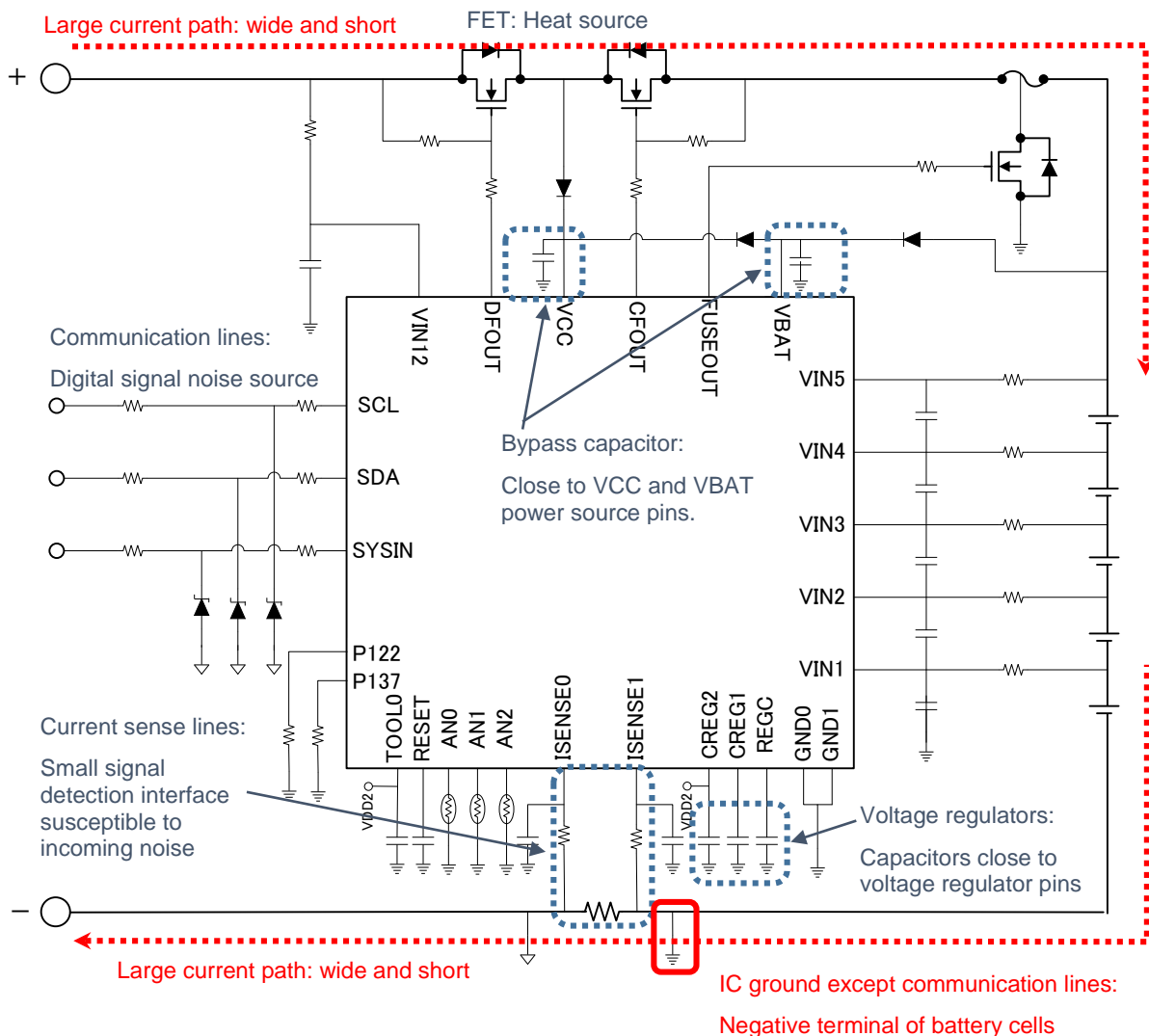
C15: REGC/AGND2 (0.47 $\mu$ F to 1 $\mu$ F is recommended.)



## 5.4 Layout Guidelines

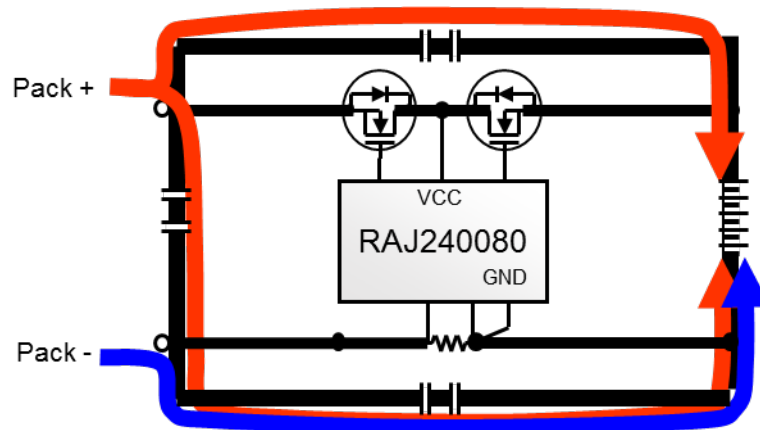
### 5.4.1 Summary

- Large current patterns must be wide and short to minimize voltage drop and the heat generation.
- Bypass capacitors must be mounted as close as possible to the device VCC / VBAT and GND pins to prevent erroneous operations due to noise from power supply.
- Capacitors for voltage regulators must be located close to regulator pins to ensure loop stability and ESD tolerance.
- All IC ground must be connected to the negative terminal of battery cells except ground for communication lines.
- Communication lines must be away from small signal current sense line to prevent the input signal from being disturbed by the incoming radiation noise.
- RAJ240080 must be located away from any heat source (FET, current sense resistor and large current patterns) to minimize the influence of heat.



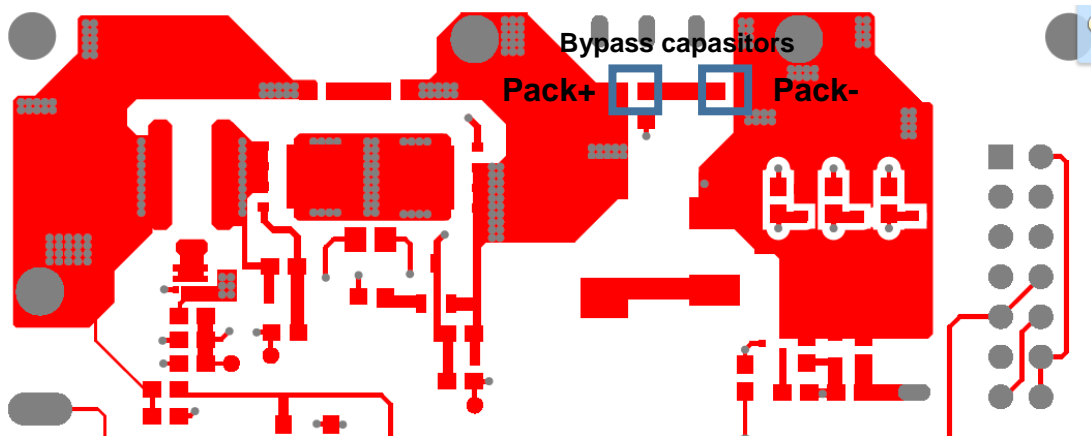
### 5.4.2 ESD protections on each terminal (basic policy)

- ESD applied on Pack+ terminal must be lead to the top side of the cell or to Pack- terminal through a capacitor.
- ESD applied to Pack- terminal must be lead to the GND side of the cell.
- ESD applied to communication terminals and other GPIOs must be lead to the GND side of the cell via Pack- terminal.
- The noise from PACK+ or PACK- must be lead to battery cell so that it will not interfere with RAJ240080 functions and measurements.



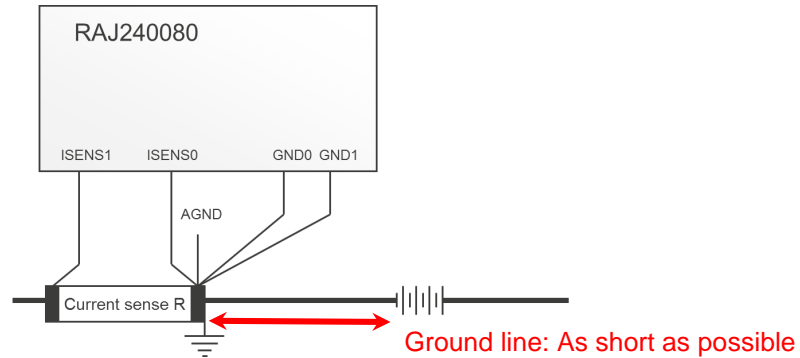
### 5.4.3 Pack+, Pack-

- Bypass capacitor must be placed between Pack+ and Pack-. (Countermeasure against ESD)
- Bypass capacitor must be located adjacent to Pack+, Pack-. (Minimize the ESD influence)
- Capacitors must be placed in series. (Countermeasure against short-circuit of capacitors)
- Don't use tantalum capacitor. (Tantalum capacitor can end up with short-circuited failure when damaged.)



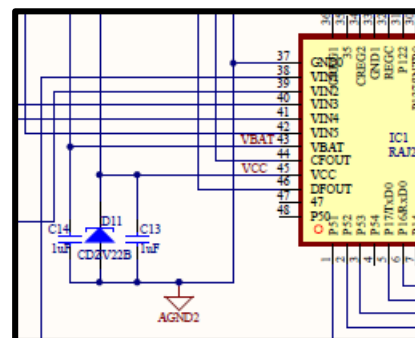
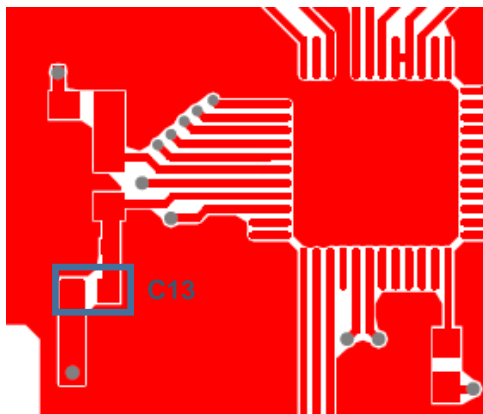
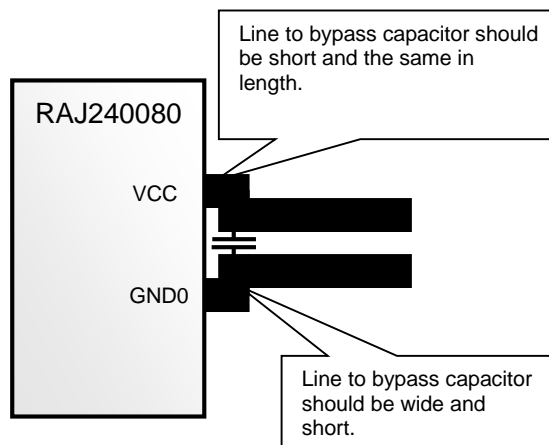
### 5.4.4 How AGND and AGND2 must be connected to the ground

- AGND and AGND2 of RAJ240080 must be connected to the one point of current detection resistor of the cell side by the pattern with an adequate width. (Prevent potential variation by large current.)
- The patterns between AGND and AGND2 must not be divided. (Keeping the GND potential of MCU and AFE equal)
- The lines from cell GND to current sensing resistor must be wide and as short as possible to avoid potential difference generated between cell GND and RAJ240080 when current flows.



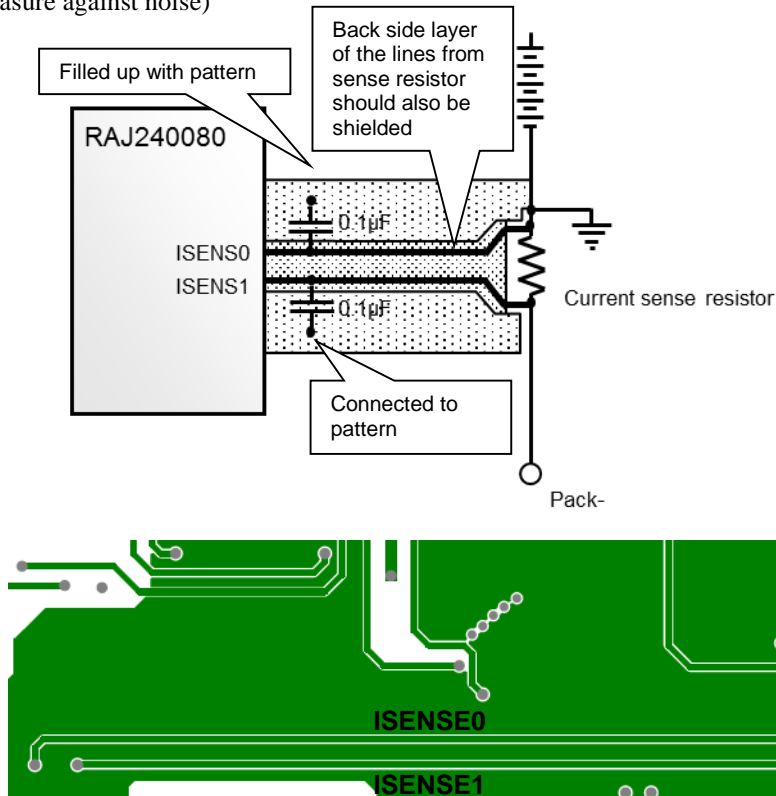
### 5.4.5 Bypass capacitor between VCC and GND0

- The patterns between VCC pin and a bypass capacitor and between GND0 pin and a bypass capacitor must be as short as possible and the same in length with each other. (Countermeasure for ESD) RAJ240080 and bypass capacitors must be placed on the same side of PCB without any through-hole.
- The lines to bypass capacitor must be wide and short. (To keep bypass capacitor effective in suppressing the potential variation.)



### 5.4.6 ISENS0, ISENS1

- Two lines from current sense resistor to ISENS0, ISEN1 must be the same in width and length, and in parallel with the same space between the two lines. (Prevent erroneous detections due to noise)
- The space between lines to ISENS0 and ISENS1 must be filled up with the shielding pattern one which is connected to GND. Also, the layer on the pack side of board must also be filled up with the shielding pattern. (Prevent erroneous detections due to noise)
- There must be no unnecessary divergence between current sense resistors to ISENS0 and ISENS1. (Incoming noise from the pattern unnecessarily divergence.)
- Capacitors connected to shielding pattern are recommended to be located adjacent to RAJ240080. (Countermeasure against noise)



### 5.4.7 SMBus

- SMBus lines must be equipped with zener diodes. And it is necessary to mount resistors on the side of RAJ240080 and D-GND. (Zener diode and the resistor on the side of D-GND are for surge countermeasure, the resistor on the side of FG-IC for noise countermeasure.)
- The resistor on the side of RAJ240080 must be located as adjacent to FG-IC as possible. (Countermeasure for noise)

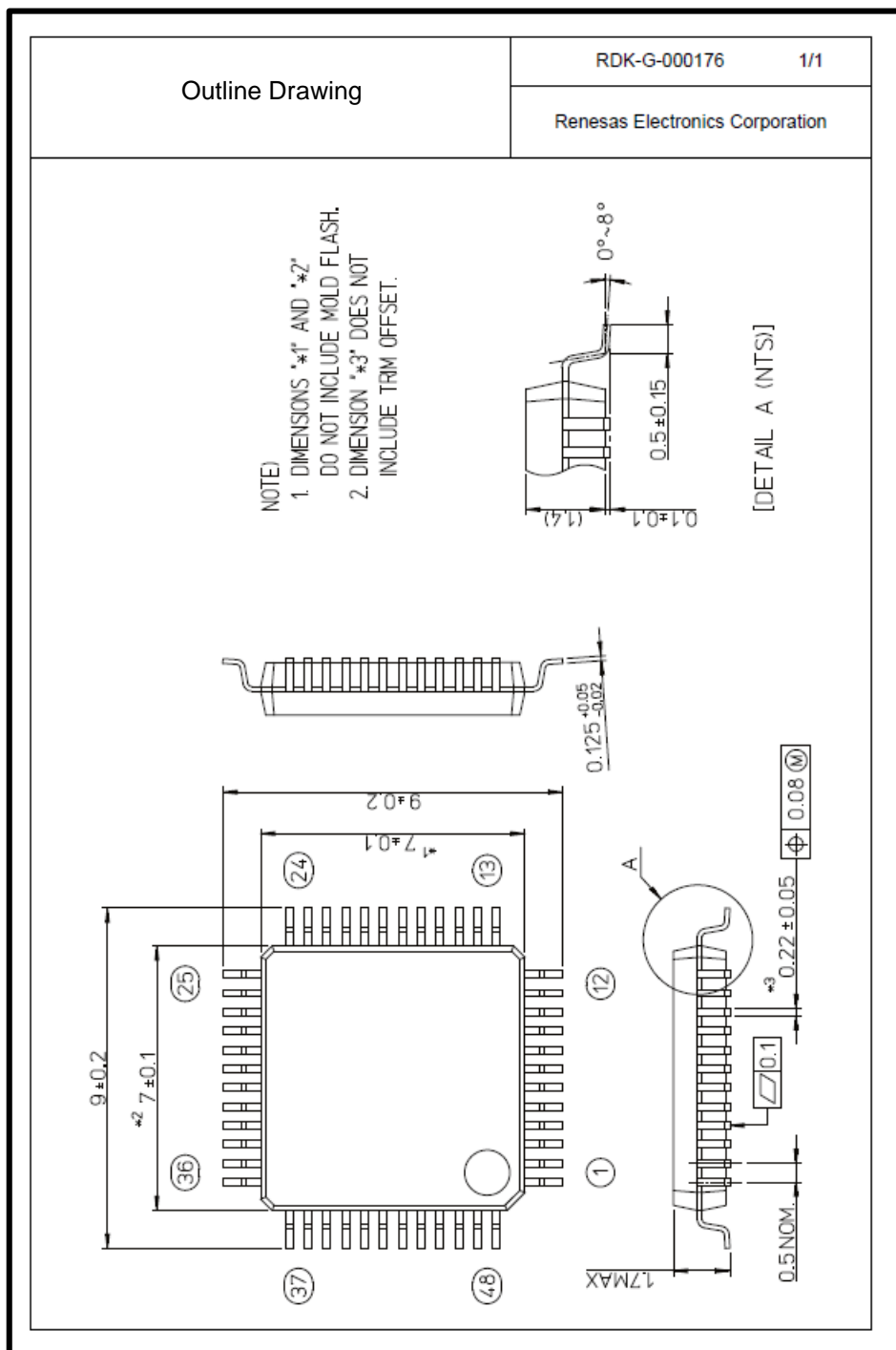
### 5.4.8 Unused Pins

- Unused pins are recommended to be connected to GND via resistor. (It is connected via resistor to GND against ESD. Setting low output by software prevents the terminal from becoming indefinite).

### 5.4.9 Cell GND

- The lines from cell GND to current sensing resistor must be wide and as short as possible. (To avoid potential difference generated between cell GND and RAJ240080 when current flows. Cell voltage on the side of GND can not be detected correctly when potential difference is generated.)

## 6. Packaging Information



---

## REVISION HISTORY

Revision	Description	Chapter
Rev1.00	Initial version.	-

## Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through or website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in the document. No license, express, implied, or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in the document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheet or data book, etc.  

"Standard":	Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.
"High Quality":	Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.
"Specific":	Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrences of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by for Renesas Electronics.



---

## NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to CREG2 (VREG2) or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE:** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up