8TS805, 806
Latches/Flip-Flops

8TS805 Octal Transparent Latch With 3-State Outputs
8TS806 Octal D Flip-Flop With 3-State Outputs
Product Specification

Logic Products

FEATURES

- **8-bit transparent latch – 8TS805**
- **8-bit positive, edge-triggered register – 8TS806**
- **3-State output buffers**
- **Common 3-State Output Enable**
- **Independent register and 3-State buffer operation**

DESCRIPTION

The 8TS805 is an octal, transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one set-up time before the High-to-Low enable transition. The enable gate has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
8TS805	10ns	105mA
8TS806	8ns	116mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N8TS805N, N8TS806N

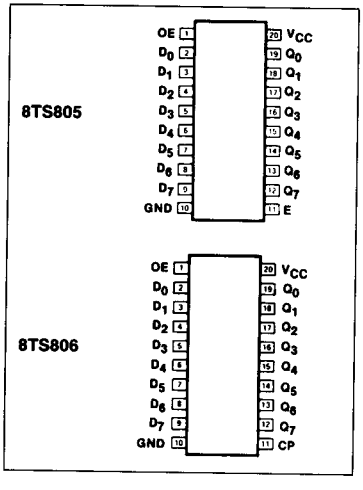
NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

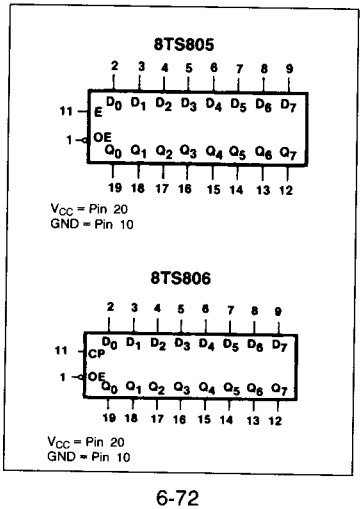
PINS	DESCRIPTION	8TS
All	Inputs	1Sul
All	Outputs	10Sul

NOTE:
An 8TS unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}.

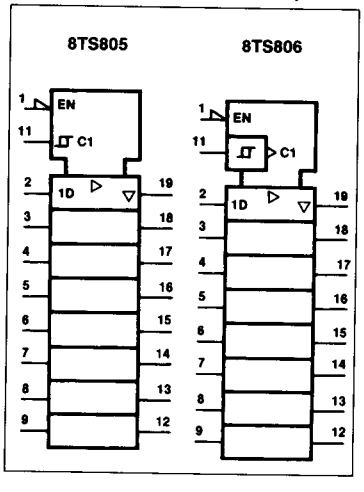
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

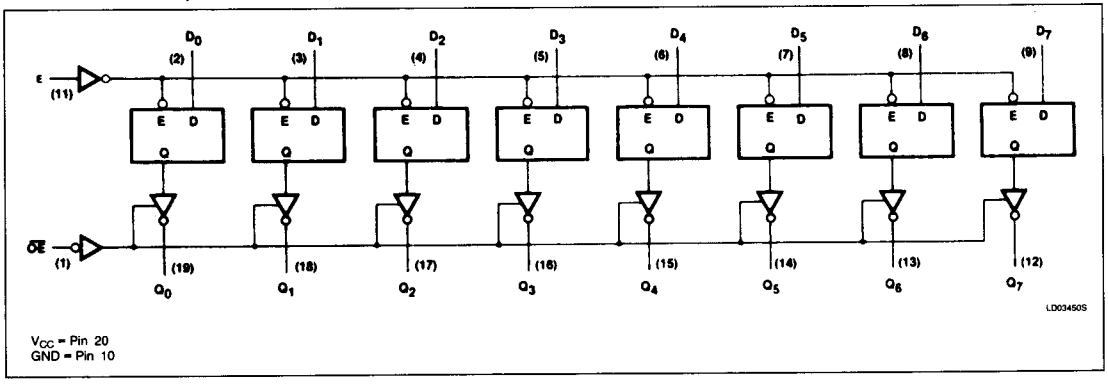


The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is LOW, the latched or transparent data appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

The 8TS806 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

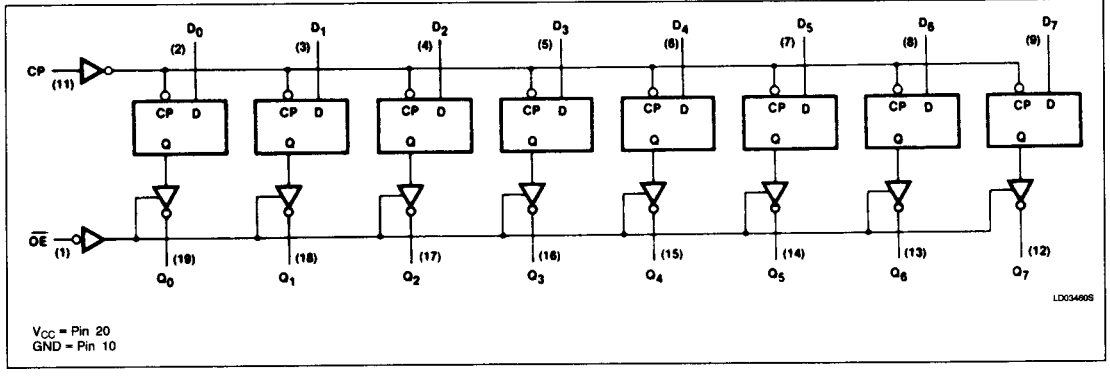
The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

LOGIC DIAGRAM, 8TS805



V_{CC} = Pin 20
GND = Pin 10

LOGIC DIAGRAM, 8TS806



V_{CC} = Pin 20
GND = Pin 10

MODE SELECT — FUNCTION TABLE, 8TS805

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		$Q_0 - Q_7$
Enable and read register	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Disable outputs	H	X	X	X	(Z)

MODE SELECT — FUNCTION TABLE, 8TS806

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		$Q_0 - Q_7$
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	X	X	X	(Z)

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW OE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW OE transition.
(Z) = HIGH impedance "off" state
↑ = LOW-to-HIGH clock transition
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		S8TS	N8TS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to $+V_{CC}$	−0.5 to $+V_{CC}$	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		8TS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−6.5	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

NOTE:
V_{IL} = + 0.7V MAX for S8TS at T_A = + 125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS[1]			8TS805, 806			UNIT
				Min	Typ[2]	Max	
V_{OH} HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX			2.4	3.1		V
V_{OL} LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX				0.5	V
V_{IK} Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.2	V
I_{OZH} Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V					50	μA
I_{OZL} Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V					−50	μA
I_I Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V					1.0	mA
I_{IH} HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					50	μA
I_{IL} LOW-level input current	V_{CC} = MAX, V_I = 0.5V					−0.25	mA
I_{OS} Short-circuit output current[3]	V_{CC} = MAX			−40		−100	mA
I_{CC} Supply current (total)	V_{CC} = MAX	I_{CCL}	8TS805		105	160	mA
		I_{CCL}	All inputs grounded, 8TS806		102	140	mA
		I_{CCZ}	CP, $\overline{OE}$ = 4.5V D inputs = GND		131	180	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
4. V_{OL} = + 0.45V MAX for S8TS at T_A = + 125°C only.

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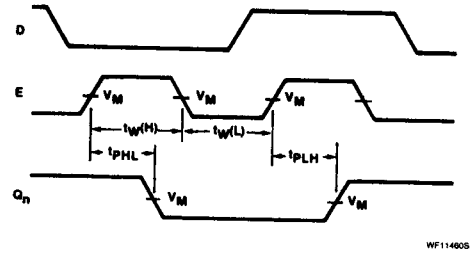
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

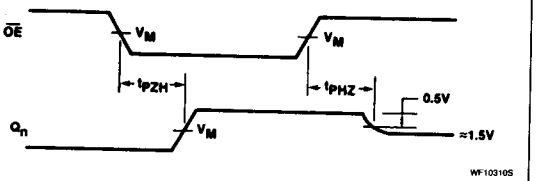
PARAMETER		TEST CONDITIONS	8TS		UNIT
			C_L = 15pF, R_L = 280Ω		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 6, 8TS806	75		MHz
t_{PLH} t_{PHL}	Propagation delay Latch enable to output	Waveform 1, 8TS805		14 18	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 4, 8TS805		9 13	ns
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 6, 8TS806		15 17	ns
t_{PZH}	Enable time to HIGH level	Waveform 2		15	ns
t_{PZL}	Enable time to LOW level	Waveform 3 8TS805 8TS806		18 18	ns
t_{PHZ}	Disable time from HIGH level	Waveform 2, C_L = 5pF		9	ns
t_{PLZ}	Disable time from LOW level	Waveform 3, C_L = 5pF		12	ns

NOTE:
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

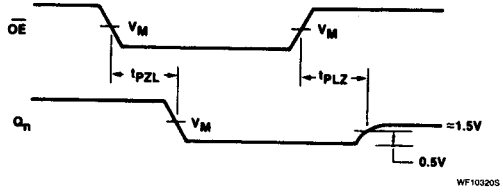
AC WAVEFORMS



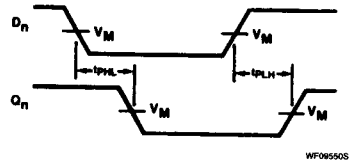
Waveform 1. Latch Enable To Output Delays And Latch Enable Pulse Width



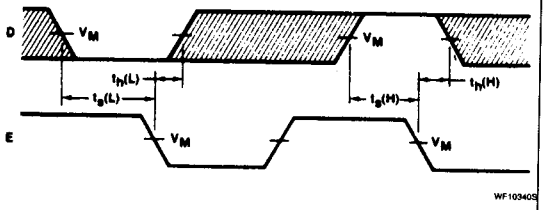
Waveform 2. 3-State Enable Time To High Level And Disable Time from High Level



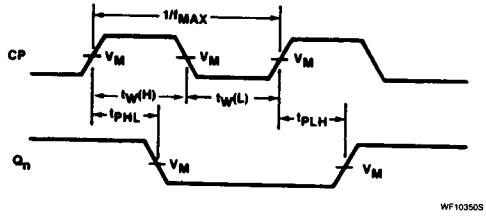
Waveform 3. 3-State Enable Time To Low Level And Disable Time From Low Level



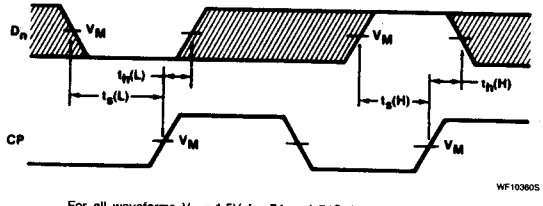
Waveform 4. Propagation Delay Data To Q Outputs



Waveform 5. Data Set-up And Hold Times



Waveform 6. Clock To Output Delays And Clock Pulse Width



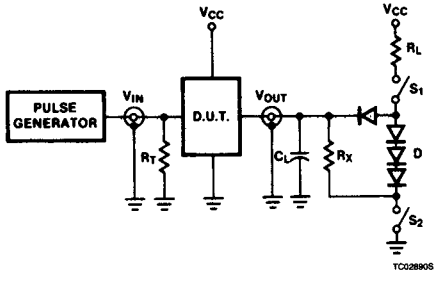
For all waveforms V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 7. Data Set-up And Hold Times

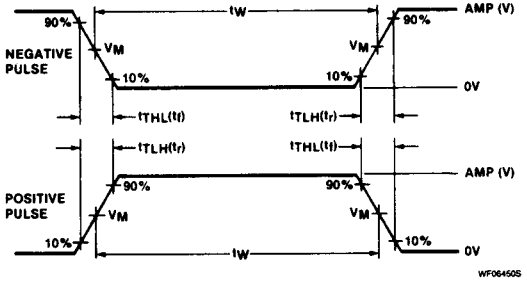
AC SET-UP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	8TS		UNIT
			Min	Max	
$t_{W(H)}$ $t_{W(L)}$	Latch enable pulse width	Waveform 1, 8TS805	6 7.3		ns
t_s	Set-up time, data to latch enable	Waveform 5, 8TS805	5		ns
t_h	Hold time, data to latch enable	Waveform 5, 8TS805	10		ns
$t_{W(H)}$ $t_{W(L)}$	Clock pulse width	Waveform 6, 8TS806	6 7.3		ns
t_s	Set-up time, data to clock	Waveform 7, 8TS806	5		ns
t_h	Hold time, data to clock	Waveform 7, 8TS806	4		ns

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 3-State Outputs



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
8T	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

R_X = 1kΩ for 74, 74S, R_X = 5kΩ for 74LS.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.