

18-Bit universal bus transceiver; 3-state

74ALVCH16600

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Universal bus transceiver with D-type latches and D-type Flip-flops capable of operating in transparent, latched, clocked or clocked-enabled mode.
- All inputs have bushold circuitry
- Output drive capability 50Ω transmission lines @ 85 °C
- 3-state non-inverting outputs for bus oriented applications

DESCRIPTION

The 74ALVCH16600 is an 18-bit universal bus transceiver. Data flow in each direction is controlled by output enable (\overline{OE}_{AB} , \overline{OE}_{BA}), latch-enable (LE_{AB} , LE_{BA}) and clock inputs (\overline{CP}_{AB} , \overline{CP}_{BA}). The clock enable inputs (\overline{CE}_{AB} , \overline{CE}_{BA}) control the clock. When LE_{AB} is HIGH, the A-B dataflow is transparent. When LE_{AB} is LOW, and \overline{CP}_{AB} is held at LOW or HIGH, the A data is latched; on the HIGH-to-LOW transition of \overline{CP}_{AB} the A-data is stored in the latch/flip-flop. The outputs are active when \overline{OE}_{AB} is LOW. When \overline{OE}_{AB} is LOW the B-outputs are in 3-state. Similarly, the LE_{BA} , \overline{OE}_{BA} and \overline{CP}_{BA} control the B-to-A dataflow.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^\circ\text{C}$; $t_r = t_f = 2.5\text{ ns}$

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | UNIT |
|-------------------|---|---|---------|------|
| t_{PHL}/t_{PLH} | propagation delay | $C_L = 50\text{ pF}$ $V_{CC} = 3.3\text{ V}$ | 3.0 | ns |
| | A_n to B_n LE_{AB} to A_n | | 3.2 | |
| C_I | input capacitance | | 5.0 | pF |
| C_{VO} | input/output capacitance | | 10 | pF |
| C_{PD} | power dissipation capacitance per latch | notes 1 and 2 | 22 | pF |

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is $V_i = \text{GND to } V_{CC}$.

ORDERING INFORMATION

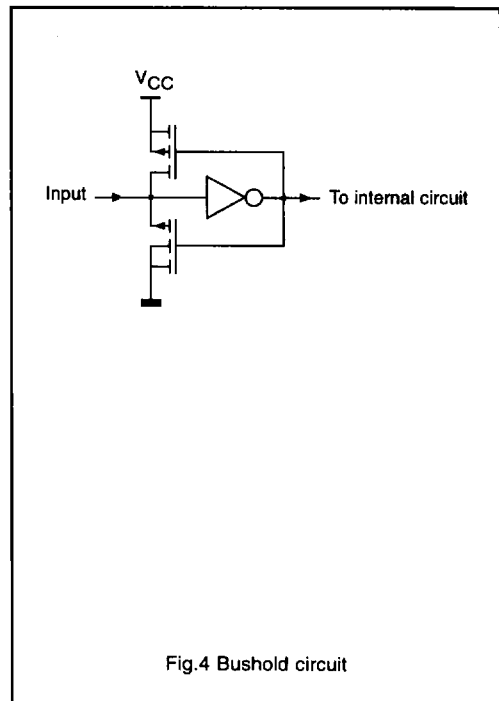
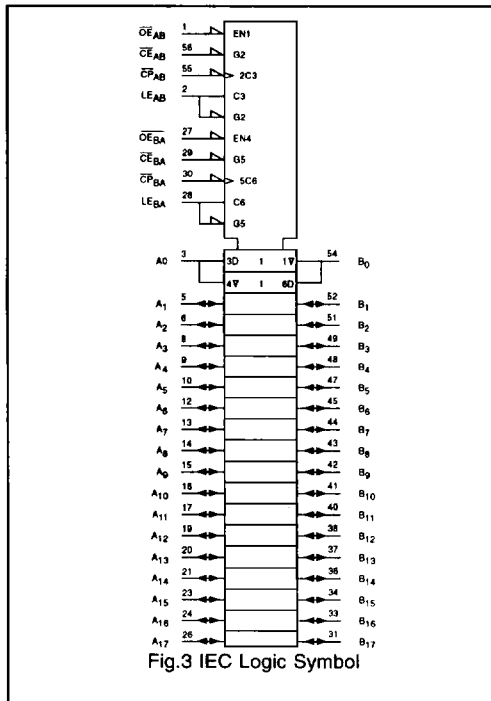
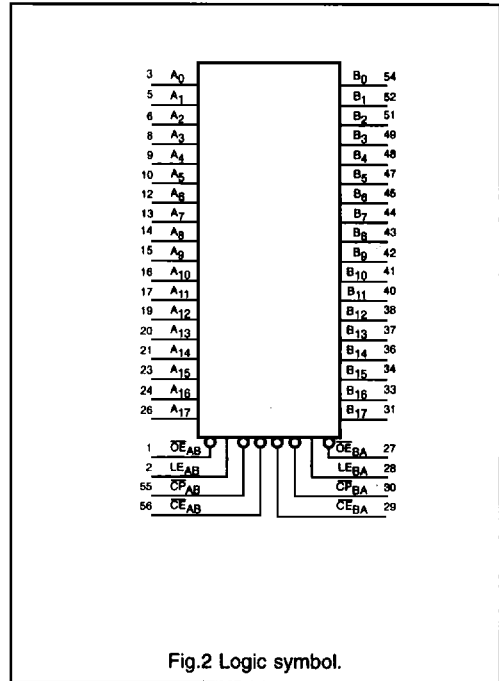
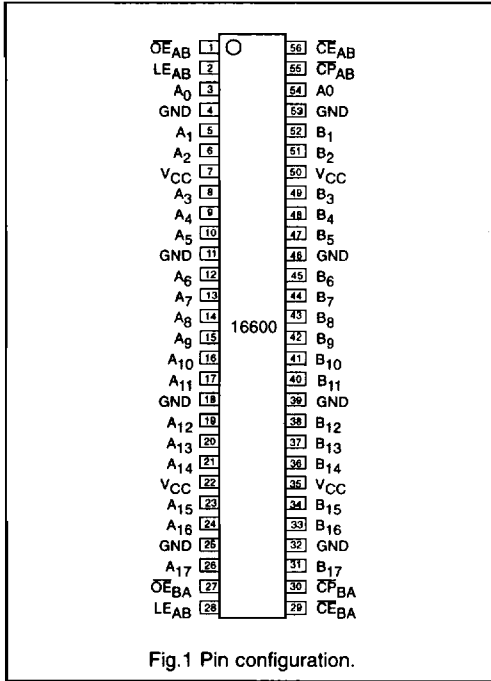
| TYPE NUMBER | PACKAGES | | | |
|-----------------|----------|---------|----------|----------|
| | PINS | PACKAGE | MATERIAL | CODE |
| 74ALVCH16600DL | 56 | SSOP56 | plastic | SOT371-1 |
| 74ALVCH16600DGG | 56 | TSSOP56 | plastic | SOT364-1 |

PINNING

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|--|----------------------|---------------------------------|
| 1 | \overline{OE}_{AB} | Output enable A-to-B |
| 2 | LE_{AB} | Latch enable A-to-B |
| 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26 | A_0 to A_{17} | 'A' data inputs/outputs |
| 4, 11, 18, 25, 29, 32, 39, 46, 53, 56 | GND | ground (0 V) |
| 7, 22, 35, 50 | V_{CC} | positive supply voltage |
| 27 | \overline{OE}_{BA} | Output enable B-to-A |
| 28 | LE_{BA} | Latch enable B-to-A |
| 30 | \overline{CP}_{BA} | Clock input B-to-A, HIGH-to-LOW |
| 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31 | B_0 to B_{17} | 'B' data inputs/outputs |
| 55 | \overline{CP}_{AB} | Clock input A-to-B, HIGH-to-LOW |
| 29 | \overline{CE}_{BA} | Clock enable B-to-A |
| 56 | \overline{CE}_{AB} | Clock enable A-to-B |

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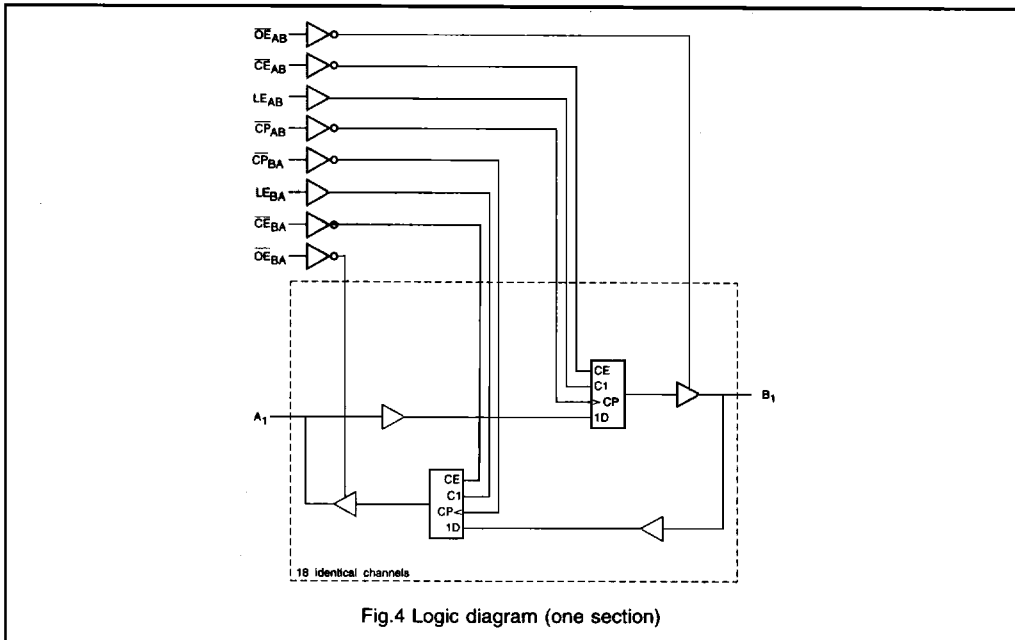


Fig.4 Logic diagram (one section)

FUNCTION TABLE

| INPUTS | | | | DATA | OUTPUTS | STATUS |
|----------------------|----------------------|-----------|----------------------|------|---------|------------------|
| \overline{CE}_{xx} | \overline{OE}_{xx} | LE_{xx} | \overline{CP}_{xx} | | | |
| X | H | X | X | X | Z | Disabled |
| X | L | H | X | H | H | Transparent |
| X | L | H | X | L | L | |
| H | L | L | X | X | NC | Hold |
| H | L | L | X | X | NC1 | |
| L | L | L | ↓ | h | Z | Disabled + latch |
| L | L | L | ↓ | l | Z | |
| L | L | L | ↓ | h | H | Latch + display |
| L | L | L | ↓ | l | L | |
| L | L | L | H | X | NC | Hold |
| L | L | L | L | X | NC1 | |

XX = AB for A-to-B direction, BA for B-to-A direction

H = HIGH voltage level

L = LOW voltage level

h = High state must be present one setup time before the low-to-high transition of \overline{CP}_{xx}

l = Low state must be present one setup time before the low-to-high transition of \overline{CP}_{xx}

X = Don't care

↓ = HIGH-to-LOW level transition

NC = No change

NC1 = No change provided that \overline{CP}_{xx} was LOW before LE_{xx} went low

Z = High impedance "off" state

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DC CHARACTERISTICS FOR 74ALVCH16600

For the DC characteristics see chapter "ALVCH family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74ALVCH16600

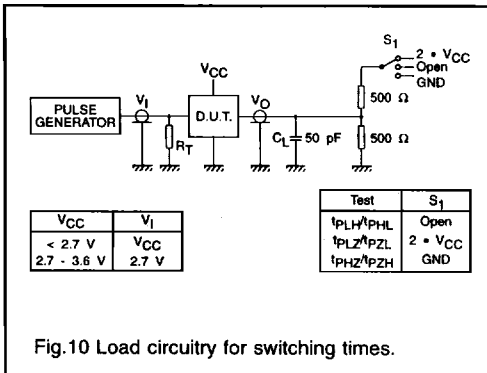
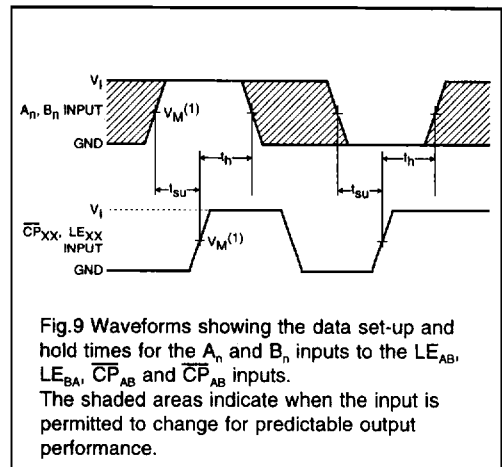
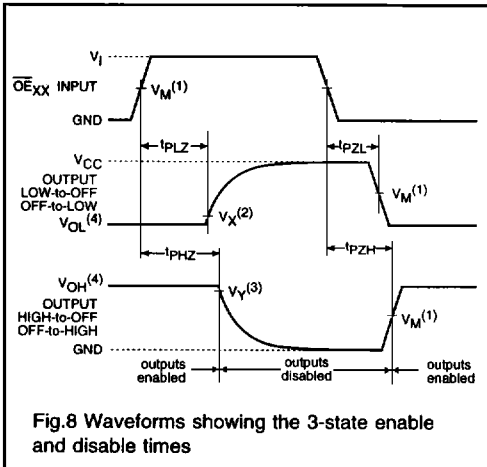
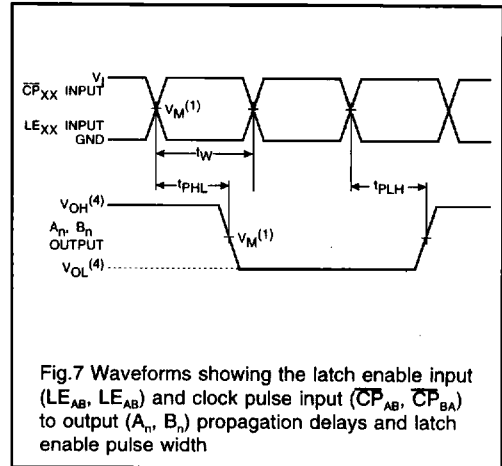
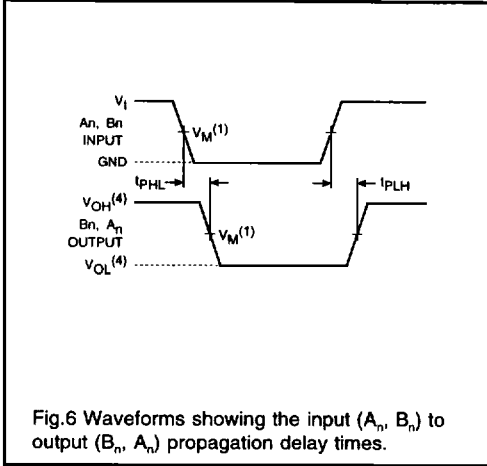
GND = 0 V; $t_r = t_f = 2.5$ ns; $C_L = 50$ pF

| SYMBOL | PARAMETER | T_{amb} (°C) | | | UNIT | TEST CONDITIONS | |
|-------------------|--|----------------|------|------|------|-----------------|-----------|
| | | -40 to +85 | | | | V_{CC} (V) | WAVEFORMS |
| | | MIN. | TYP. | MAX. | | | |
| t_{PHL}/t_{PLH} | propagation delay A_n to B_n , B_n to A_n | - | - | 18.0 | ns | 1.2 | Fig.6 |
| | | - | - | 4.8 | | 2.7 | |
| | | - | 3.0* | 4.4 | | 3.0 to 3.6 | |
| t_{PHL}/t_{PLH} | propagation delay LE_{BA} to A_n , LE_{AB} to B_n | - | - | 20.0 | ns | 1.2 | Fig.7 |
| | | - | - | 6.0 | | 2.7 | |
| | | - | 3.2* | 5.4 | | 3.0 to 3.6 | |
| t_{PHL}/t_{PLH} | propagation delay \overline{CP}_{BA} to A_n , \overline{CP}_{AB} to B_n | - | - | 20.0 | ns | 1.2 | Fig.7 |
| | | - | - | 6.0 | | 2.7 | |
| | | - | 3.2* | 5.4 | | 3.0 to 3.6 | |
| t_{PHZ}/t_{PLZ} | 3-state output enable time \overline{OE}_{BA} to A_n , \overline{OE}_{AB} to B_n | - | - | 22.0 | ns | 1.2 | Fig.8 |
| | | - | - | 6.1 | | 2.7 | |
| | | - | - | 5.5 | | 3.0 to 3.6 | |
| t_{PHZ}/t_{PLZ} | 3-state output disable time \overline{OE}_{BA} to A_n , \overline{OE}_{AB} to B_n | - | - | 22.0 | ns | 1.2 | Fig.8 |
| | | - | - | 6.1 | | 2.7 | |
| | | - | - | 5.5 | | 3.0 to 3.6 | |

| SYMBOL | PARAMETER | T_{amb} (°C) | | | UNIT | TEST CONDITIONS | | |
|--|---|----------------------|------|------------|------------|-----------------|-----------|-----|
| | | -40 to +85 | | | | V_{CC} (V) | WAVEFORMS | |
| | | MIN. | TYP. | MAX. | | | | |
| t_w | LE pulse width, LE_{AB} or LE_{BA} HIGH | - | - | - | ns | 1.2 | Fig. 7 | |
| | | 2.5 | - | - | | 2.7 to 3.6 | | |
| | | - | - | - | | 1.2 | | |
| t_{su} | LE pulse width, \overline{CP}_{AB} or \overline{CP}_{BA} HIGH or LOW | 2.5 | - | - | ns | 2.7 to 3.6 | Fig.9 | |
| | | - | - | - | | 1.2 | | |
| | | - | - | - | | 2.7 to 3.6 | | |
| t_{su} | set-up time, A_n before $\overline{CP}_{AB} \downarrow$ | - | - | - | ns | 1.2 | Fig.9 | |
| | | 3 | - | - | | 2.7 to 3.6 | | |
| | set-up time, B_n before $\overline{CP}_{AB} \downarrow$ | - | - | - | ns | 1.2 | | |
| | | 3 | - | - | | 2.7 to 3.6 | | |
| | set-up time, A_n before $LE_{AB} \downarrow$ B_n before $LE_{AB} \downarrow$ | \overline{CP} high | - | - | - | ns | | 1.2 |
| | | 1.5 | - | - | 2.7 to 3.6 | | | |
| set-up time, A_n before $LE_{AB} \downarrow$ B_n before $LE_{AB} \downarrow$ | \overline{CP} low | - | - | - | ns | 1.2 | | |
| | 1.5 | - | - | 2.7 to 3.6 | | | | |
| t_h | hold time, A_n after $\overline{CP}_{AB} \downarrow$ or B_n before $\overline{CP}_{AB} \downarrow$ | - | - | - | ns | 1.2 | | |
| | | 0 | - | - | | 2.7 to 3.6 | | |
| t_h | hold time, A_n after $LE_{AB} \downarrow$ or B_n before $LE_{BA} \downarrow$ | - | - | - | ns | 1.2 | | |
| | | 1 | - | - | | 2.7 to 3.6 | | |

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS



- Notes:
- $V_M = 1.5 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$
 - $V_X = V_{OL} + 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$
 - $V_Y = V_{OH} - 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$
 - V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.