# 3.3V Octal transparent latch (3-State) 74LVT373

## FEATURES

- Designed for use in the 3.3V high-performance market
- Supports mixed-mode signal operation; 5V input and output voltages with 3.3V $V_{CC}$
- Bus-hold inputs eliminate the need for external pull-up resistors to hold unused pins
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- 8-bit transparent latch
- 3-State output buffers
- Zero-static power dissipation
- Pin and function compatibility with ABT
- AC and DC performance compatibility with ABT
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

## DESCRIPTION

The 74LVT373 device is designed specifically for low-voltage (3.3V) $V_{CC}$ operation, but can provide a TTL interface to a 5V system environment.

The 74LVT373 high-performance BiCMOS device combines zero static and low dynamic power dissipation with high speed and high output drive.

The 74LVT373 device is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS $T_{amb}$ = 25°C; GND = 0V | TYPICAL | UNIT |
|---|---|---|---|---|
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>Dn to Qn | $C_L$ = 50pF; $V_{CC}$ = 3.3V | 2.5<br>2.7 | ns |
| $C_{IN}$ | Input capacitance | $V_I$ = 0V or $V_{CC}$ | 4 | pF |
| $C_{OUT}$ | Output capacitance | $V_I$ = 0V or $V_{CC}$ | 7 | pF |
| $I_{CCZ}$ | Total supply current | Outputs disabled; $V_{CC}$ =5.5V | 0.13 | mA |

## ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | DWG NUMBER |
|---|---|---|---|---|
| 20-Pin Plastic SOL | –40°C to +85°C | 74LVT373 D | 74LVT373 D | SOT163-1 |
| 20-Pin Plastic SSOP Type II | –40°C to +85°C | 74LVT373 DB | 74LVT373 DB | SOT339-1 |
| 20-Pin Plastic TSSOP Type I | –40°C to +85°C | 74LVT373 PW | 74LVT373PW DH | SOT360-1 |

## PIN DESCRIPTION

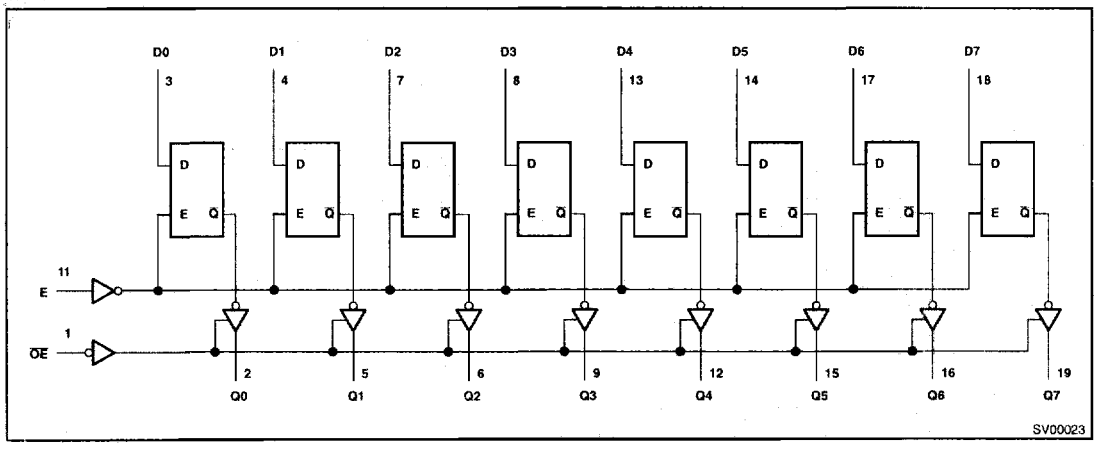
| PIN NUMBER | SYMBOL | FUNCTION |
|---|---|---|
| 1 | $\overline{OE}$ | Output enable input (active-Low) |
| 3, 4, 7, 8, 13, 14, 17, 18 | D0-D7 | Data inputs |
| 2, 5, 6, 9, 12, 15, 16, 19 | Q0-Q7 | Data outputs |
| 11 | E | Enable input (active-High) |
| 10 | GND | Ground (0V) |
| 20 | $V_{CC}$ | Positive supply voltage |

## FUNCTION TABLE

| INPUTS | | | INTERNAL REGISTER | OUTPUTS | OPERATING MODE |
|---|---|---|---|---|---|
| $\overline{OE}$ | E | Dn | | Q0 - Q7 | |
| L<br>L | ↓<br>↓ | l<br>h | L<br>H | L<br>H | Latch and read register |
| L | L | X | NC | NC | Hold |
| H<br>H | L<br>H | X<br>Dn | NC<br>Dn | Z<br>Z | Disable outputs |

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC = No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

## LOGIC DIAGRAM



## ABSOLUTE MAXIMUM RATINGS[1, 2]

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | DC supply voltage | | −0.5 to +4.6 | V |
| $I_{IK}$ | DC input diode current | $V_I < 0$ | −50 | mA |
| $V_I$ | DC input voltage[3] | | −0.5 to +7.0 | V |
| $I_{OK}$ | DC output diode current | $V_O < 0$ | −50 | mA |
| $V_{OUT}$ | DC output voltage[3] | output in Off or High state | −0.5 to +7.0 | V |
| $I_{OUT}$ | DC output current | output in Low state | 128 | mA |
| $I_{OUT}$ | DC output current | output in High state | −64 | mA |
| $T_{stg}$ | Storage temperature range | | −65 to 150 | °C |

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | UNIT |
|---|---|---|---|---|
| | | Min | Max | |
| $V_{CC}$ | DC supply voltage | 2.7 | 3.6 | V |
| $V_I$ | Input voltage | 0 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2.0 | | V |
| $V_{IL}$ | Input voltage | | 0.8 | V |
| $I_{OH}$ | High-level output current | | −32 | mA |
| $I_{OL}$ | Low-level output current | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | 0 | 10 | ns/V |
| $T_{amb}$ | Operating free-air temperature range | −40 | +85 | °C |

## DC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS | | LIMITS Temp = -40°C to +85°C MIN | TYP[1] | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = 2.7V; $I_{IK}$ = –18mA | | | | –1.2 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = 2.7 to 3.6V; $I_{OH}$ = –100µA | | $V_{CC}$-0.2 | | | V |
| | | $V_{CC}$ = 2.7V; $I_{OH}$ = –8mA | | 2.4 | | | |
| | | $V_{CC}$ = 3.0V; $I_{OH}$ = –32mA | | 2.0 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = 2.7V; $I_{OL}$ = 100µA | | | | 0.2 | V |
| | | $V_{CC}$ = 2.7V; $I_{OL}$ = 24mA | | | | 0.5 | |
| | | $V_{CC}$ = 3.0V; $I_{OL}$ = 16mA | | | | 0.4 | |
| | | $V_{CC}$ = 3.0V; $I_{OL}$ = 32mA | | | | 0.5 | |
| | | $V_{CC}$ = 3.0V; $I_{OL}$ = 64mA | | | | 0.55 | |
| $I_I$ | Input leakage current | $V_{CC}$ = 3.6V; $V_I$ = 5.5V | | | | 10 | µA |
| | | $V_{CC}$ = 0 or 3.6V; $V_I$ = $V_{CC}$ or GND | Control pins | | | ±1 | |
| | | $V_{CC}$ = 3.6V; $V_I$ = $V_{CC}$ | Data pins[4] | | | 1 | |
| | | $V_{CC}$ = 3.6V; $V_I$ = 0 | | | | -5 | |
| $I_{OFF}$ | Output off current | $V_{CC}$ = 0V; $V_I$ or $V_O$ = 0 to 4.5V | | | | ±100 | µA |
| $I_{HOLD}$ | Bus Hold current A or B ports | $V_{CC}$ = 3V; $V_I$ = 0.8V | | 75 | | | µA |
| | | $V_{CC}$ = 3V; $V_I$ = 2.0V | | –75 | | | µA |
| $I_{EX}$ | Current into an output in the High state when $V_O > V_{CC}$ | $V_O$ = 5.5V; $V_{CC}$ = 3.0V | | | | 125 | µA |
| $I_{PU/PD}$ | Power up/down 3-State output current[3] | $V_{CC} \leq$ 1.2V; $V_O$ = 0.5V to $V_{CC}$; $V_I$ = GND or $V_{CC}$; $\overline{OE}$/OE = X | | | | ±100 | µA |
| $I_{OZH}$ | 3-State output High current | $V_{CC}$ = 3.6; $V_O$ = 3V; $V_I$ = $V_{IL}$ or $V_{IH}$ | | | | 5 | µA |
| $I_{OZL}$ | 3-State output Low current | $V_{CC}$ = 3.6V; $V_O$ = 0.5V; $V_I$ = $V_{IL}$ or $V_{IH}$ | | | | –5 | µA |
| $I_{CCH}$ | Quiescent supply current | $V_{CC}$ = 3.6V; Outputs High, $V_I$ = GND or $V_{CC}$, $I_O$ = 0 | | | 0.13 | 0.19 | mA |
| $I_{CCL}$ | | $V_{CC}$ = 3.6V; Outputs Low, $V_I$ = GND or $V_{CC}$, $I_O$ = 0 | | | 3 | 12 | |
| $I_{CCZ}$ | | $V_{CC}$ = 3.6V; Outputs Disabled; $V_I$ = GND or $V_{CC}$, $I_O$ = 0 | | | 0.13 | 0.19 | |
| $\Delta I_{CC}$ | Additional supply current per input pin[2] | $V_{CC}$ = 3V to 3.6V; One input at $V_{CC}$-0.6V, Other inputs at $V_{CC}$ or GND | | | | 0.2 | mA |
| $C_I$ | Input capacitance | $V_I$ = 3V or 0 | | | 4 | | pF |
| $C_O$ | Output capacitance | $V_O$ = 3V or 0 | | | 8 | | pF |

**NOTES:**
1. All typical values are at $V_{CC}$ = 3.3V and $T_{amb}$ = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than $V_{CC}$ or GND
3. This parameter is valid for any $V_{CC}$ between 0V and 1.3V with a transition time of up to 10msec. From $V_{CC}$ = 1.3V to $V_{CC}$ = 3.3V ± 0.3V a transition time of 100µsec is permitted. X = Don't care. This parameter is valid for $T_{amb}$ = 25° C only.
4. Unused pins at $V_{CC}$ or GND.

## AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; $C_L$ = 50pF; $R_L$ = 500Ω, $T_{amb}$ = –40°C to +85°C.

| SYMBOL | PARAMETER | WAVEFORM | LIMITS $V_{CC}$ = 3.3V ±0.3V MIN | TYP[1] | MAX | $V_{CC}$ = 2.7V MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>Dn to Qn | 2 | 1.0<br>1.0 | 2.5<br>2.7 | 4.2<br>4.3 | 4.7<br>5.2 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>E to Qn | 1 | 1.6<br>2.5 | 3.5<br>4.3 | 5.6<br>6.5 | 6.3<br>7.2 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output enable time<br>$\overline{OE}$n to Qn | 4<br>5 | 1.0<br>1.3 | 2.8<br>3.3 | 5.1<br>5.5 | 6.2<br>6.6 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output disable time<br>$\overline{OE}$n to Qn | 4<br>5 | 2.0<br>1.5 | 3.7<br>3.0 | 5.7<br>4.6 | 6.7<br>5.1 | ns |

**NOTE:**
1. All typical values are at $V_{CC}$ = 3.3V and $T_{amb}$ = 25°C.

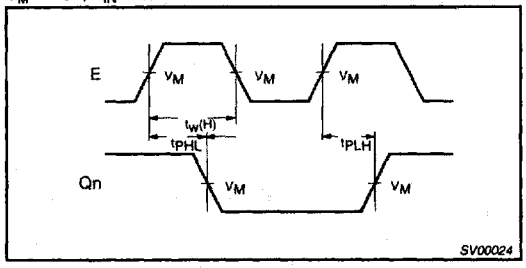
## AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; $C_L$ = 50pF; $R_L$ = 500Ω, $T_{amb}$ = –40°C to +85°C.

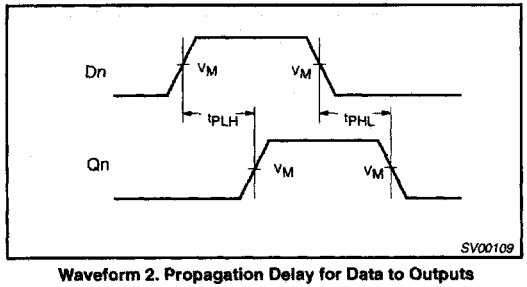
| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3V ±0.3V | | $V_{CC}$ = 2.7V | |
| | | | MIN | MAX | MAX | |
| $t_S(H)$<br>$t_S(L)$ | Setup time, High or Low, Dn to E | 3 | 0.7<br>0.7 | | 0.6<br>0.6 | ns |
| $t_H(H)$<br>$t_H(L)$ | Propagation delay<br>E to Qn | 3 | 1.6<br>1.6 | | 1.8<br>1.8 | ns |
| $t_W(H)$ | E pulse width High | 1 | 3.3 | | 3.3 | ns |

## AC WAVEFORMS

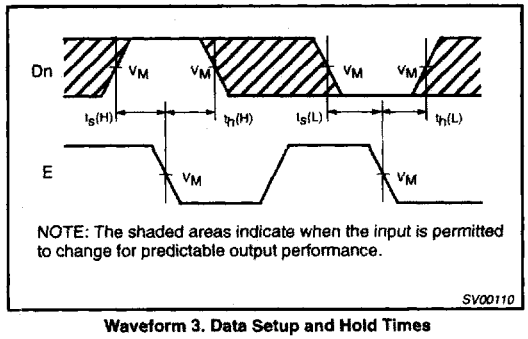
$V_M$ = 1.5V, $V_{IN}$ = GND to 3.0V



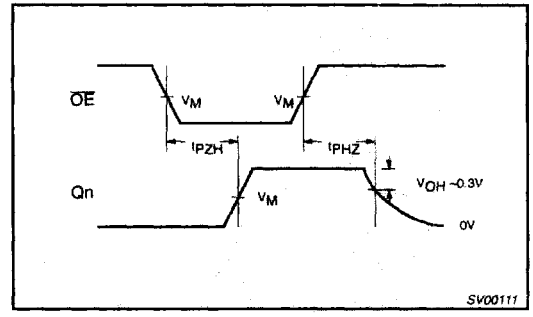

**Waveform 1. Propagation Delay, Enable to Output, and Enable Pulse Width**



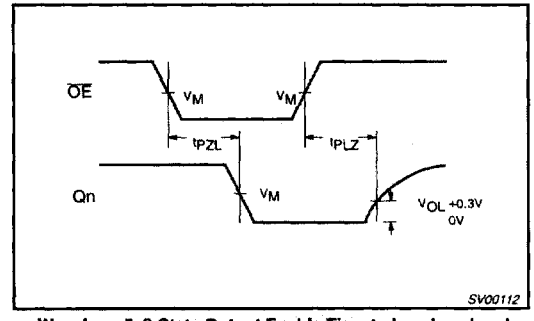

**Waveform 2. Propagation Delay for Data to Outputs**




**Waveform 3. Data Setup and Hold Times**

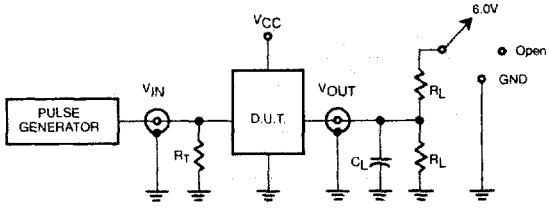



**Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level**

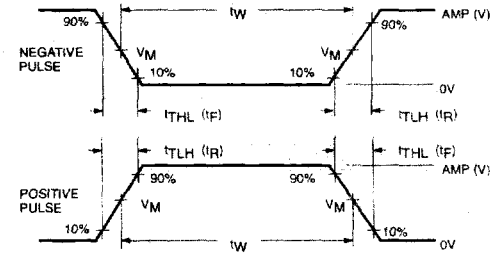



**Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level**

## TEST CIRCUIT AND WAVEFORM




*Test Circuit for 3-State Outputs*




$V_M$ = 1.5V
Input Pulse Definition

### SWITCH POSITION

| TEST | SWITCH |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6V |
| $t_{PHZ}/t_{PZH}$ | GND |

### DEFINITIONS

$R_L$ = Load resistor; see AC CHARACTERISTICS for value.

$C_L$ = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

$R_T$ = Termination resistance should be equal to $Z_{OUT}$ of pulse generators.

| FAMILY | INPUT PULSE REQUIREMENTS | | | | |
|---|---|---|---|---|---|
| | Amplitude | Rep. Rate | $t_W$ | $t_R$ | $t_F$ |
| 74LVT | 2.7V | ≤ 10MHz | 500ns | ≤ 2.5ns | ≤ 2.5ns |

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