



UTRON

Rev. 1.9

UT62L1024  
128KX8 BIT LOW POWER CMOS SRAM

REVISION HISTORY

| REVISION | DESCRIPTION   | DATE         |
|----------|---|--------------|
| Rev. 1.0 | Original  | Jun 01, 1997 |
| Rev. 1.1 | 128Kx 8 Low Voltage CMOS SRAM 之TN8106 body 已作fine tunings,將 $I_{SB1}$ 降為0.5uA(LL)、2uA(L)、Vcc range : 3.0V~3.6V  | Apr 05, 2000 |
| Rev. 1.2 | Add STSOP-I Package   | Aug 29, 2000 |
| Rev. 1.3 | Modify the format of power consumption  | Sep 01, 2000 |
| Rev. 1.4 | Add speed : -55ns   | Dec 01, 2000 |
| Rev. 1.5 | Vcc min 3.1→2.7V  | Mar 15, 2001 |
| Rev. 1.6 | 1. The symbols CE1# ,OE# & WE# are revised as $\overline{CE1}$ , $\overline{OE}$ & $\overline{WE}$<br>2. Add Icc value of 55ns range(access time)<br>3. $V_{OH}$ is revised as 2.2V<br>4. $I_{SB1}$ is revised as 100 $\mu$ A | Jun 26, 2001 |
| Rev. 1.7 | Revised 32 pin 8mmx13.4mm STSOP Package Outline Dimension   | Nov 26, 2001 |
| Rev. 1.8 | 1. $V_{OH}$ is revised as 2.4V (min.)<br>2. Revised Package Outline Dimension   | Apr 9, 2002  |
| Rev. 1.9 | 1. Add Operation temperature : Extended temp -20 ~80<br>2. Add Order information for lead free product  | May 09.2003  |



FEATURES

- Fast access time : 35/55/70ns (max.)
- Low power consumption :
  - Operating current : 40/35/30mA (typical)
  - Standby current : 2.5μA (typical) L-version  
0.5μA (typical) LL-version
- Power supply range : 2.7V to 3.6V
- Operating temperature :
  - Commercial : 0 ~70
  - Extended : -20 ~80
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Data retention voltage : 2V (min.)
- Package : 32-pin 600 mil PDIP  
32-pin 450 mil SOP  
32-pin 8x20 mm TSOP-1  
32-pin 8x13.4 mm STSOP

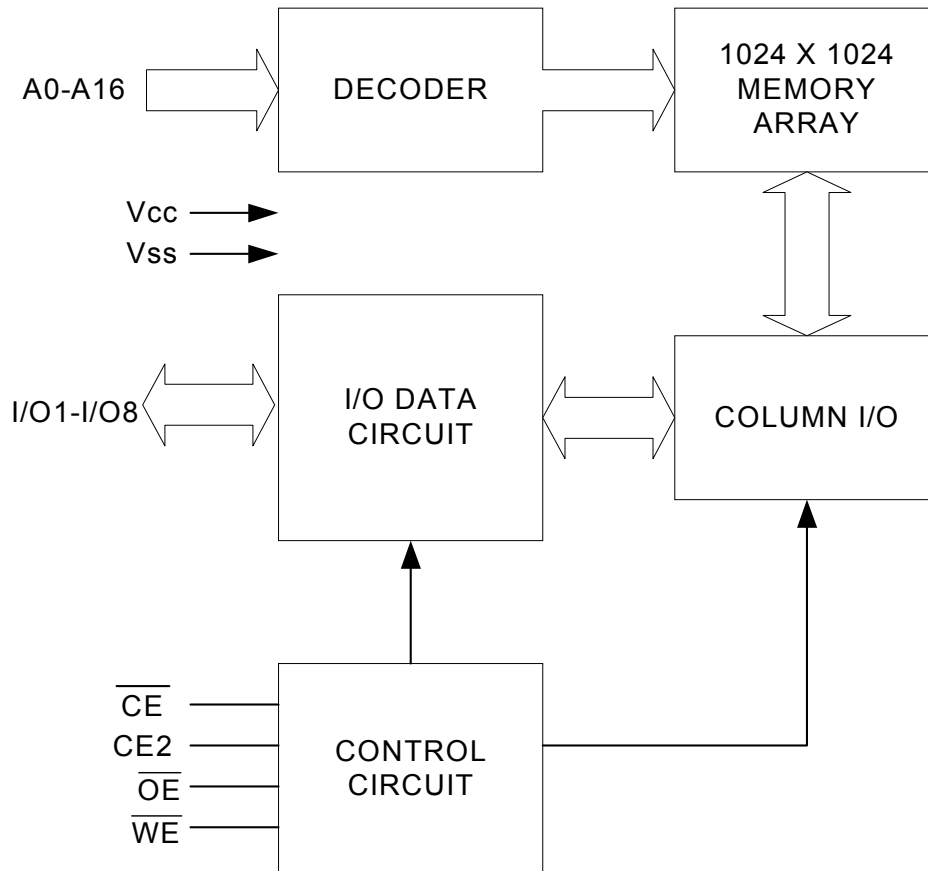
GENERAL DESCRIPTION

The UT62L1024 is a 1,048,576-bit low power CMOS static random access memory organized as 131,072 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

Easy memory expansion is provided by using two chip enable inputs.(  $\overline{CE}$  ,CE2) It is particularly well suited for battery back-up nonvolatile memory application.

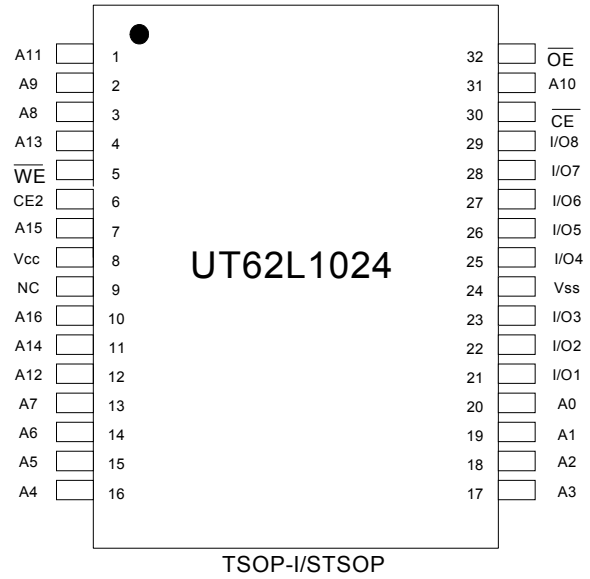
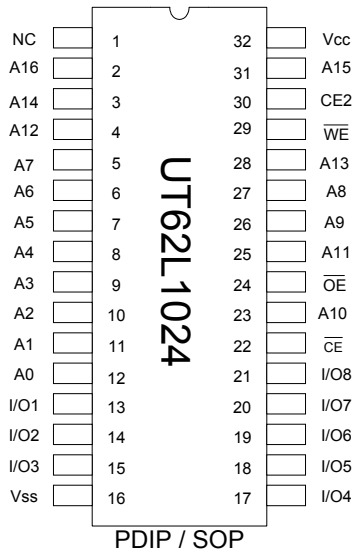
The UT62L1024 operates from a single 2.7V~ 3.6V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM





PIN CONFIGURATION



PIN DESCRIPTION

| SYMBOL                | DESCRIPTION            |
|-----------------------|------------------------|
| A0 - A16              | Address Inputs         |
| I/O1 - I/O8           | Data Inputs/Outputs    |
| $\overline{CE}$ , CE2 | Chip enable 1,2 Inputs |
| $\overline{WE}$       | Write Enable Input     |
| $\overline{OE}$       | Output Enable Input    |
| V <sub>CC</sub>       | Power Supply           |
| V <sub>SS</sub>       | Ground                 |
| NC                    | No Connection          |

**ABSOLUTE MAXIMUM RATINGS\***

| PARAMETER  | SYMBOL              | RATING         | UNIT       |
|--|---------------------|----------------|------------|
| Terminal Voltage with Respect to V <sub>SS</sub> | V <sub>TERM</sub>   | -0.5 to +4.6   | V          |
| Operating Temperature                            | Commerical          | T <sub>A</sub> | 0 to +70   |
|  | Extended            | T <sub>A</sub> | -20 to +80 |
| Storage Temperature                              | T <sub>STG</sub>    | -65 to +150    |            |
| Power Dissipation                                | P <sub>D</sub>      | 1              | W          |
| DC Output Current                                | I <sub>OUT</sub>    | 50             | mA         |
| Soldering Temperature (under 10 sec)             | T <sub>solder</sub> | 260            |            |

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

**TRUTH TABLE**

| MODE           | $\overline{CE}$ | CE2 | $\overline{OE}$ | $\overline{WE}$ | I/O OPERATION    | SUPPLY CURRENT                     |
|----------------|-----------------|-----|-----------------|-----------------|------------------|------------------------------------|
| Standby        | H               | X   | X               | X               | High - Z         | I <sub>SB</sub> , I <sub>SB1</sub> |
| Standby        | X               | L   | X               | X               | High - Z         | I <sub>SB</sub> , I <sub>SB1</sub> |
| Output Disable | L               | H   | H               | H               | High - Z         | I <sub>CC</sub> , I <sub>CC1</sub> |
| Read           | L               | H   | L               | H               | D <sub>OUT</sub> | I <sub>CC</sub> , I <sub>CC1</sub> |
| Write          | L               | H   | X               | L               | D <sub>IN</sub>  | I <sub>CC</sub> , I <sub>CC1</sub> |

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.

**DC ELECTRICAL CHARACTERISTICS** (V<sub>CC</sub> = 2.7V~3.6V, T<sub>A</sub> = 0 to +70 / -20 to +80 (E))

| PARAMETER                              | SYMBOL                        | TEST CONDITION   | MIN.             | TYP.   | MAX.                 | UNIT |     |                         |    |
|--|-------------------------------|--|------------------|--|----------------------|------|-----|-------------------------|----|
| Input High Voltage                     | V <sub>IH</sub> <sup>*1</sup> |  | 2.0              | -  | V <sub>CC</sub> +0.5 | V    |     |                         |    |
| Input Low Voltage                      | V <sub>IL</sub> <sup>*2</sup> |  | - 0.5            | -  | 0.6                  | V    |     |                         |    |
| Input Leakage Current                  | I <sub>IL</sub>               | V <sub>SS</sub> V <sub>IN</sub> V <sub>CC</sub>  | - 1              | -  | 1                    | μA   |     |                         |    |
| Output Leakage Current                 | I <sub>OL</sub>               | V <sub>SS</sub> V <sub>I/O</sub> V <sub>CC</sub><br>$\overline{CE} = V_{IH}$ or CE2 = V <sub>IL</sub> or<br>$\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ | - 1              | -  | 1                    | μA   |     |                         |    |
| Output High Voltage                    | V <sub>OH</sub>               | I <sub>OH</sub> = - 1mA  | 2.4              | -  | -                    | V    |     |                         |    |
| Output Low Voltage                     | V <sub>OL</sub>               | I <sub>OL</sub> = 4mA  | -                | -  | 0.4                  | V    |     |                         |    |
| Average Operating Power Supply Current | I <sub>CC</sub>               | Cycle time = Min. 100% Duty,<br>$\overline{CE} = V_{IL}$ , CE2 = V <sub>IH</sub> ,<br>I <sub>I/O</sub> = 0mA   | 35               | -  | 40                   | 60   | mA  |                         |    |
|  |                               |  | 55               | -  | 35                   | 50   | mA  |                         |    |
|  |                               |  | 70               | -  | 30                   | 40   | mA  |                         |    |
|  | I <sub>CC1</sub>              | Cycle time = 1μs, 100% Duty,<br>$\overline{CE} = 0.2V$ , CE2 = V <sub>CC</sub> -0.2V,<br>I <sub>I/O</sub> = 0mA  | -                | -  | 5                    | mA   |     |                         |    |
| Standby Power Supply Current           | I <sub>SB</sub>               | $\overline{CE} = V_{IH}$ or CE2 = V <sub>IL</sub>  | -                | -  | 1.0                  | mA   |     |                         |    |
|  |                               |  | I <sub>SB1</sub> | $\overline{CE} = V_{CC}-0.2V$ or<br>CE2 = 0.2V | - L                  | -    | 2.5 | 100<br>20 <sup>*4</sup> | μA |
|  |                               |  |                  |  | - LL                 | -    | 0.5 | 40<br>10 <sup>*4</sup>  | μA |

Notes:

1. Overshoot : V<sub>CC</sub>+3.0v for pulse width less than 10ns.
2. Undershoot : V<sub>SS</sub>-3.0v for pulse width less than 10ns.
3. Overshoot and Undershoot are sampled, not 100% tested.
4. Those parameters are for reference only under 50□

**CAPACITANCE** ( $T_A=25$  ,  $f=1.0\text{MHz}$ )

| PARAMETER                | SYMBOL    | MIN. | MAX. | UNIT |
|--------------------------|-----------|------|------|------|
| Input Capacitance        | $C_{IN}$  | -    | 6    | pF   |
| Input/Output Capacitance | $C_{I/O}$ | -    | 8    | pF   |

Note : These parameters are guaranteed by device characterization, but not production tested.

**AC TEST CONDITIONS**

|  |  |
|--|--|
| Input Pulse Levels                       | 0.4V to 2.4V   |
| Input Rise and Fall Times                | 5ns  |
| Input and Output Timing Reference Levels | 1.5V   |
| Output Load                              | $C_L=50\text{pF}$ , $I_{OH}/I_{OL}=-1\text{mA}/2\text{mA}$ |

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 2.7\text{V}\sim 3.6\text{V}$  ,  $T_A = 0$  to  $+70$  /  $-20$  to  $+80$  (E))**(1) READ CYCLE**

| PARAMETER                          | SYMBOL      | UT62L1024-35 |      | UT62L1024-55 |      | UT62L1024-70 |      | UNIT |
|------------------------------------|-------------|--------------|------|--------------|------|--------------|------|------|
|                                    |             | MIN.         | MAX. | MIN.         | MAX. | MIN.         | MAX. |      |
| Read Cycle Time                    | $t_{RC}$    | 35           | -    | 55           | -    | 70           | -    | ns   |
| Address Access Time                | $t_{AA}$    | -            | 35   | -            | 55   | -            | 70   | ns   |
| Chip Enable Access Time            | $t_{ACE}$   | -            | 35   | -            | 55   | -            | 70   | ns   |
| Output Enable Access Time          | $t_{OE}$    | -            | 25   | -            | 30   | -            | 35   | ns   |
| Chip Enable to Output in Low-Z     | $t_{CLZ}^*$ | 10           | -    | 10           | -    | 10           | -    | ns   |
| Output Enable to Output in Low-Z   | $t_{OLZ}^*$ | 5            | -    | 5            | -    | 5            | -    | ns   |
| Chip Disable to Output in High-Z   | $t_{CHZ}^*$ | -            | 25   | -            | 30   | -            | 35   | ns   |
| Output Disable to Output in High-Z | $t_{OHZ}^*$ | -            | 25   | -            | 30   | -            | 35   | ns   |
| Output Hold from Address Change    | $t_{OH}$    | 5            | -    | 5            | -    | 5            | -    | ns   |

**(2) WRITE CYCLE**

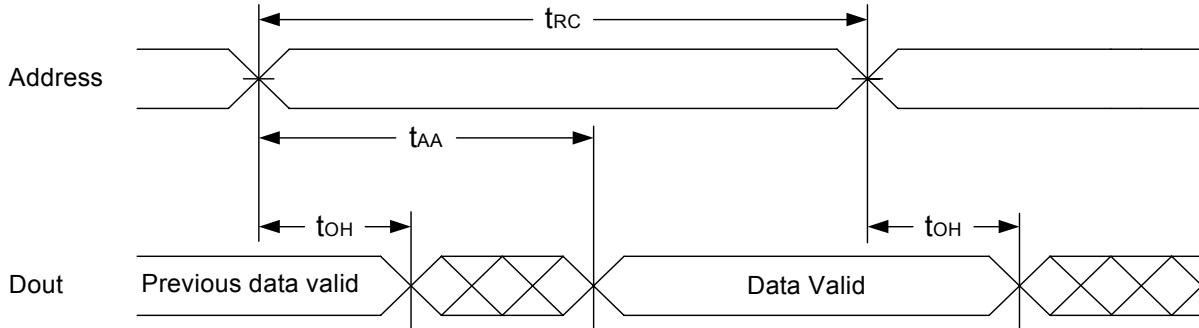
| PARAMETER                        | SYMBOL      | UT62L1024-35 |      | UT62L1024-55 |      | UT62L1024-70 |      | UNIT |
|----------------------------------|-------------|--------------|------|--------------|------|--------------|------|------|
|                                  |             | MIN.         | MAX. | MIN.         | MAX. | MIN.         | MAX. |      |
| Write Cycle Time                 | $t_{WC}$    | 35           | -    | 55           | -    | 70           | -    | ns   |
| Address Valid to End of Write    | $t_{AW}$    | 30           | -    | 50           | -    | 60           | -    | ns   |
| Chip Enable to End of Write      | $t_{CW}$    | 30           | -    | 50           | -    | 60           | -    | ns   |
| Address Set-up Time              | $t_{AS}$    | 0            | -    | 0            | -    | 0            | -    | ns   |
| Write Pulse Width                | $t_{WP}$    | 25           | -    | 40           | -    | 45           | -    | ns   |
| Write Recovery Time              | $t_{WR}$    | 0            | -    | 0            | -    | 0            | -    | ns   |
| Data to Write Time Overlap       | $t_{DW}$    | 20           | -    | 25           | -    | 30           | -    | ns   |
| Data Hold from End of Write-Time | $t_{DH}$    | 0            | -    | 0            | -    | 0            | -    | ns   |
| Output Active from End of Write  | $t_{OW}^*$  | 5            | -    | 5            | -    | 5            | -    | ns   |
| Write to Output in High-Z        | $t_{WHZ}^*$ | -            | 15   | -            | 20   | -            | 25   | ns   |

\*These parameters are guaranteed by device characterization, but not production tested.

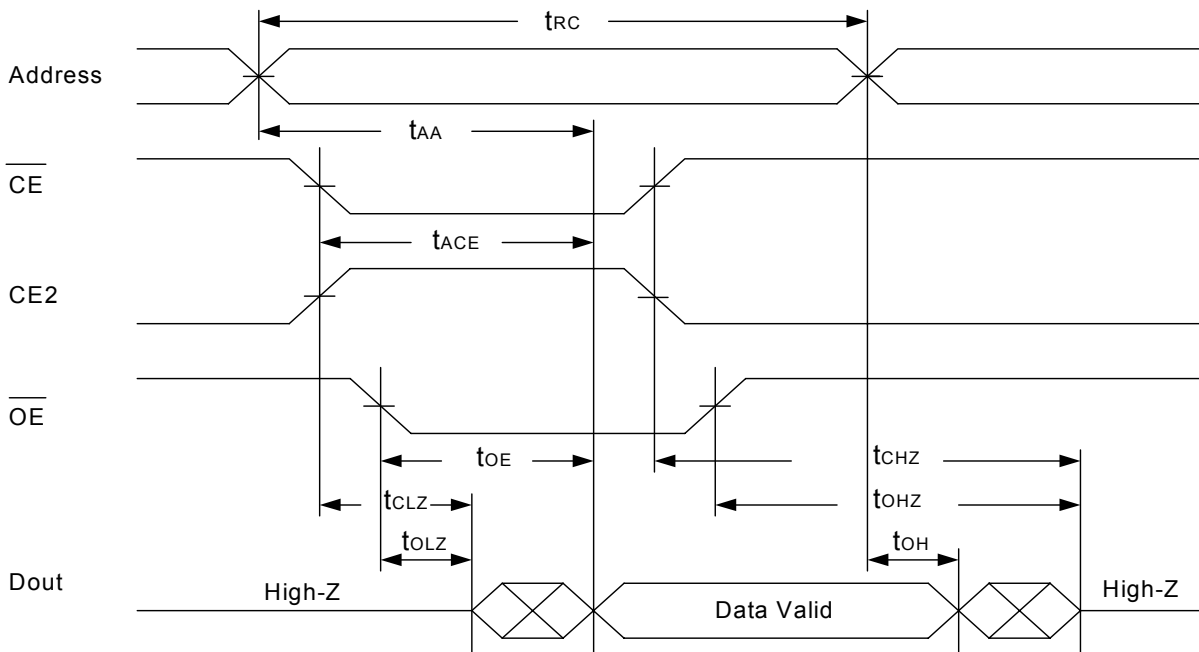


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 ( $\overline{CE}$  and CE2 and  $\overline{OE}$  Controlled) (1,3,4,5)

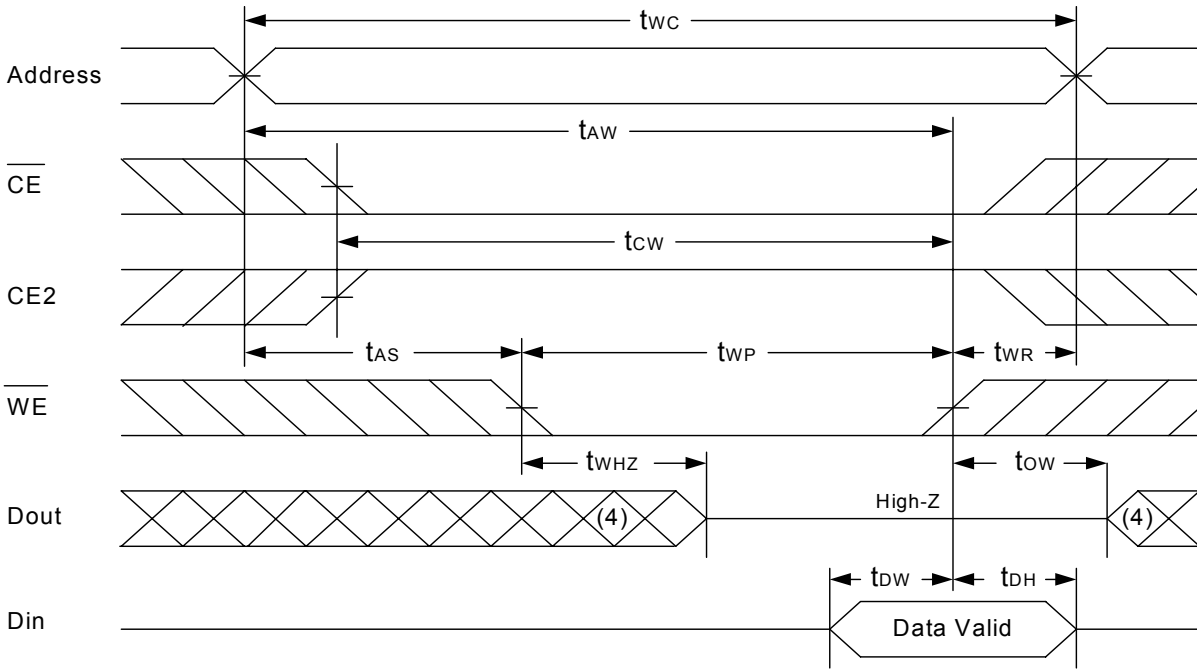


Notes :

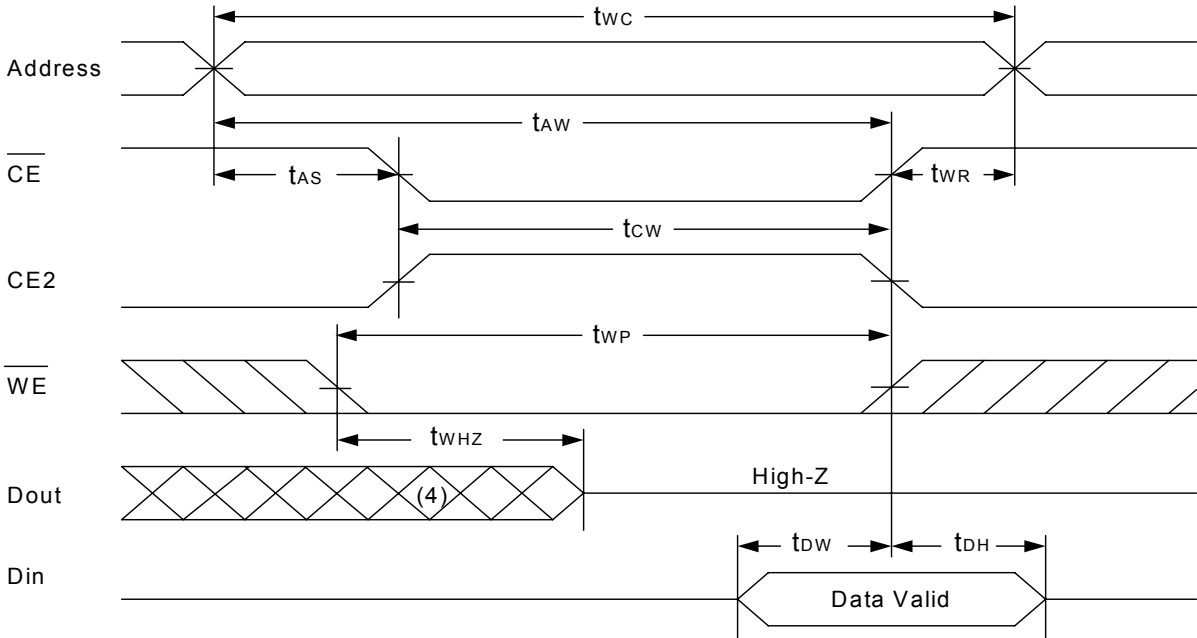
1.  $\overline{WE}$  is high for read cycle.
2. Device is continuously selected  $\overline{OE}$  =low,  $\overline{CE}$  =low, CE2=high.
3. Address must be valid prior to or coincident with  $\overline{CE}$  =low, CE2=high; otherwise  $t_{AA}$  is the limiting parameter.
4.  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$  and  $t_{OHZ}$  are specified with  $C_L=5pF$ . Transition is measured  $\pm 500mV$  from steady state.
5. At any given temperature and voltage condition,  $t_{CHZ}$  is less than  $t_{CLZ}$ ,  $t_{OHZ}$  is less than  $t_{OLZ}$ .



**WRITE CYCLE 1** ( $\overline{WE}$  Controlled) (1,2,3,5,6)



**WRITE CYCLE 2** ( $\overline{CE}$  and  $\overline{CE2}$  Controlled) (1,2,5,6)





Notes :

1.  $\overline{WE}$ ,  $\overline{CE}$  must be high or  $\overline{CE2}$  must be low during all address transitions.
2. A write occurs during the overlap of a low  $\overline{CE}$ , high  $\overline{CE2}$ , low  $\overline{WE}$ .
3. During a  $\overline{WE}$  controlled write cycle with  $\overline{OE}$  low,  $t_{WP}$  must be greater than  $t_{WHZ} + t_{OW}$  to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the  $\overline{CE}$  low transition and  $\overline{CE2}$  high transition occurs simultaneously with or after  $\overline{WE}$  low transition, the outputs remain in a high impedance state.
6.  $t_{OW}$  and  $t_{WHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.

DATA RETENTION CHARACTERISTICS ( $T_A = 0$  to  $+70$  /  $-20$  to  $+80$  (E))

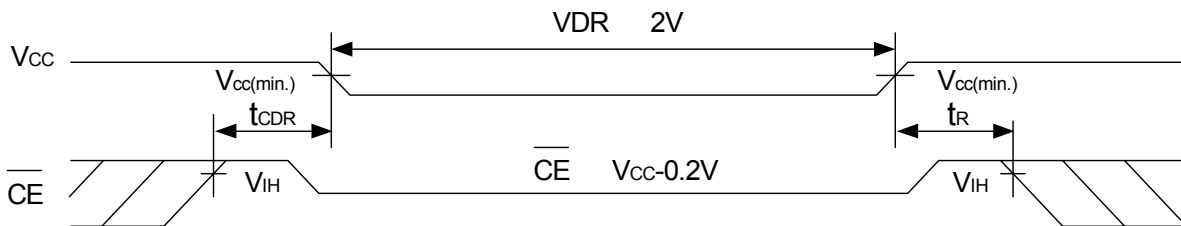
| PARAMETER                           | SYMBOL           | TEST CONDITION   | MIN.              | TYP. | MAX. | UNIT    |
|-------------------------------------|------------------|--|-------------------|------|------|---------|
| Vcc for Data Retention              | V <sub>DR</sub>  | $\overline{CE}$ V <sub>CC</sub> -0.2V or<br>CE2 $\leq 0.2V$                        | 2.0               | -    | 3.3  | V       |
| Data Retention Current              | I <sub>DR</sub>  | V <sub>CC</sub> =2V<br>$\overline{CE}$ V <sub>CC</sub> -0.2V or<br>CE2 $\leq 0.2V$ | - L               | 1    | 40   | $\mu A$ |
|                                     |                  |  | - LL              | 0.3  | 20   | $\mu A$ |
| Chip Disable to Data Retention Time | t <sub>CDR</sub> | See Data Retention Waveforms (below)   | 0                 | -    | -    | ns      |
| Recovery Time                       | t <sub>R</sub>   |  | t <sub>RC</sub> * | -    | -    | ns      |

t<sub>RC</sub>\* = Read Cycle Time

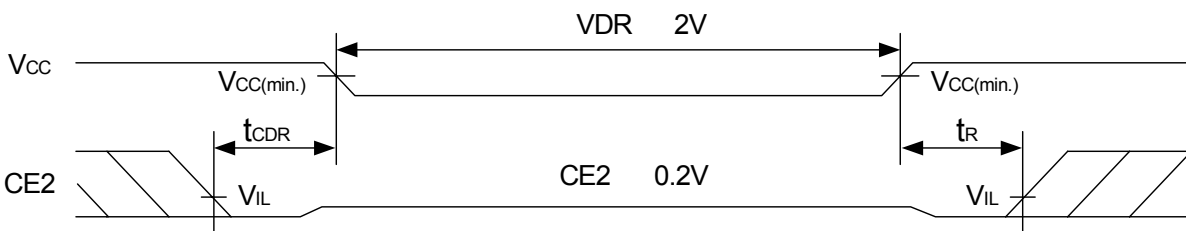
\*Those parameters are for reference only under 50

DATA RETENTION WAVEFORM

Low Vcc Data Retention Waveform (1) ( $\overline{CE}$  controlled)



Low Vcc Data Retention Waveform (2) (CE2 controlled)

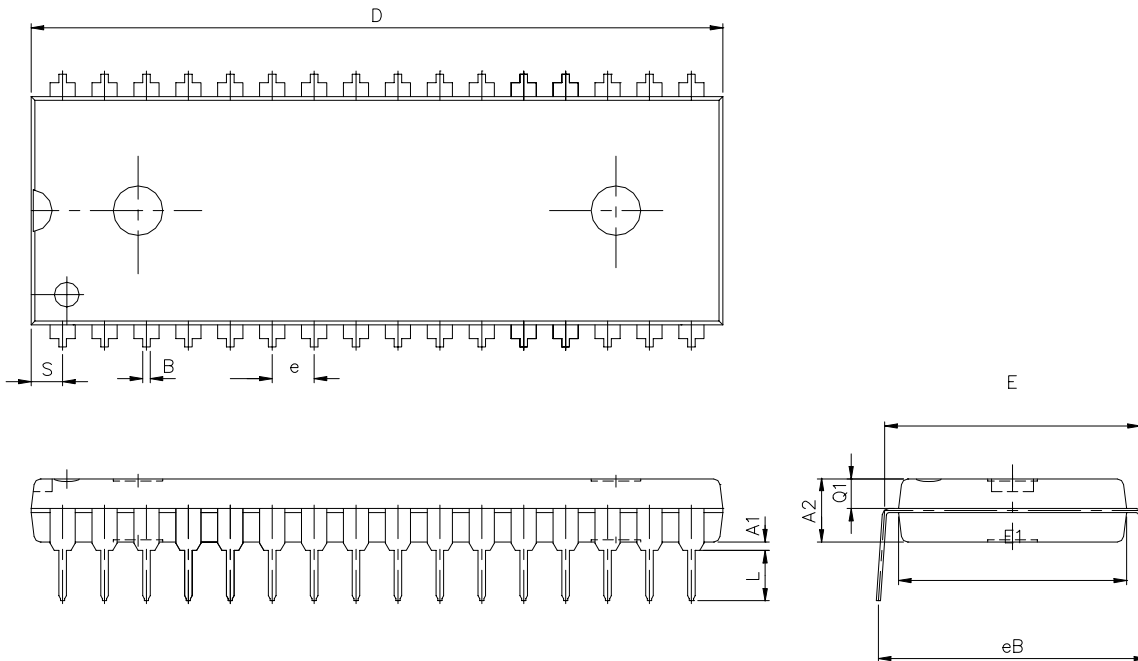






PACKAGE OUTLINE DIMENSION

32-pin 600mil PDIP Package Outline Dimension



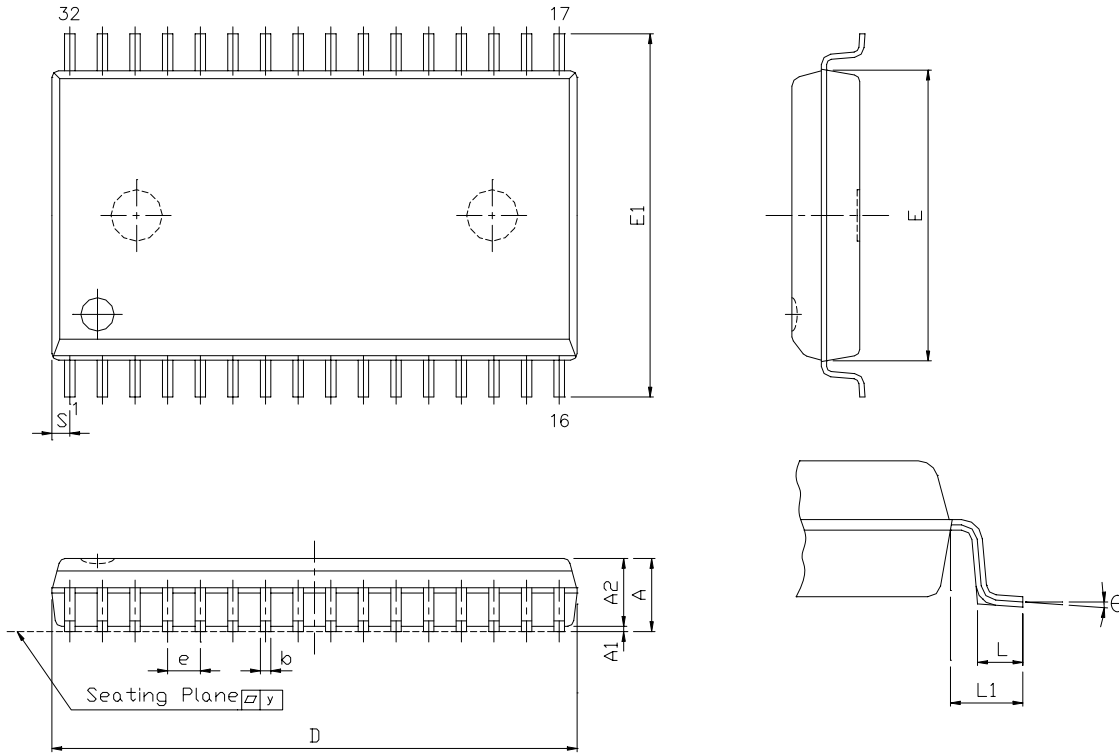
| SYMBOL \ UNIT | INCH(BASE)    | MM(REF)        |
|---------------|---------------|----------------|
| A1            | 0.010(MIN)    | 0.254(MIN)     |
| A2            | 0.150 ± 0.005 | 3.810 ± 0.127  |
| B             | 0.018 ± 0.005 | 0.457 ± 0.127  |
| D             | 1.650 ± 0.005 | 41.910 ± 0.127 |
| E             | 0.600 ± 0.010 | 15.240 ± 0.254 |
| E1            | 0.544 ± 0.004 | 13.818 ± 0.102 |
| e             | 0.100 (TYP)   | 2.540 (TYP)    |
| eB            | 0.640 ± 0.020 | 16.256 ± 0.508 |
| L             | 0.130 ± 0.010 | 3.302 ± 0.254  |
| S             | 0.075 ± 0.010 | 1.905 ± 0.254  |
| Q1            | 0.070 ± 0.005 | 1.778 ± 0.127  |

NOTE:

1. D/E1/S dimension do not include mold flash.



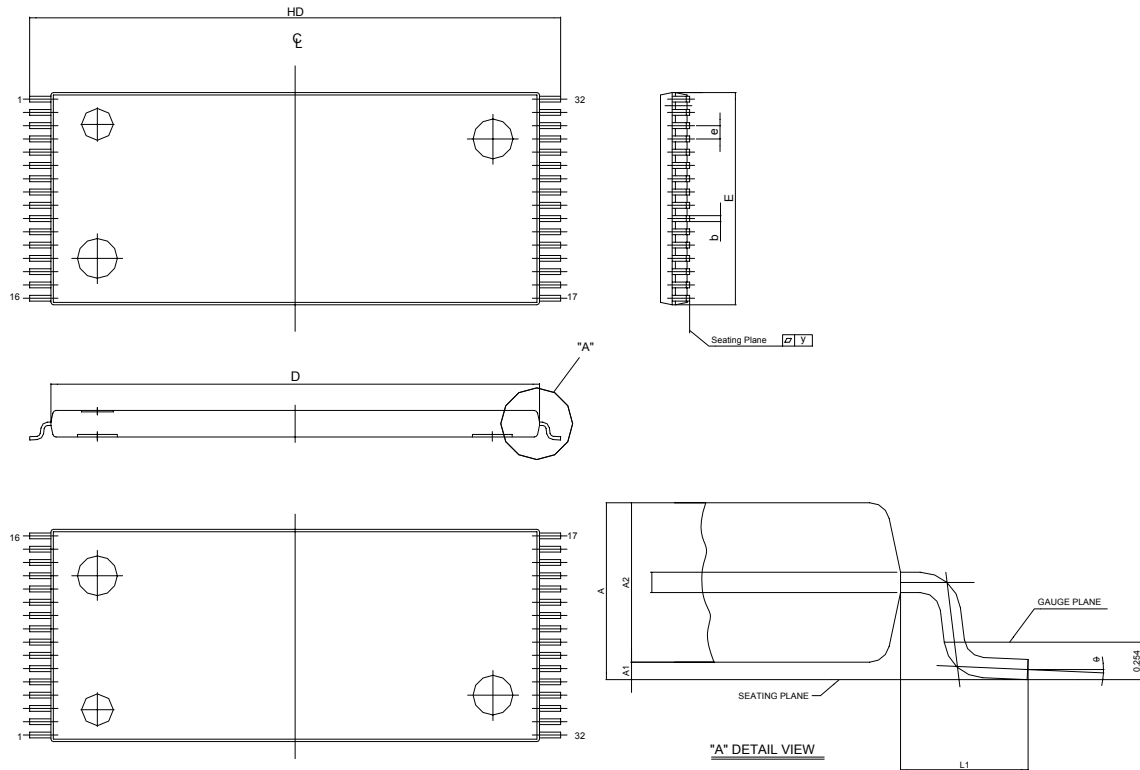
32-pin 450mil SOP Package Outline Dimension



| SYMBOL \ UNIT | INCH(BASE)     | MM(REF)        |
|---------------|----------------|----------------|
| A             | 0.118 (MAX)    | 2.997 (MAX)    |
| A1            | 0.004 (MIN)    | 0.102 (MIN)    |
| A2            | 0.111 (MAX)    | 2.82 (MAX)     |
| b             | 0.016 (TYP)    | 0.406 (TYP)    |
| D             | 0.817 (MAX)    | 20.75 (MAX)    |
| E             | 0.445 ± 0.005  | 11.303 ± 0.127 |
| E1            | 0.555 ± 0.012  | 14.097 ± 0.305 |
| e             | 0.050 (TYP)    | 1.270 (TYP)    |
| L             | 0.0347 ± 0.008 | 0.881 ± 0.203  |
| L1            | 0.055 ± 0.008  | 1.397 ± 0.203  |
| S             | 0.026 (MAX)    | 0.660 (MAX)    |
| y             | 0.004 (MAX)    | 0.101 (MAX)    |
|               | 0° ~ 10°       | 0° ~ 10°       |



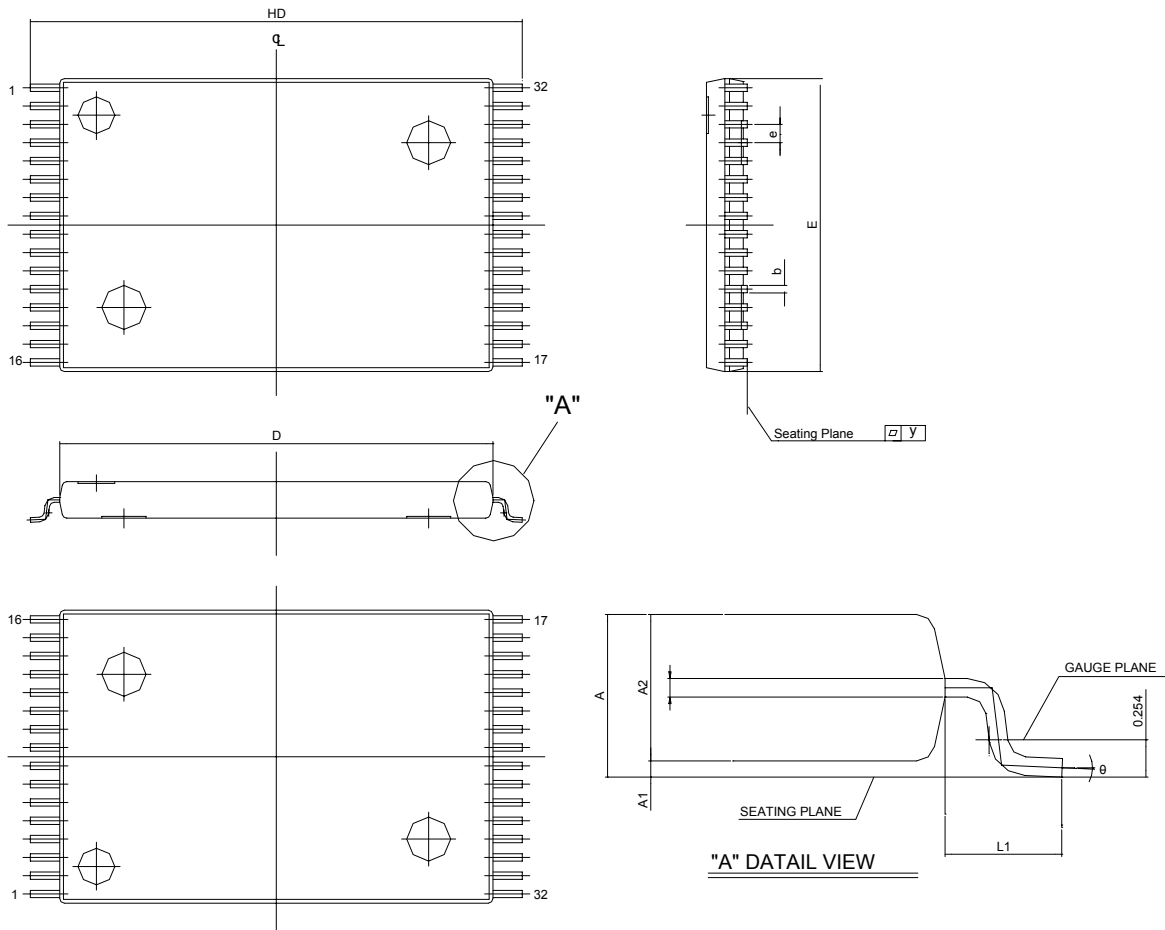
32-pin 8mm x 20mm TSOP- Package Outline Dimension



| SYMBOL | UNIT | INCH(BASE)               | MM(REF)               |
|--------|------|--------------------------|-----------------------|
| A      |      | 0.047 (MAX)              | 1.20 (MAX)            |
| A1     |      | 0.004 ± 0.002            | 0.10 ± 0.05           |
| A2     |      | 0.039 ± 0.002            | 1.00 ± 0.05           |
| b      |      | 0.008 + 0.002<br>- 0.001 | 0.20 + 0.05<br>- 0.03 |
| D      |      | 0.724 ± 0.004            | 18.40 ± 0.10          |
| E      |      | 0.315 ± 0.004            | 8.00 ± 0.10           |
| e      |      | 0.020 (TYP)              | 0.50 (TYP)            |
| HD     |      | 0.787 ± 0.008            | 20.00 ± 0.20          |
| L1     |      | 0.0315 ± 0.004           | 0.80 ± 0.10           |
| y      |      | 0.003 (MAX)              | 0.076 (MAX)           |
|        |      | 0° 5°                    | 0° 5°                 |



32-pin 8mm x 13.4mm STSOP Package Outline Dimension



| SYMBOL | UNIT | INCH(BASE)     | MM(REF)        |
|--------|------|----------------|----------------|
| A      |      | 0.047 (MAX)    | 1.20 (MAX)     |
| A1     |      | 0.004 ± 0.002  | 0.10 ± 0.05    |
| A2     |      | 0.039 ± 0.002  | 1.00 ± 0.05    |
| b      |      | 0.008 ± 0.001  | 0.200 ± 0.025  |
| D      |      | 0.465 ± 0.004  | 11.800 ± 0.100 |
| E      |      | 0.315 ± 0.004  | 8.000 ± 0.100  |
| e      |      | 0.020 (TYP)    | 0.50 (TYP)     |
| HD     |      | 0.528 ± 0.008  | 13.40 ± 0.20.  |
| L1     |      | 0.0315 ± 0.004 | 0.80 ± 0.10    |
| y      |      | 0.003 (MAX)    | 0.076 (MAX)    |
|        |      | 0° 5°          | 0° 5°          |

**ORDERING INFORMATION**

Commercial temperature :

| PART NO.         | ACCESS TIME<br>(ns) | STANDBY CURRENT<br>( $\mu$ A) (max) Ta = 50 | PACKAGE       |
|------------------|---------------------|---|---------------|
| UT62L1024PC-35L  | 35                  | 20  | 32 PIN PDIP   |
| UT62L1024PC-35LL | 35                  | 10  | 32 PIN PDIP   |
| UT62L1024PC-55L  | 55                  | 20  | 32 PIN PDIP   |
| UT62L1024PC-55LL | 55                  | 10  | 32 PIN PDIP   |
| UT62L1024PC-70L  | 70                  | 20  | 32 PIN PDIP   |
| UT62L1024PC-70LL | 70                  | 10  | 32 PIN PDIP   |
| UT62L1024SC-35L  | 35                  | 20  | 32 PIN SOP    |
| UT62L1024SC-35LL | 35                  | 10  | 32 PIN SOP    |
| UT62L1024SC-55L  | 55                  | 20  | 32 PIN SOP    |
| UT62L1024SC-55LL | 55                  | 10  | 32 PIN SOP    |
| UT62L1024SC-70L  | 70                  | 20  | 32 PIN SOP    |
| UT62L1024SC-70LL | 70                  | 10  | 32 PIN SOP    |
| UT62L1024LC-35L  | 35                  | 20  | 32 PIN TSOP-I |
| UT62L1024LC-35LL | 35                  | 10  | 32 PIN TSOP-I |
| UT62L1024LC-55L  | 55                  | 20  | 32 PIN TSOP-I |
| UT62L1024LC-55LL | 55                  | 10  | 32 PIN TSOP-I |
| UT62L1024LC-70L  | 70                  | 20  | 32 PIN TSOP-I |
| UT62L1024LC-70LL | 70                  | 10  | 32 PIN TSOP-I |
| UT62L1024LS-35L  | 35                  | 20  | 32 PIN STSOP  |
| UT62L1024LS-35LL | 35                  | 10  | 32 PIN STSOP  |
| UT62L1024LS-55L  | 55                  | 20  | 32 PIN STSOP  |
| UT62L1024LS-55LL | 55                  | 10  | 32 PIN STSOP  |
| UT62L1024LS-70L  | 70                  | 20  | 32 PIN STSOP  |
| UT62L1024LS-70LL | 70                  | 10  | 32 PIN STSOP  |

**ORDERING INFORMATION**

Extended temp :

| PART NO.          | ACCESS TIME<br>(ns) | STANDBY CURRENT<br>( $\mu$ A) (max) Ta = 50 | PACKAGE       |
|-------------------|---------------------|---|---------------|
| UT62L1024PC-35LE  | 35                  | 20  | 32 PIN PDIP   |
| UT62L1024PC-35LLE | 35                  | 10  | 32 PIN PDIP   |
| UT62L1024PC-55LE  | 55                  | 20  | 32 PIN PDIP   |
| UT62L1024PC-55LLE | 55                  | 10  | 32 PIN PDIP   |
| UT62L1024PC-70LE  | 70                  | 20  | 32 PIN PDIP   |
| UT62L1024PC-70LLE | 70                  | 10  | 32 PIN PDIP   |
| UT62L1024SC-35LE  | 35                  | 20  | 32 PIN SOP    |
| UT62L1024SC-35LLE | 35                  | 10  | 32 PIN SOP    |
| UT62L1024SC-55LE  | 55                  | 20  | 32 PIN SOP    |
| UT62L1024SC-55LLE | 55                  | 10  | 32 PIN SOP    |
| UT62L1024SC-70LE  | 70                  | 20  | 32 PIN SOP    |
| UT62L1024SC-70LLE | 70                  | 10  | 32 PIN SOP    |
| UT62L1024LC-35LE  | 35                  | 20  | 32 PIN TSOP-I |
| UT62L1024LC-35LLE | 35                  | 10  | 32 PIN TSOP-I |
| UT62L1024LC-55LE  | 55                  | 20  | 32 PIN TSOP-I |
| UT62L1024LC-55LLE | 55                  | 10  | 32 PIN TSOP-I |
| UT62L1024LC-70LE  | 70                  | 20  | 32 PIN TSOP-I |
| UT62L1024LC-70LLE | 70                  | 10  | 32 PIN TSOP-I |
| UT62L1024LS-35LE  | 35                  | 20  | 32 PIN STSOP  |
| UT62L1024LS-35LLE | 35                  | 10  | 32 PIN STSOP  |
| UT62L1024LS-55LE  | 55                  | 20  | 32 PIN STSOP  |
| UT62L1024LS-55LLE | 55                  | 10  | 32 PIN STSOP  |
| UT62L1024LS-70LE  | 70                  | 20  | 32 PIN STSOP  |
| UT62L1024LS-70LLE | 70                  | 10  | 32 PIN STSOP  |



**ORDERING INFORMATION (for lead free product)**

Commercial temperature :

| PART NO.          | ACCESS TIME (ns) | STANDBY CURRENT (μA) (max) Ta = 50 | PACKAGE       |
|-------------------|------------------|------------------------------------|---------------|
| UT62L1024PCL-35L  | 35               | 20                                 | 32 PIN PDIP   |
| UT62L1024PCL-35LL | 35               | 10                                 | 32 PIN PDIP   |
| UT62L1024PCL-55L  | 55               | 20                                 | 32 PIN PDIP   |
| UT62L1024PCL-55LL | 55               | 10                                 | 32 PIN PDIP   |
| UT62L1024PCL-70L  | 70               | 20                                 | 32 PIN PDIP   |
| UT62L1024PCL-70LL | 70               | 10                                 | 32 PIN PDIP   |
| UT62L1024SCL-35L  | 35               | 20                                 | 32 PIN SOP    |
| UT62L1024SCL-35LL | 35               | 10                                 | 32 PIN SOP    |
| UT62L1024SCL-55L  | 55               | 20                                 | 32 PIN SOP    |
| UT62L1024SCL-55LL | 55               | 10                                 | 32 PIN SOP    |
| UT62L1024SCL-70L  | 70               | 20                                 | 32 PIN SOP    |
| UT62L1024SCL-70LL | 70               | 10                                 | 32 PIN SOP    |
| UT62L1024LCL-35L  | 35               | 20                                 | 32 PIN TSOP-I |
| UT62L1024LCL-35LL | 35               | 10                                 | 32 PIN TSOP-I |
| UT62L1024LCL-55L  | 55               | 20                                 | 32 PIN TSOP-I |
| UT62L1024LCL-55LL | 55               | 10                                 | 32 PIN TSOP-I |
| UT62L1024LCL-70L  | 70               | 20                                 | 32 PIN TSOP-I |
| UT62L1024LCL-70LL | 70               | 10                                 | 32 PIN TSOP-I |
| UT62L1024LSL-35L  | 35               | 20                                 | 32 PIN STSOP  |
| UT62L1024LSL-35LL | 35               | 10                                 | 32 PIN STSOP  |
| UT62L1024LSL-55L  | 55               | 20                                 | 32 PIN STSOP  |
| UT62L1024LSL-55LL | 55               | 10                                 | 32 PIN STSOP  |
| UT62L1024LSL-70L  | 70               | 20                                 | 32 PIN STSOP  |
| UT62L1024LSL-70LL | 70               | 10                                 | 32 PIN STSOP  |



**ORDERING INFORMATION (for lead free product)**

Extended temperature :

| PART NO.           | ACCESS TIME (ns) | STANDBY CURRENT (μA) (max) Ta = 50 | PACKAGE       |
|--------------------|------------------|------------------------------------|---------------|
| UT62L1024PCL-35LE  | 35               | 20                                 | 32 PIN PDIP   |
| UT62L1024PCL-35LLE | 35               | 10                                 | 32 PIN PDIP   |
| UT62L1024PCL-55LE  | 55               | 20                                 | 32 PIN PDIP   |
| UT62L1024PCL-55LLE | 55               | 10                                 | 32 PIN PDIP   |
| UT62L1024PCL-70LE  | 70               | 20                                 | 32 PIN PDIP   |
| UT62L1024PCL-70LLE | 70               | 10                                 | 32 PIN PDIP   |
| UT62L1024SCL-35LE  | 35               | 20                                 | 32 PIN SOP    |
| UT62L1024SCL-35LLE | 35               | 10                                 | 32 PIN SOP    |
| UT62L1024SCL-55LE  | 55               | 20                                 | 32 PIN SOP    |
| UT62L1024SCL-55LLE | 55               | 10                                 | 32 PIN SOP    |
| UT62L1024SCL-70LE  | 70               | 20                                 | 32 PIN SOP    |
| UT62L1024SCL-70LLE | 70               | 10                                 | 32 PIN SOP    |
| UT62L1024LCL-35LE  | 35               | 20                                 | 32 PIN TSOP-I |
| UT62L1024LCL-35LLE | 35               | 10                                 | 32 PIN TSOP-I |
| UT62L1024LCL-55LE  | 55               | 20                                 | 32 PIN TSOP-I |
| UT62L1024LCL-55LLE | 55               | 10                                 | 32 PIN TSOP-I |
| UT62L1024LCL-70LE  | 70               | 20                                 | 32 PIN TSOP-I |
| UT62L1024LCL-70LLE | 70               | 10                                 | 32 PIN TSOP-I |
| UT62L1024LSL-35LE  | 35               | 20                                 | 32 PIN STSOP  |
| UT62L1024LSL-35LLE | 35               | 10                                 | 32 PIN STSOP  |
| UT62L1024LSL-55LE  | 55               | 20                                 | 32 PIN STSOP  |
| UT62L1024LSL-55LLE | 55               | 10                                 | 32 PIN STSOP  |
| UT62L1024LSL-70LE  | 70               | 20                                 | 32 PIN STSOP  |
| UT62L1024LSL-70LLE | 70               | 10                                 | 32 PIN STSOP  |





UTRON

Rev. 1.9

UT62L1024

128KX8 BIT LOW POWER CMOS SRAM

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