DESCRIPTION

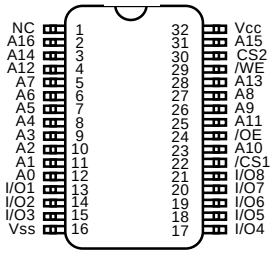
The HY628100A is a high speed, low power and 1M bit CMOS Static Random Access Memory organized as 131,072 words by 8bit. The HY628100A uses high performance CMOS process technology and designed for high speed low power circuit technology. It is particulary well suited for used in high density low power system application. This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0V.

FEATURES

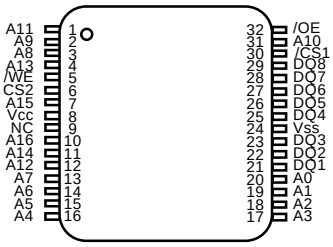
- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Battery backup(L/LL-part)
  - 2.0V(min) data retention
- Standard pin configuration
  - 32pin 525mil SOP
  - 32pin 8x20mm TSOP-I(Standard)

Product No	Voltage (V)	Speed (ns)	Operation Current(mA)	Standby Current(uA)			Temperature (¡É)
					L	LL	
HY628100A	5.0	50/55/70	10	1mA	100	20	0~70

PIN CONNECTION



SOP

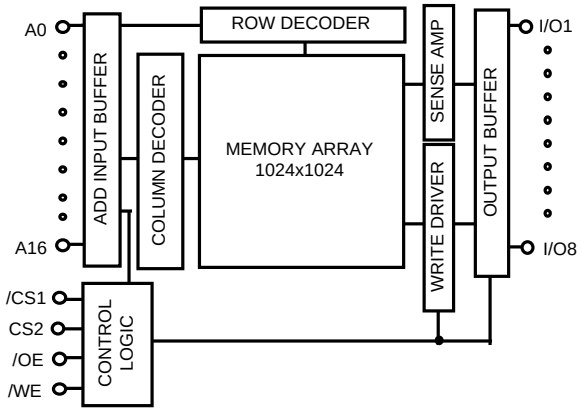


TSOP-I(Standard)

PIN DESCRIPTION

Pin Name	Pin Function
/CS1	Chip Select 1
CS2	Chip Select 2
/WE	Write Enable
/OE	Output Enable
A0 ~ A16	Address Input
I/O1 ~ I/O8	Data Input/Output
Vcc	Power(5.0V)
Vss	Ground

BLOCK DIAGRAM



ORDERING INFORMATION

Part No.	Speed	Power	Temp	Package
HY628100AG	50/55/70			SOP
HY628100ALG	50/55/70	L-part		SOP
HY628100ALLG	50/55/70	LL-part		SOP
HY628100AT1	50/55/70			TSOP-I(Standard)
HY628100ALT1	50/55/70	L-part		TSOP-I(Standard)
HY628100ALLT1	50/55/70	LL-part		TSOP-I(Standard)

ABSOLUTE MAXIMUM RATING (1)

Symbol	Parameter	Rating	Unit
Vcc, VIN, VOUT	Power Supply, Input/Output Voltage	-0.5 to 7.0	V
TA	Operating Temperature	0 to 70	¡É
TSTG	Storage Temperature	-65 to 125	¡É
PD	Power Dissipation	1.0	W
IOUT	Data Output Current	50	mA
TSOLDER	Lead Soldering Temperature & Time	260•10	¡É•sec

Note
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliablity.

RECOMMENDED DC OPERATING CONDITION

TA=0¡É to 70¡É/-40¡É to 85¡É

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
Vss	Ground	0	0	0	V
VIH	Input High Voltage	2.2	-	Vcc+0.5	V
VIL	Input Low Voltage	-0.5(1)	-	0.8	V

Note :
1. VIL = -3.0V for pulse width less than 30ns

TRUTH TABLE

/CS1	CS2	/WE	/OE	MODE	I/O OPERATION
H	X	X	X	Standby	High-Z
X	L	X	X		High-Z
L	H	H	H	Output Disabled	High-Z
L	H	H	L	Read	Data Out
L	H	L	X	Write	Data In

Note :
1. H=VIH, L=VIL, X=don't care

DC ELECTRICAL CHARACTERISTICS

Vcc = 5.0V¡¾10%, TA = 0¡É to 70¡É, unless otherwise specified

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
ILI	Input Leakage Current	Vss ¡ÂVIN ¡Â Vcc		-1	-	1	uA
ILO	Output Leakage Current	Vss ¡ÂVOUT ¡ÂVcc, /CS1 = VIH or CS2 = VIL or /OE = VIH or /WE = VIL		-1	-	1	uA
Icc	Operating Power Supply Current	/CS1 = VIL, CS2 = VIH, VIN = VIH or VIL, II/O = 0mA		-	5	10	mA
ICC1	Average Operating Current	/CS1 = VIL CS2 = VIH, Min Duty Cycle = 100%, II/O = 0mA		-	30	50	mA
ISB	TTL Standby Current (TTL Input)	/CS1 = VIH or CS2 = VIL		-	1	2	mA
ISB1	Standby Current (CMOS Input)	/CS1 ¡Ã Vcc - 0.2V		-	-	1	mA
		CS2 ¡Â 0.2V or	L	-	2	100	uA
		CS2 ¡Ã Vcc - 0.2V	LL	-	1	20	uA
VOL	Output Low Voltage	IOL = 2.1mA		-	-	0.4	V
VOH	Output High Voltage	IOH = -1mA		2.4	-	-	V

Note : Typical values are at Vcc = 5.0V, TA = 25¡É

AC CHARACTERISTICS

Vcc = 5.0V¡¾10%, TA = 0¡É to 70¡É(Normal), unless otherwise specified

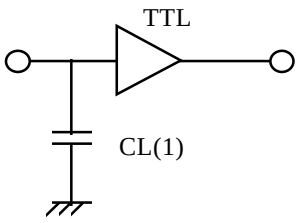
#	Symbol	Parameter	-50		-55		-70		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
	READ CYCLE								
1	tRC	Read Cycle Time	50	-	55	-	70	-	ns
2	tAA	Address Access Time	-	50	-	55	-	70	ns
3	tACS	Chip Select Access Time	-	50	-	55	-	70	ns
4	tOE	Output Enable to Output Valid	-	25	-	25	-	35	ns
5	tCLZ	Chip Select to Output in Low Z	10	-	10	-	10	-	ns
6	tOLZ	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
7	tCHZ	Chip Deselection to Output in High Z	0	20	0	20	0	25	ns
8	tOHZ	Out Disable to Output in High Z	0	20	0	20	0	25	ns
9	tOH	Output Hold from Address Change	10	-	10	-	10	-	ns
	WRITE CYCLE								
10	tWC	Write Cycle Time	50	-	50	-	70	-	ns
11	tCW	Chip Selection to End of Write	45	-	45	-	60	-	ns
12	tAW	Address Valid to End of Write	45	-	45	-	60	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width	40	-	40	-	50	-	ns
15	tWR	Write Recovery Time	0	-	0	-	0	-	ns
16	tWHZ	Write to Output in High Z	0	20	0	20	0	25	ns
17	tDW	Data to Write Time Overlap	25	-	25	-	30	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
19	tOW	Output Active from End of Write	5	-	5	-	5	-	ns

AC TEST CONDITIONS

T_A = 0¡É to 70¡É(Normal), unless otherwise specified

PARAMETER	Value
Input Pulse Level	0.8V to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V
Output Load	CL = 100pF + 1TTL Load

AC TEST LOADS



Note : Including jig and scope capacitance

CAPACITANCE

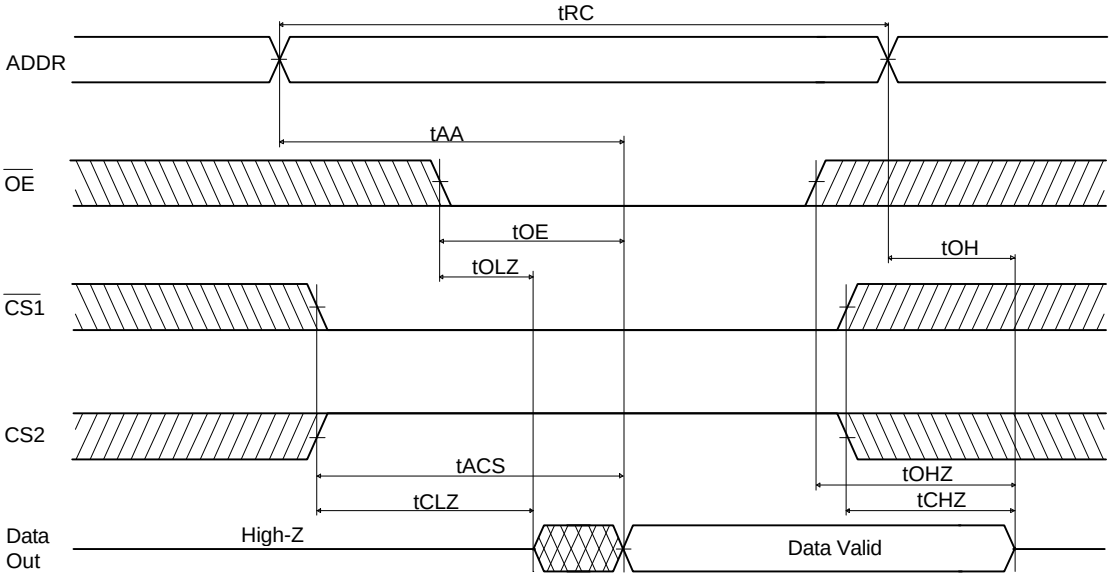
Temp = 25¡É, f= 1.0MHz

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	8	pF

Note : These parameters are sampled and not 100% tested

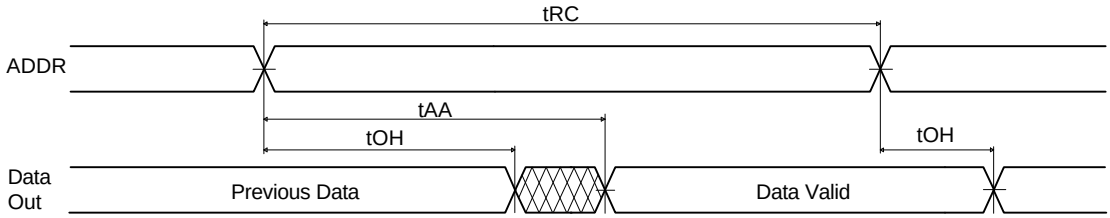
TIMING DIAGRAM

READ CYCLE 1



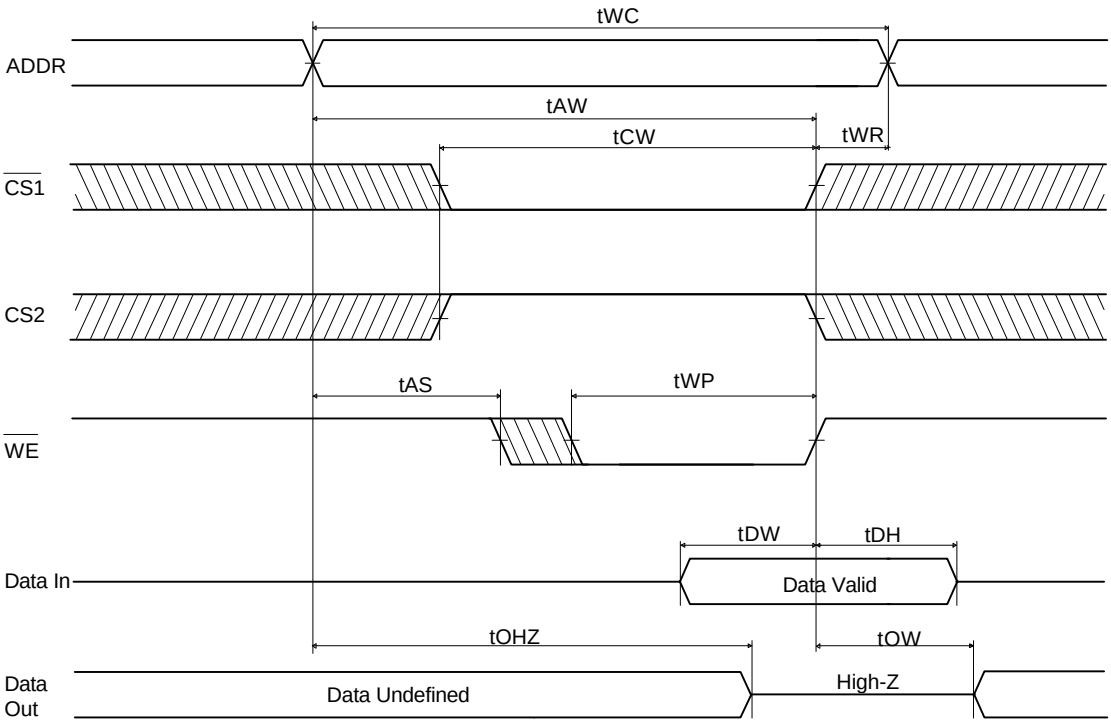
Note(READ CYCLE):
1. tCHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels
2. At any given temperature and voltage condition, tCHZ max. is less than tCLZ min. both for a given device and from device to device.
3. /WE is high for the read cycle.

READ CYCLE 2

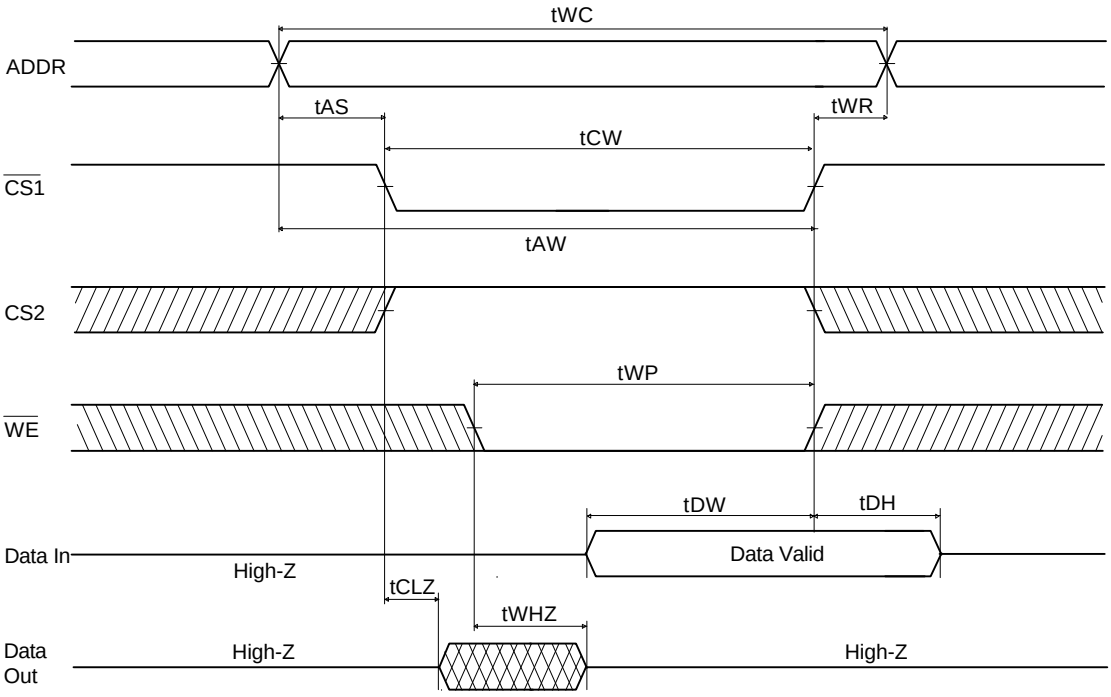


Note(READ CYCLE):
1. /WE is high for the read cycle.
2. Device is continuously selected /CS1 = V_{IL}, CS2 = V_{IH}.
3. /OE =V_{IL}.

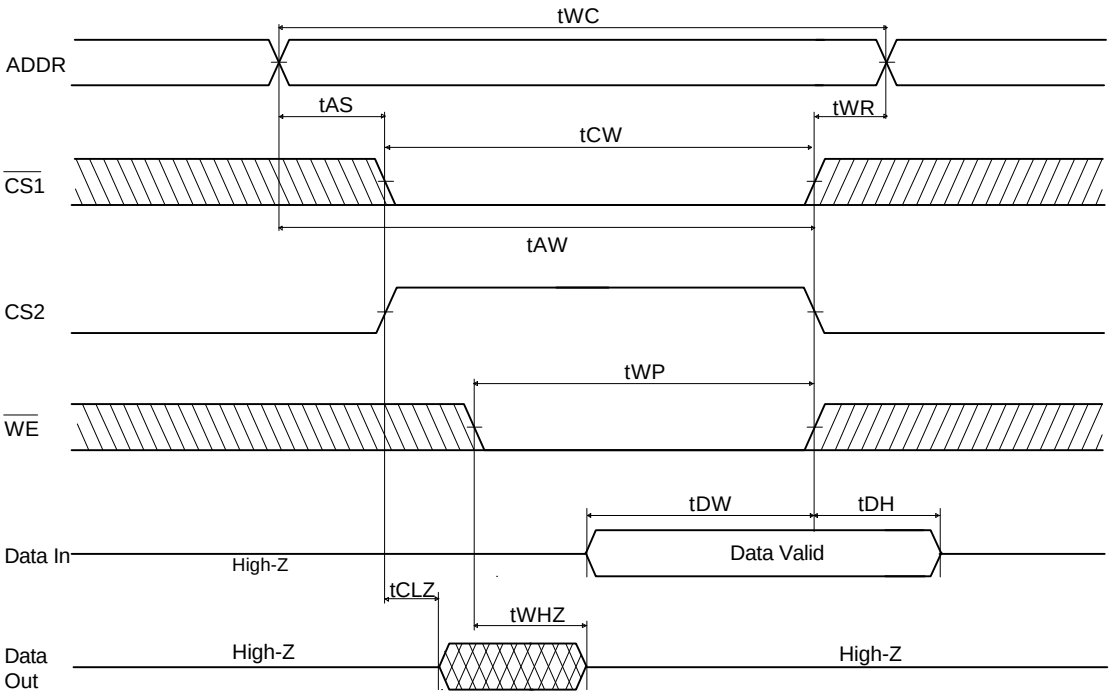
WRITE CYCLE 1(/WE Controlled)



WRITE CYCLE 2 (/CS1 Controlled)



WRITE CYCLE 3 (CS2 Controlled)



Notes(WRITE CYCLE):

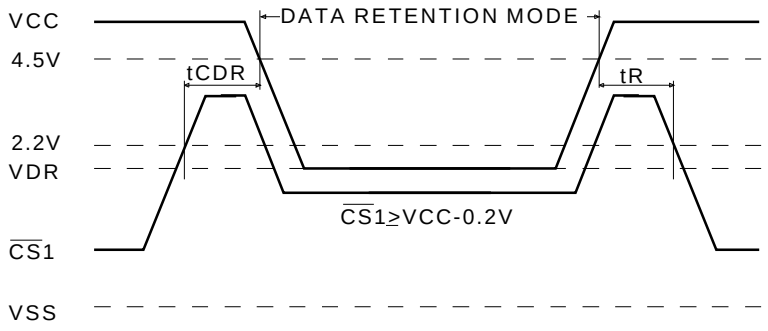
1. A write occurs during the overlap of a low /CS1, CS2 and low /WE. A write begines at the latest transition among /CS1 going low, CS2 going high and /WE going low: A write ends at the earliest transition among /CS1 going high, CS2 low and /WE going high. tWP is measured from the beginning of write to the end of write. .
2. tCW is measured from the later of /CS1 going low or CS2 going high to the end of write .
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR is applied in case a write ends as /CS1, or /WE going high, and tWR is applied in case a write ends at CS2 going low.
5. If /OE, CS2 and /WE are in the read mode during this period, the I/O pins are in the output low-Z state, input of opposite phase of the output must not be applied because bus contention can occur.
6. If /CS1 goes low simultaneously with /WE going low, the outputs remain in high impedance state.
7. Dout is the read data of the new address.
8. When /CS1 is low and CS2 is high, I/O pins are in the output state. The input signals in the opposite phase leading to the outputs should not be applied.

DATA RETENTION ELECTRIC CHARACTERISTIC

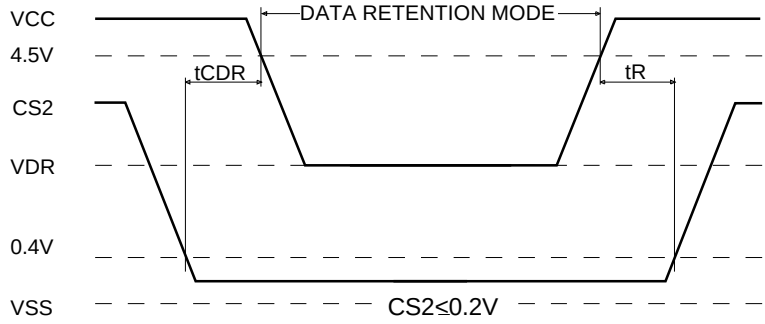
SYM	Parameter	Test Condition		Min	Typ	Max	Unit
VDR	Vcc for Data Retention	/CS1 ¡Ã Vcc - 0.2V CS2 ¡Â 0.2V or ¡Ã Vcc - 0.2V, Vss¡Â VIN¡Â Vcc		2.0	-	-	V
ICCDR	Data Retention Current	Vcc = 3.0V, /CS1¡ÃVcc - 0.2V	L	-	2	50	uA
		CS2¡Â 0.2V or ¡Ã Vcc - 0.2V, Vss¡Â VIN ¡Â Vcc	LL	-	1	10	uA
tCDR	Chip Deselect to Data Retention Time			0	-	-	ns
tR	Operating Recovery Time			tRC(2)	-	-	ns

Notes:
1. Typical values are under the condition of TA = 25¡É.
2. tRC is read cycle time.

DATA RETENTION TIMING DIAGRAM 1



DATA RETENTION TIMING DIAGRAM 2

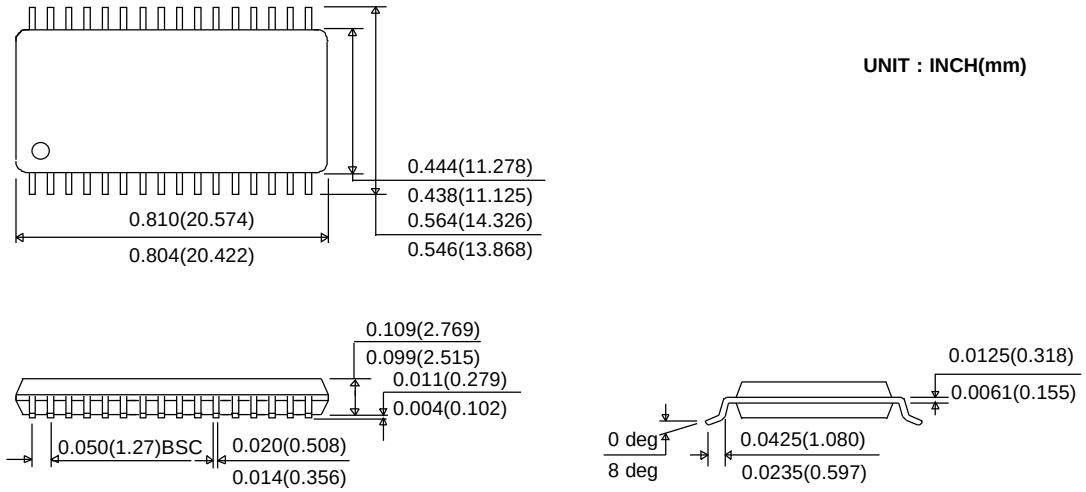


RELIABILITY SPEC.

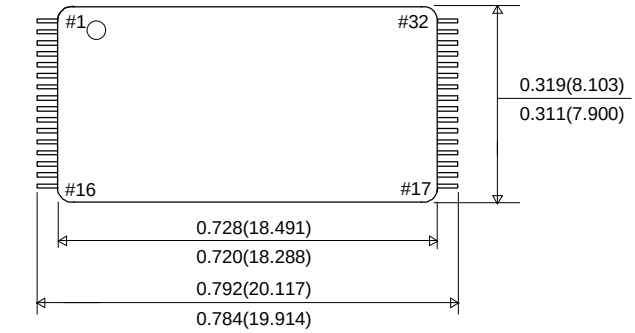
TEST MODE		TEST SPEC.
ESD	HBM	¡Ã 2000V
	MM	¡Ã 250V
LATCH - UP		¡Â -100mA
		¡Ã100mA

PACKAGE INFORMATION

32pin 525mil Small Outline Package(G)



32pin 8x20mm Thin Small Outline Package Standard(T1)



UNIT : INCH(mm)