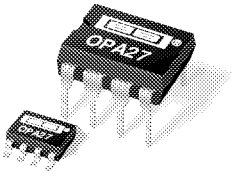
BURR - BROWN®



OPA27
OPA37

Ultra-Low Noise Precision OPERATIONAL AMPLIFIERS

FEATURES

- LOW NOISE: 4.5nV/√Hz max at 1kHz
- LOW OFFSET: 100μV max
- LOW DRIFT: 0.4μV/°C
- HIGH OPEN-LOOP GAIN: 117dB min
- HIGH COMMON-MODE REJECTION: 100dB min
- HIGH POWER SUPPLY REJECTION: 94dB min
- FITS OP-07, OP-05, AD510, AD517 SOCKETS

APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- PROFESSIONAL AUDIO EQUIPMENT
- TRANSDUCER AMPLIFIER
- RADIATION HARD EQUIPMENT

DESCRIPTION

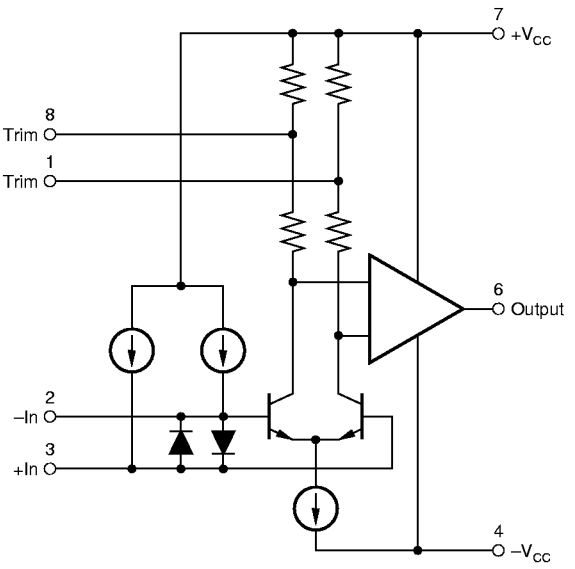
The OPA27/37 is an ultra-low noise, high precision monolithic operational amplifier.

Laser-trimmed thin-film resistors provide excellent long-term voltage offset stability and allow superior voltage offset compared to common zener-zap techniques.

A unique bias current cancellation circuit allows bias and offset current specifications to be met over the full –55°C to +125°C temperature range.

The OPA27 is internally compensated for unity-gain stability. The decompensated OPA37 requires a closed-loop gain ≥ 5.

The Burr-Brown OPA27/37 is an improved replacement for the industry-standard OP-27/OP-37.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-466M
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SPECIFICATIONS

At V_{CC} = ±15V and T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	OPA27/37G MIN	OPA27/37G TYP	OPA27/37G MAX	UNITS
INPUT NOISE[6]					
Voltage, f_O = 10Hz			3.8	8.0	nV/√Hz
f_O = 30Hz			3.3	5.6	nV/√Hz
f_O = 1kHz			3.2	4.5	nV/√Hz
f_B = 0.1Hz to 10Hz			0.09	0.25	µVp-p
Current,[1] f_O = 10Hz			1.7		pA/√Hz
f_O = 30Hz			1.0		pA/√Hz
f_O = 1kHz			0.4	0.6	pA/√Hz
OFFSET VOLTAGE[2]					
Input Offset Voltage			±25	±100	µV
Average Drift[3]	$T_{A\ MIN}$ to $T_{A\ MAX}$		±0.4	±1.8[6]	µV/°C
Long Term Stability[4]			0.4	2.0	µV/mo
Supply Rejection	±V_{CC} = 4 to 18V	94	120		dB
	±V_{CC} = 4 to 18V		±1	±20	µV/V
BIAS CURRENT					
Input Bias Current			±15	±80	nA
OFFSET CURRENT					
Input Offset Current			10	75	nA
IMPEDANCE					
Common-Mode			2 || 2.5		GΩ || pF
VOLTAGE RANGE					
Common-Mode Input Range		±11	±12.3		V
Common-Mode Rejection	V_{IN} = ±11VDC	100	122		dB
OPEN-LOOP VOLTAGE GAIN, DC	R_L ≥ 2kΩ	117	124		dB
	R_L ≥ 1kΩ		124		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product[5]	OPA27	5[6]	8		MHz
	OPA37	45[6]	63		MHz
Slew Rate[5]	V_O = ±10V, R_L = 2kΩ				
	OPA27, G = +1	1.7[6]	1.9		V/µs
	OPA37, G = +5	11[6]	11.9		V/µs
Settling Time, 0.01%	OPA27, G = +1		25		µs
	OPA37, G = +5		25		µs
RATED OUTPUT					
Voltage Output	R_L ≥ 2kΩ	±12	±13.8		V
	R_L ≥ 600Ω	±10	±12.8		V
Output Resistance	DC, Open Loop		70		Ω
Short Circuit Current	R_L = 0Ω		25	60[6]	mA
POWER SUPPLY					
Rated Voltage			±15		VDC
Voltage Range,					
Derated Performance		±4		±22	VDC
Current, Quiescent	I_O = 0mADC		3.3	5.7	mA
TEMPERATURE RANGE					
Specification		–40		+85	°C
Operating		–40		+85	°C

NOTES: (1) Measured with industry-standard noise test circuit (Figures 1 and 2). Due to errors introduced by this method, these current noise specifications should be used for comparison purposes only. (2) Offset voltage specification are measured with automatic test equipment after approximately 0.5 seconds from power turn-on. (3) Unnulled or nulled with 8kΩ to 20kΩ potentiometer. (4) Long-term voltage offset vs time trend line does not include warm-up drift. (5) Typical specification only on plastic package units. Slew rate varies on all units due to differing test methods. Minimum specification applies to open-loop test. (6) This parameter guaranteed by design.

SPECIFICATIONS

At V_{CC} = ±15V and T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	OPA27/37G MIN	OPA27/37G TYP	OPA27/37G MAX	UNITS
INPUT VOLTAGE(1)					
Input Offset Voltage			±48	±220(3)	µV
Average Drift(2)	$T_{A\,MIN}$ to $T_{A\,MAX}$		±0.4	±1.8(3)	µV/°C
Supply Rejection	±V_{CC} = 4.5 to 18V				
	±V_{CC} = 4.5 to 18V	90 (3)	122		dB
BIAS CURRENT					
Input Bias Current			±21	±150(3)	nA
OFFSET CURRENT					
Input Offset Current					
E, F, G			20	135(3)	nA
VOLTAGE RANGE					
Common-Mode Input Range		±10.5(3)	±11.8		V
Common-Mode Rejection	V_{IN} = ±11VDC	96(3)	122		dB
OPEN-LOOP GAIN, DC					
Open-Loop Voltage Gain	R_L ≥ 2kΩ	113(3)	120		dB
RATED OUTPUT					
Voltage Output	R_L = 2kΩ	±11.0(3)	±13.4		V
Short Circuit Current	V_O = 0VDC		25		mA
TEMPERATURE RANGE					
Specification		–40		+85	°C

NOTES: (1) Offset voltage specification are measured with automatic test equipment after approximately 0.5s from power turn-on. (2) Unnulled or nulled with 8kΩ to 20kΩ potentiometer. (3) This parameter guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Internal Power Dissipation (1) 500mW
Input Voltage ..... ±V_{CC}
Output Short-Circuit Duration (2) ..... Indefinite
Differential Input Voltage (3) ..... ±0.7V
Differential Input Current (3) ..... ±25mA
Storage Temperature Range ..... –55°C to +125°C
Operating Temperature Range ..... –40°C to +85°C
Lead Temperature:
P (soldering, 10s) ..... +300°C
U (soldering, 3s) ..... +260°C

PACKAGE TYPE	θ_{JA}	UNITS
8-Pin Plastic DIP (P)	100	°C/W
8-Pin SOIC (U)	160	°C/W

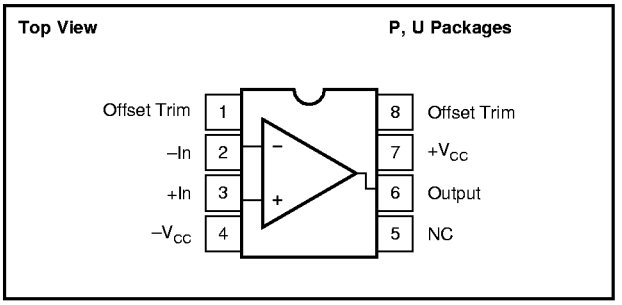
NOTES: (1) Maximum package power dissipation vs ambient temperature. (2) To common with ±V_{CC} = 15V. (3) The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

CONNECTION DIAGRAMS



PACKAGE/ORDERING INFORMATION

PRODUCT[1]	PACKAGE	TEMPERATURE RANGE (°C)	OFFSET VOLTAGE MAX (µV), 25°C	PACKAGE DRAWING NUMBER[3]
OPA27GP	Plastic	–40 to +85	±100	006
OPA27GU[2]	SOIC	–40 to +85	±100	182

NOTE: (1) Packages for OPA37 are same as for OPA27. (2) OPA27GU may be marked OPA27U. Likewise, OPA37GU may be marked OPA37U. (3) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

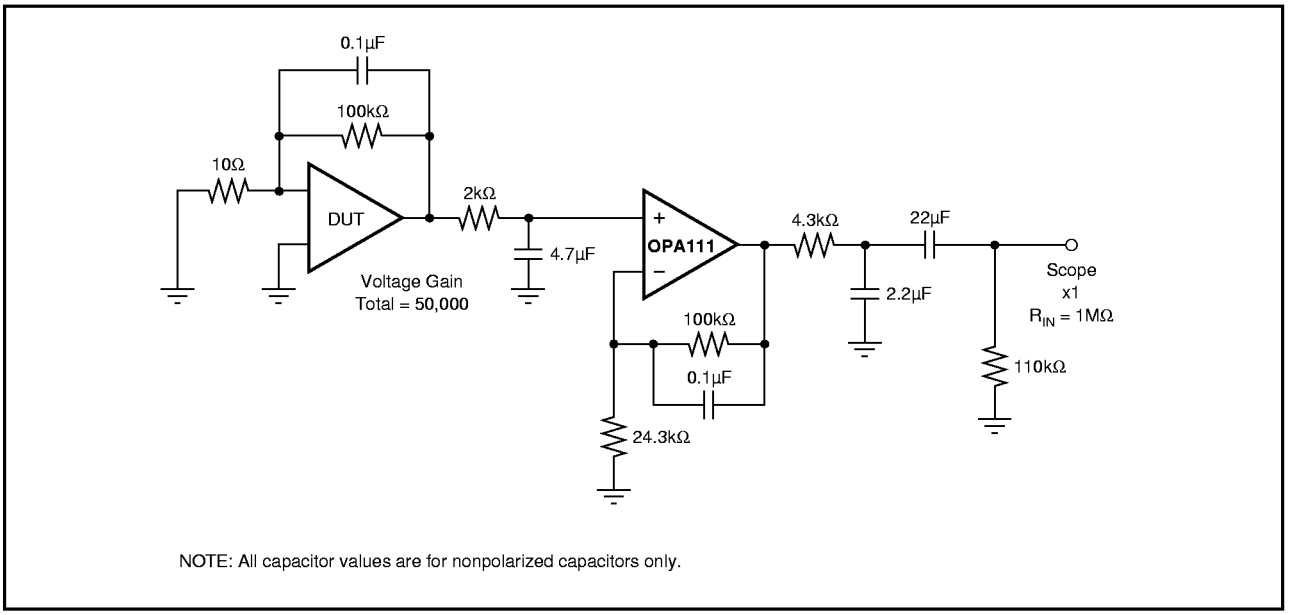


FIGURE 1. 0.1Hz to 10Hz Noise Test Circuit.

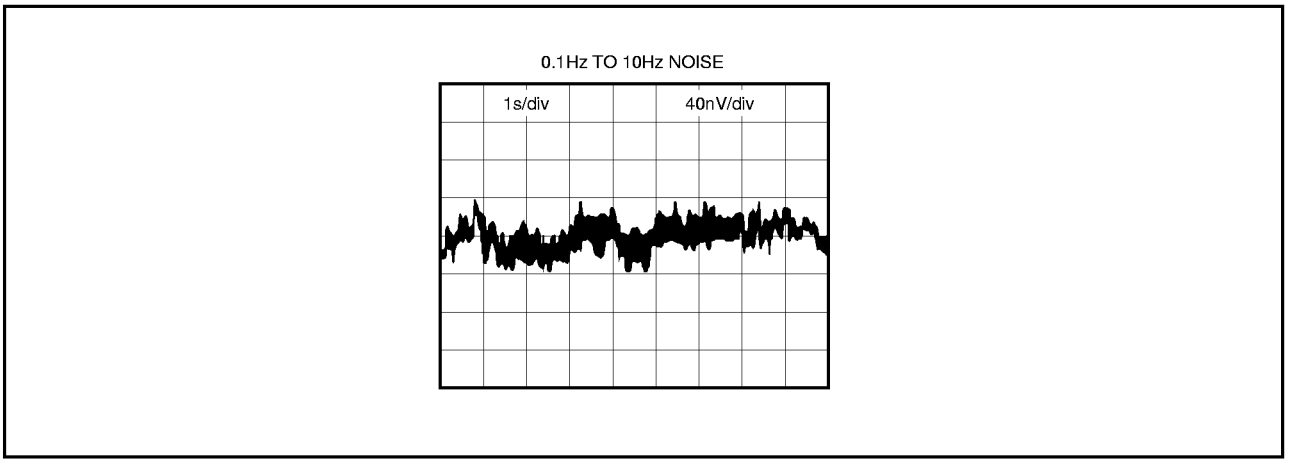
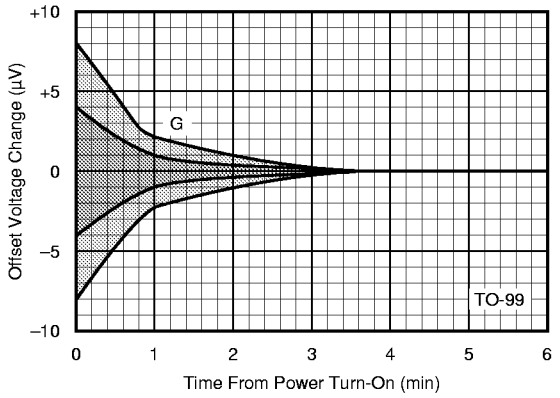


FIGURE 2. Low Frequency Noise.

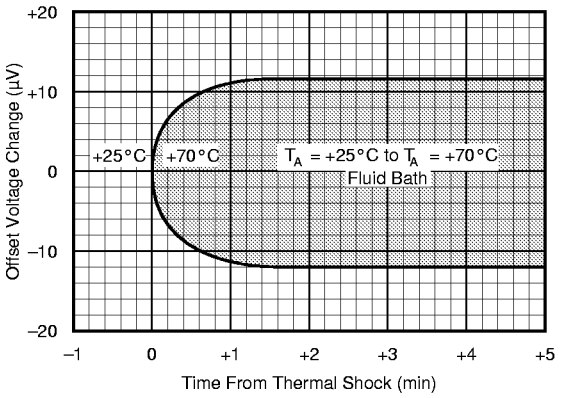
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, $\pm V_{CC}$ = ±15VDC, unless otherwise noted.

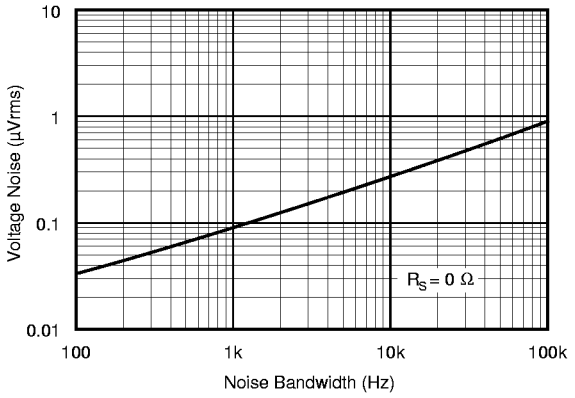
INPUT OFFSET VOLTAGE WARM-UP DRIFT



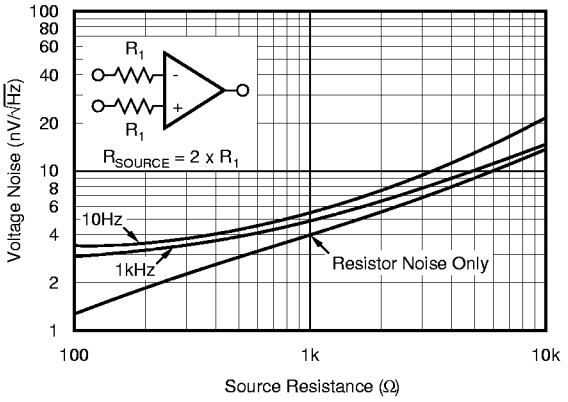
INPUT OFFSET VOLTAGE CHANGE
DUE TO THERMAL SHOCK



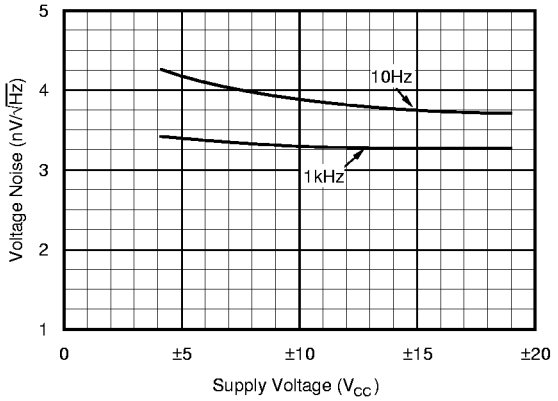
INPUT VOLTAGE NOISE vs NOISE BANDWIDTH
(0.1Hz to Indicated Frequency)



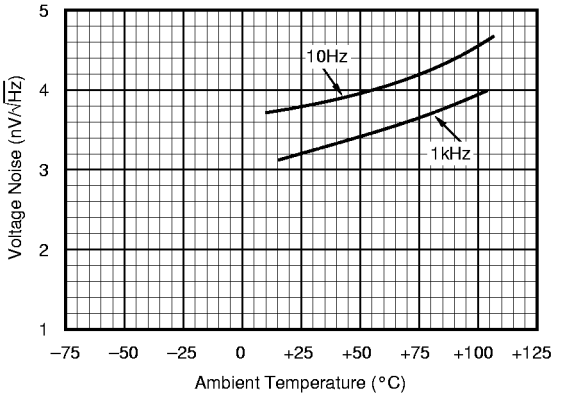
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY
vs SOURCE RESISTANCE



VOLTAGE NOISE SPECTRAL DENSITY
vs SUPPLY VOLTAGE



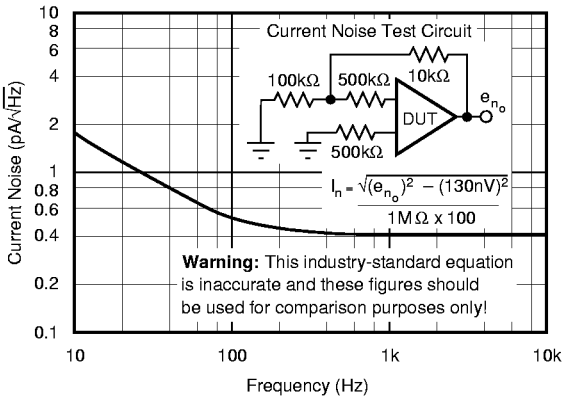
VOLTAGE NOISE SPECTRAL DENSITY
vs TEMPERATURE



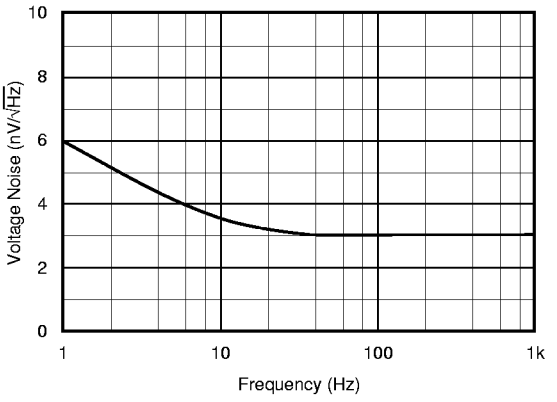
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, $\pm V_{CC}$ = ±15VDC, unless otherwise noted.

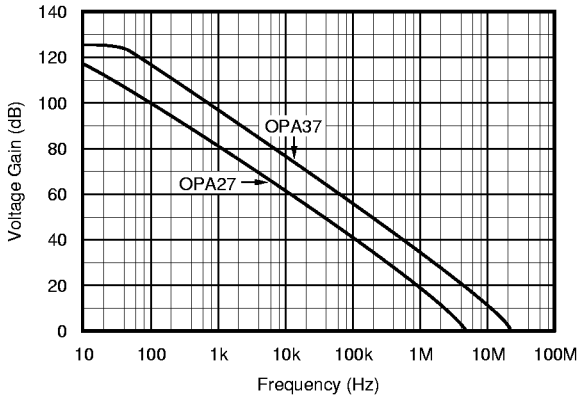
INPUT CURRENT NOISE SPECTRAL DENSITY



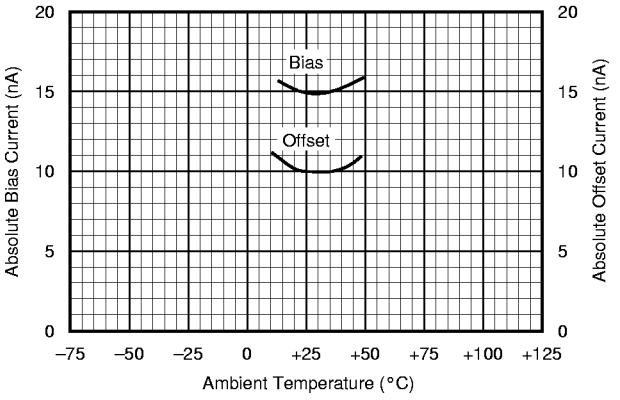
INPUT VOLTAGE NOISE SPECTRAL DENSITY



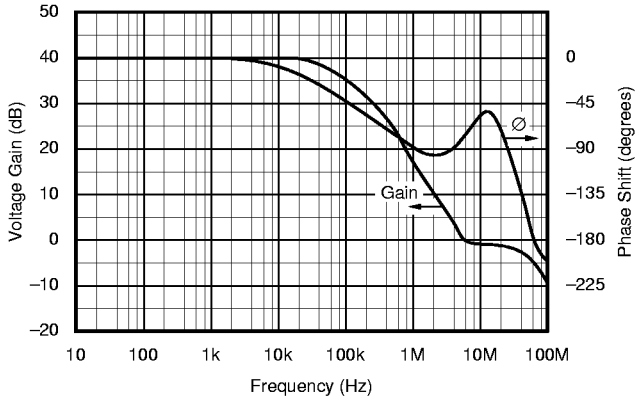
OPEN-LOOP FREQUENCY RESPONSE



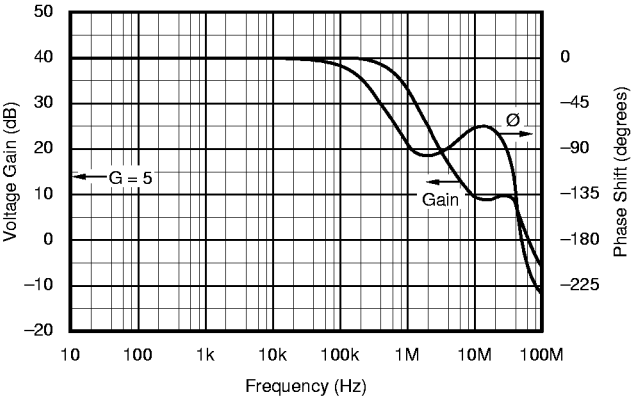
BIAS AND OFFSET CURRENT vs TEMPERATURE



OPA27 CLOSED-LOOP VOLTAGE GAIN AND PHASE SHIFT vs FREQUENCY (G = 100)



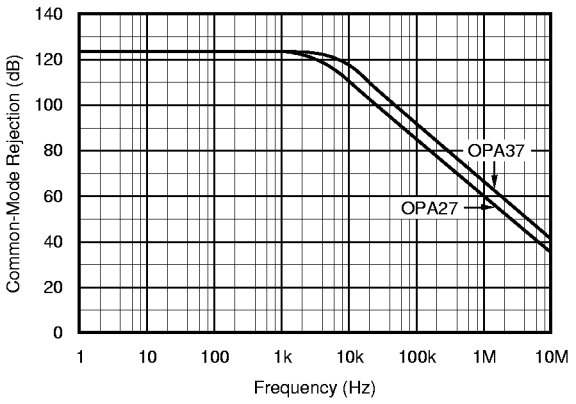
OPA37 CLOSED-LOOP VOLTAGE GAIN AND PHASE SHIFT vs FREQUENCY (G = 100)



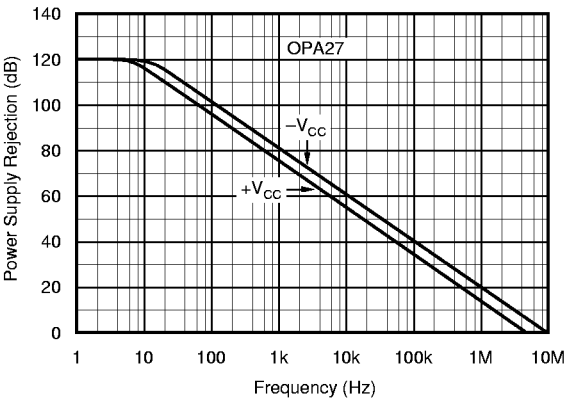
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, ±V_{CC} = ±15VDC, unless otherwise noted.

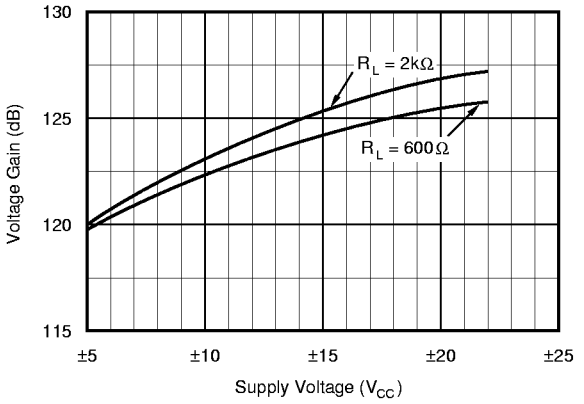
COMMON-MODE REJECTION vs FREQUENCY



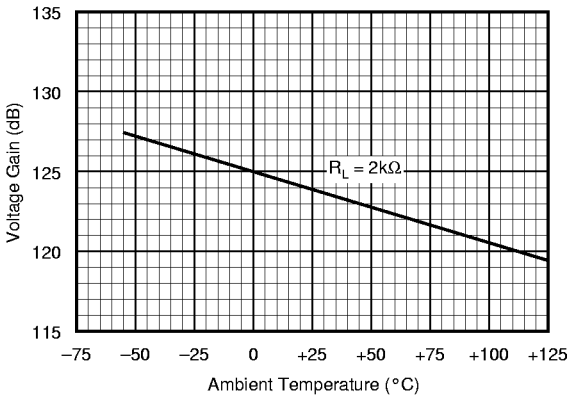
POWER SUPPLY REJECTION vs FREQUENCY



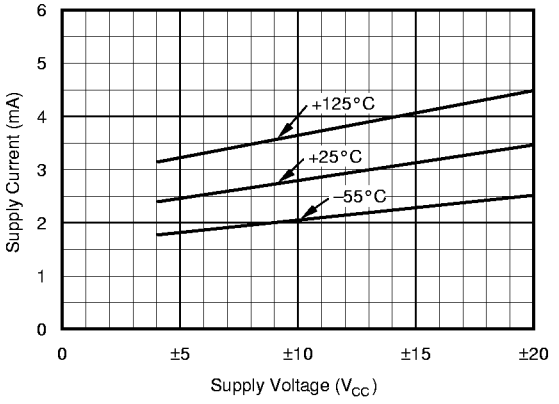
OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE



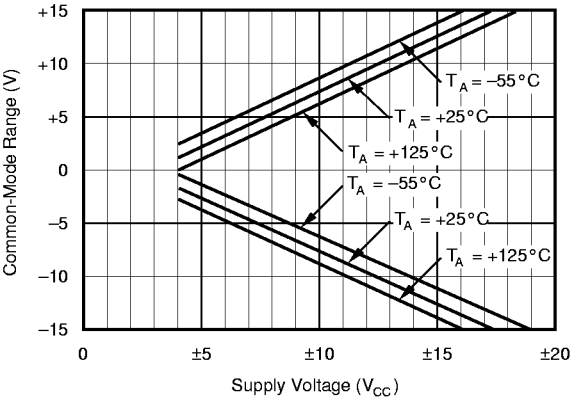
OPEN-LOOP VOLTAGE GAIN vs TEMPERATURE



SUPPLY CURRENT vs SUPPLY VOLTAGE



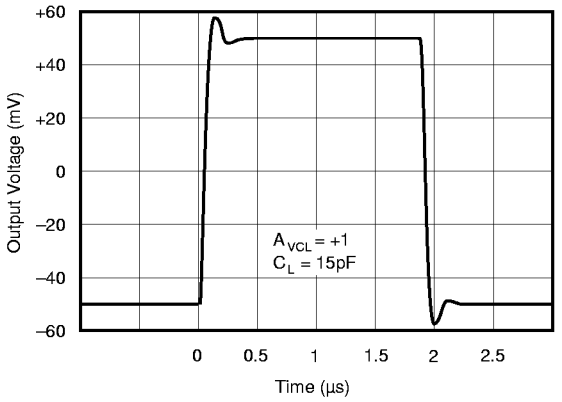
COMMON-MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE



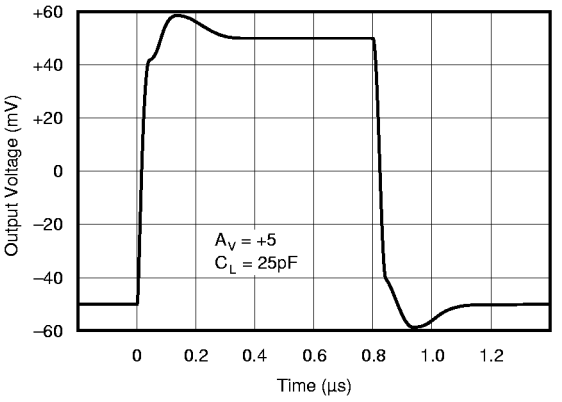
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, $\pm V_{CC}$ = ±15VDC, unless otherwise noted.

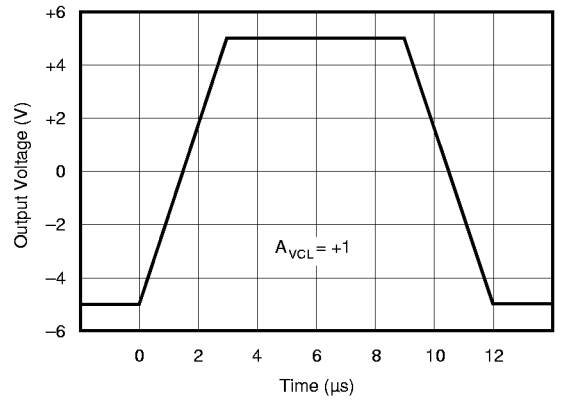
OPA27 SMALL SIGNAL TRANSIENT RESPONSE



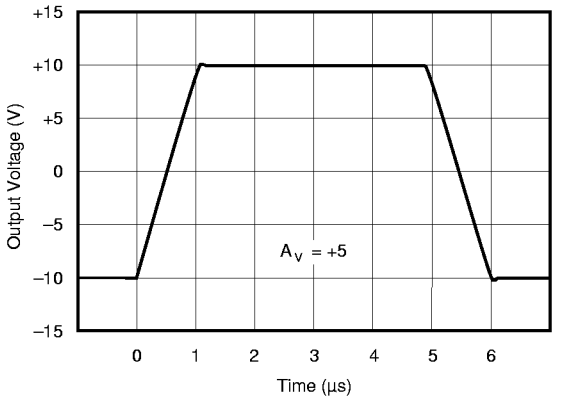
OPA37 SMALL SIGNAL TRANSIENT RESPONSE



OPA27 LARGE SIGNAL TRANSIENT RESPONSE



OPA37 LARGE SIGNAL TRANSIENT RESPONSE



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA27/37 offset voltage is laser-trimmed and will require no further trim for most applications. Offset voltage drift will not be degraded when the input offset is nulled with a 10kΩ trim potentiometer. Other potentiometer values from 1kΩ to 1MΩ can be used but V_{OS} drift will be degraded by an additional 0.1 to 0.2µV/°C. Nulling large system offsets by use of the offset trim adjust will degrade drift performance by approximately 3.3µV/°C per millivolt of offset. Large system offsets can be nulled without drift degradation by input summing.

The conventional offset voltage trim circuit is shown in Figure 3. For trimming very small offsets, the higher resolution circuit shown in Figure 4 is recommended.

The OPA27/37 can replace 741-type operational amplifiers by removing or modifying the trim circuit.

THERMOELECTRIC POTENTIALS

The OPA27/37 is laser-trimmed to microvolt-level input offset voltage and for very low input offset voltage drift.

Careful layout and circuit design techniques are necessary to prevent offset and drift errors from external thermoelectric potentials. Dissimilar metal junctions can generate small EMFs if care is not taken to eliminate either their sources (lead-to-PC, wiring, etc.) or their temperature difference. See Figure 11.

Short, direct mounting of the OPA27/37 with close spacing of the input pins is highly recommended. Poor layout can result in circuit drifts and offsets which are an order of magnitude greater than the operational amplifier alone.

NOISE: BIPOLAR VERSUS FET

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases, so consider the effect of source resistance on overall operational amplifier noise performance. At low source impedances, the lower voltage noise of a bipolar operational amplifier is superior, but at higher impedances the high current noise of a bipolar amplifier becomes a serious liability. Above about 15kΩ the Burr-Brown OPA111 low-noise FET operational amplifier is recommended for lower total noise than the OPA27 (see Figure 5).

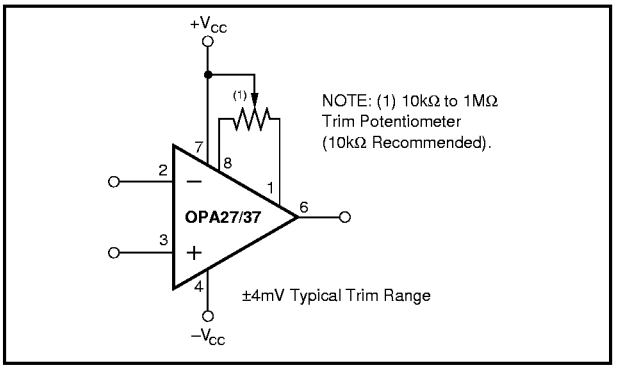


FIGURE 3. Offset Voltage Trim.

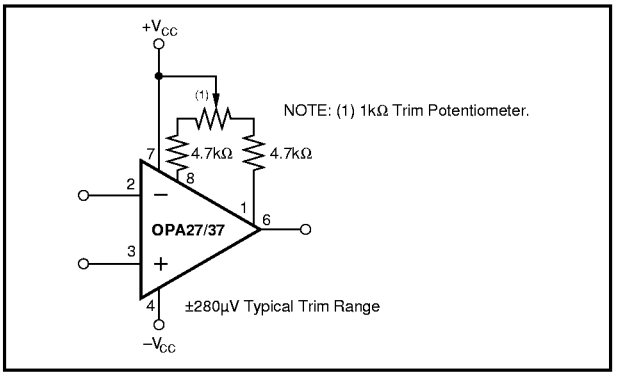


FIGURE 4. High Resolution Offset Voltage Trim.

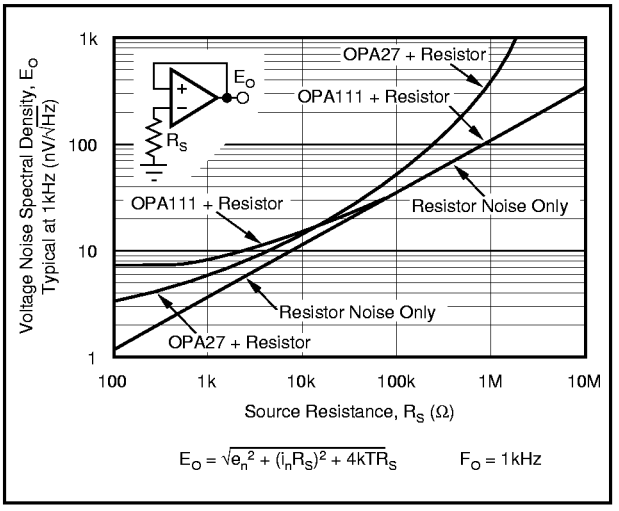


FIGURE 5. Voltage Noise Spectral Density Versus Source Resistance.

COMPENSATION

Although internally compensated for unity-gain stability, the OPA27 may require a small capacitor in parallel with a feedback resistor (R_F) which is greater than 2kΩ. This capacitor will compensate the pole generated by R_F and C_{IN} and eliminate peaking or oscillation.

INPUT PROTECTION

Back-to-back diodes are used for input protection on the OPA27/37. Exceeding a few hundred millivolts differential input signal will cause current to flow and without external current limiting resistors the input will be destroyed.

Accidental static discharge as well as high current can damage the amplifier's input circuit. Although the unit may still be functional, important parameters such as input offset voltage, drift, and noise may be permanently damaged as will any precision operational amplifier subjected to this abuse.

Transient conditions can cause feedthrough due to the amplifier's finite slew rate. When using the OP-27 as a unity-gain buffer (follower) a feedback resistor of 1kΩ is recommended (see Figure 6).

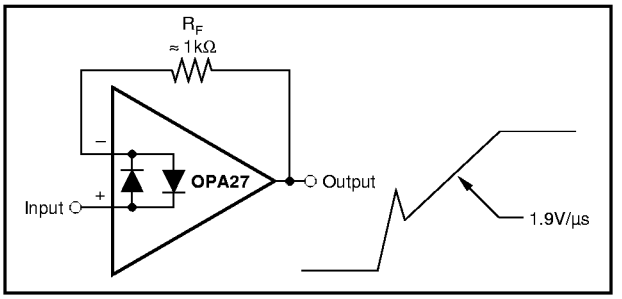


FIGURE 6. Pulsed Operation.

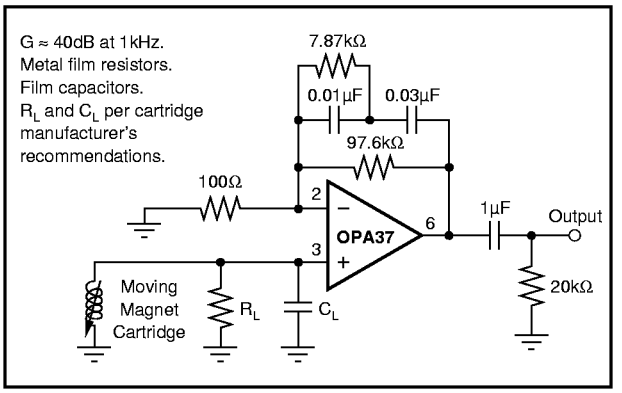


FIGURE 7. Low-Noise RIAA Preamplifier.

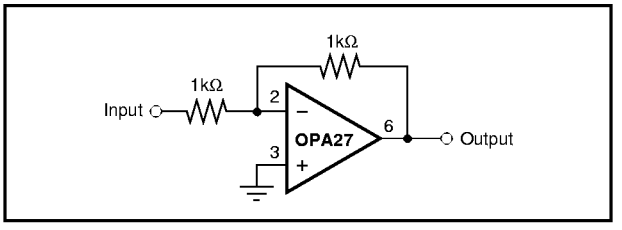


FIGURE 8. Unity-Gain Inverting Amplifier.

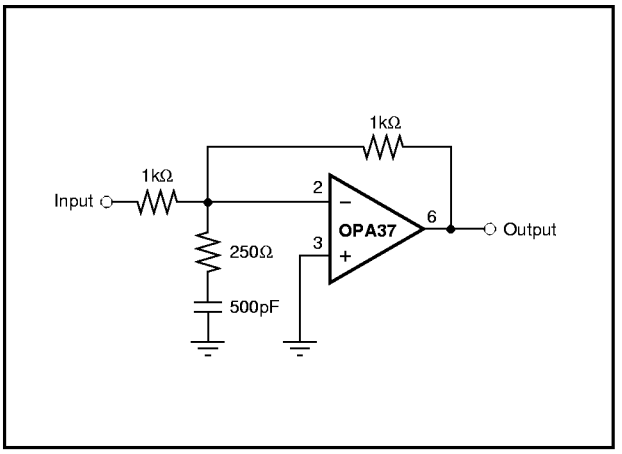


FIGURE 9. High Slew Rate Unity-Gain Inverting Amplifier.

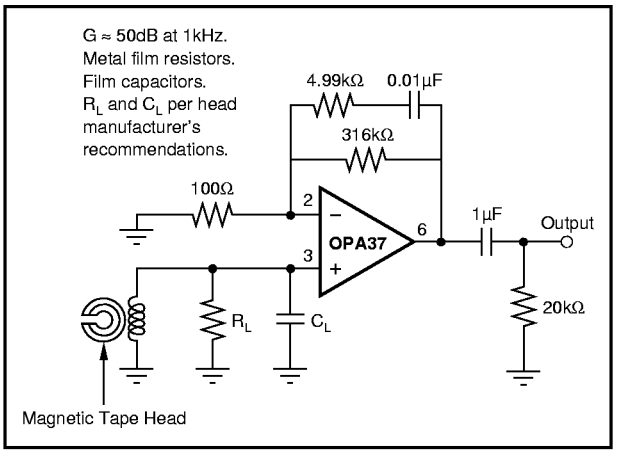


FIGURE 10. NAB Tape Head Preamplifier.

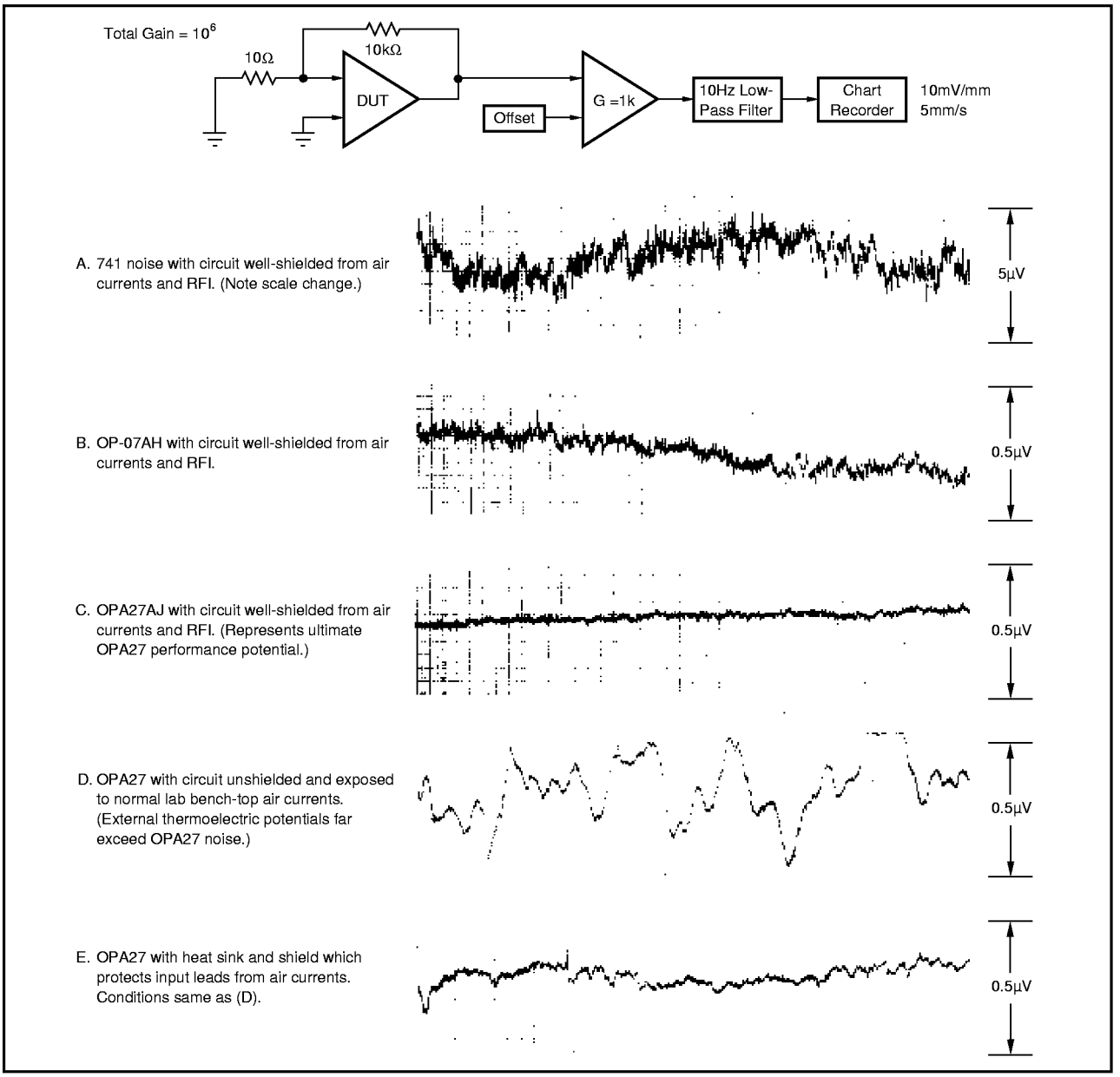


FIGURE 11. Low Frequency Noise Comparison.

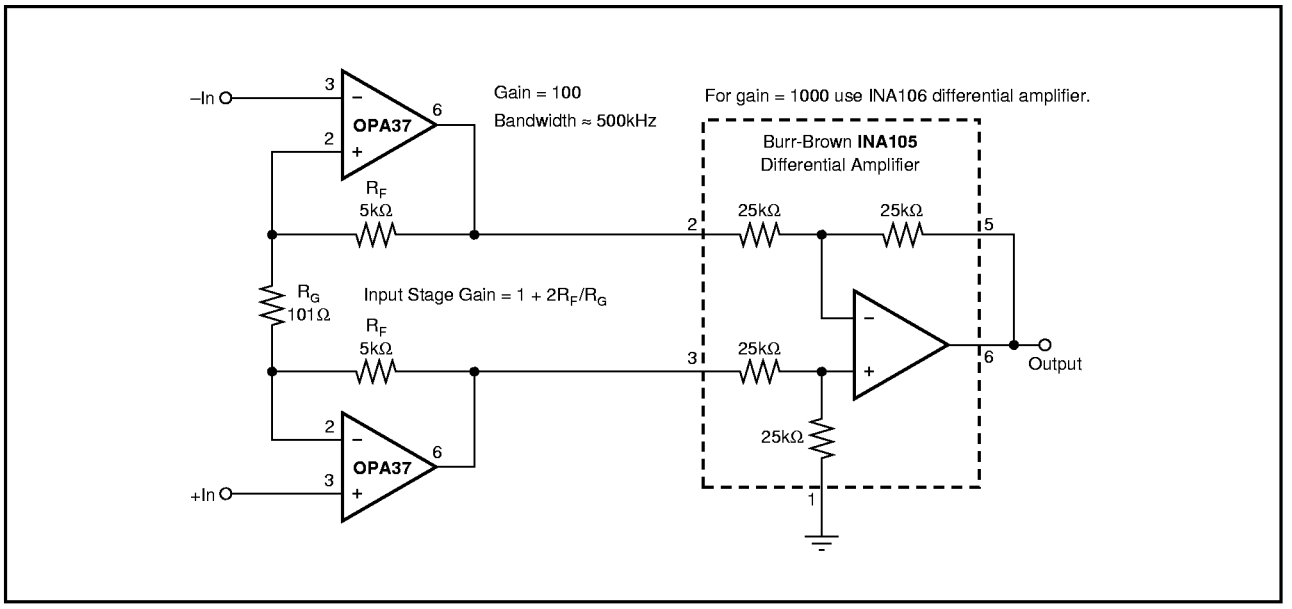


FIGURE 12. Low Noise Instrumentation Amplifier.

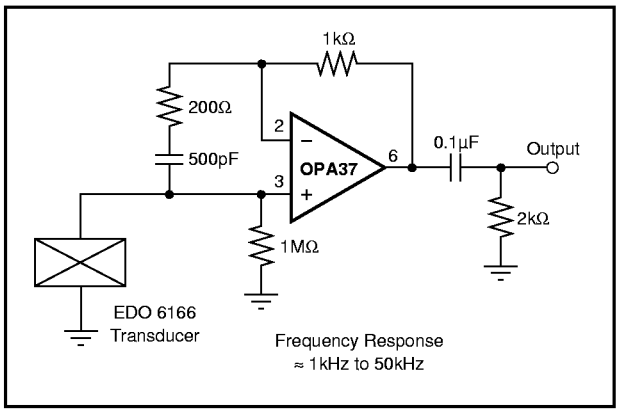


FIGURE 13. Hydrophone Preamplifier.

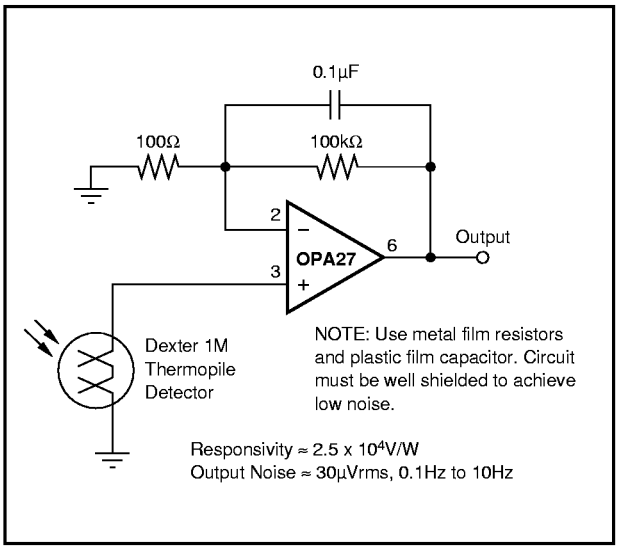


FIGURE 14. Long-Wavelength Infrared Detector Amplifier.

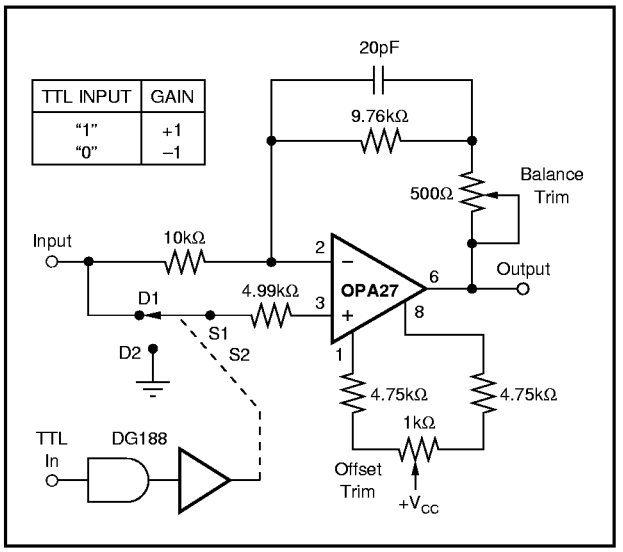


FIGURE 15. High Performance Synchronous Demodulator.

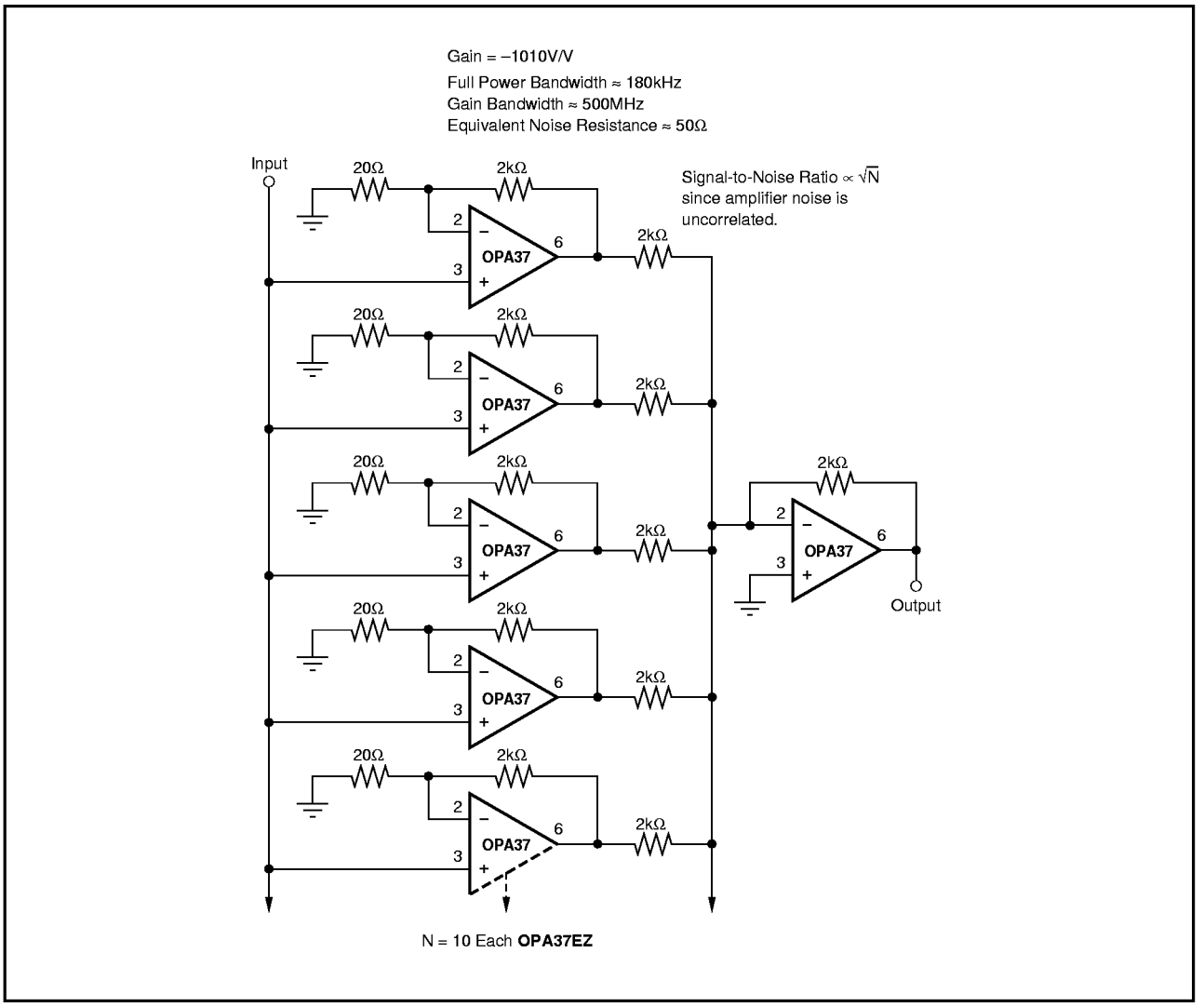


FIGURE 16. Ultra-Low Noise "N" Stage Parallel Amplifier.

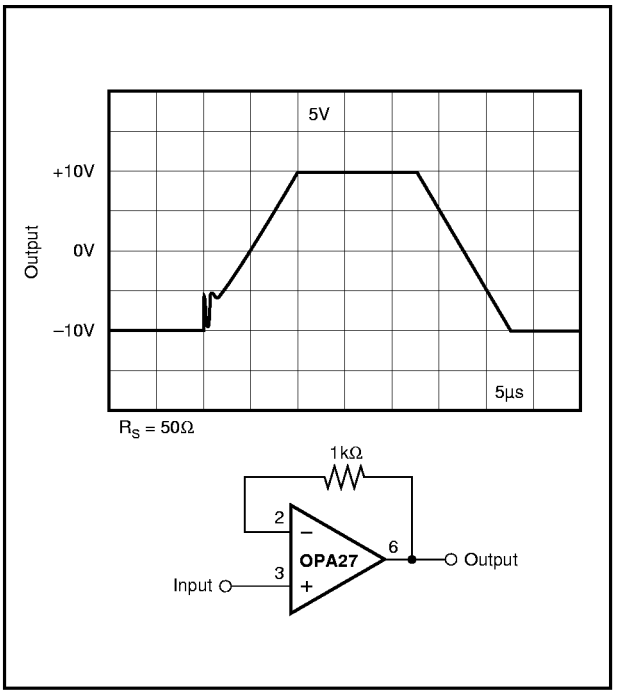


FIGURE 17. Unity-Gain Buffer.

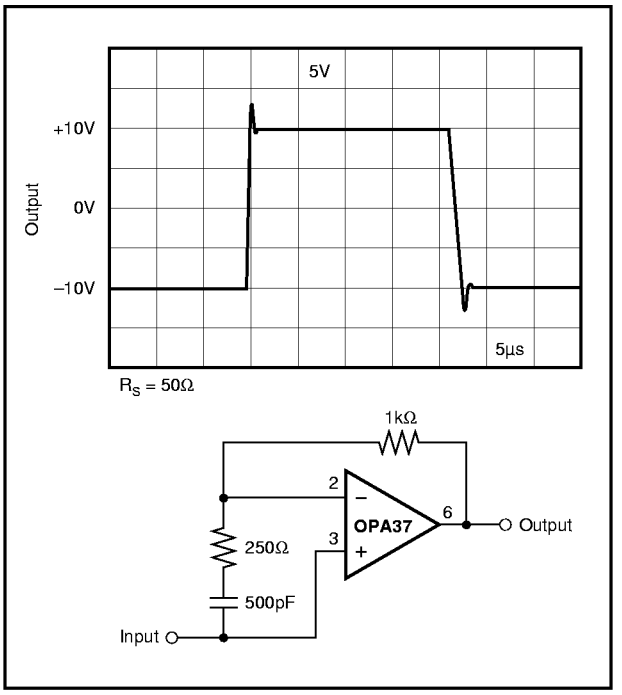


FIGURE 18. High Slew Rate Unity-Gain Buffer.

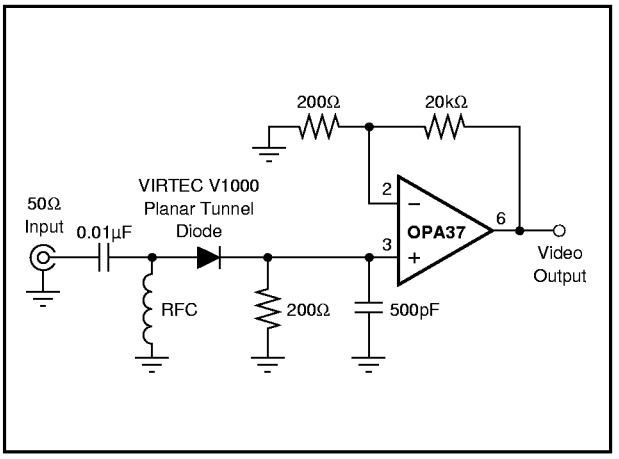


FIGURE 19. RF Detector and Video Amplifier.

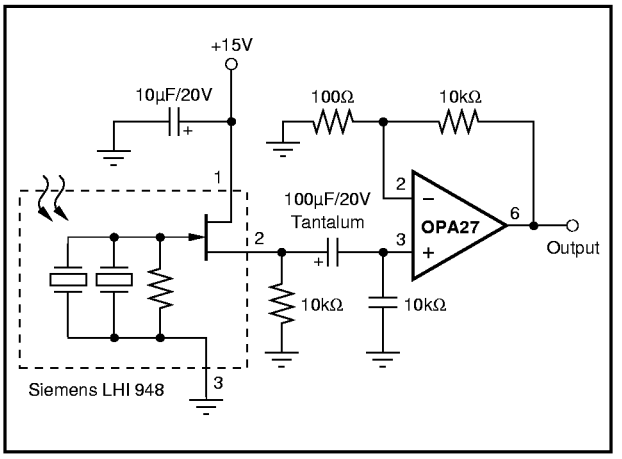


FIGURE 20. Balanced Pyroelectric Infrared Detector.

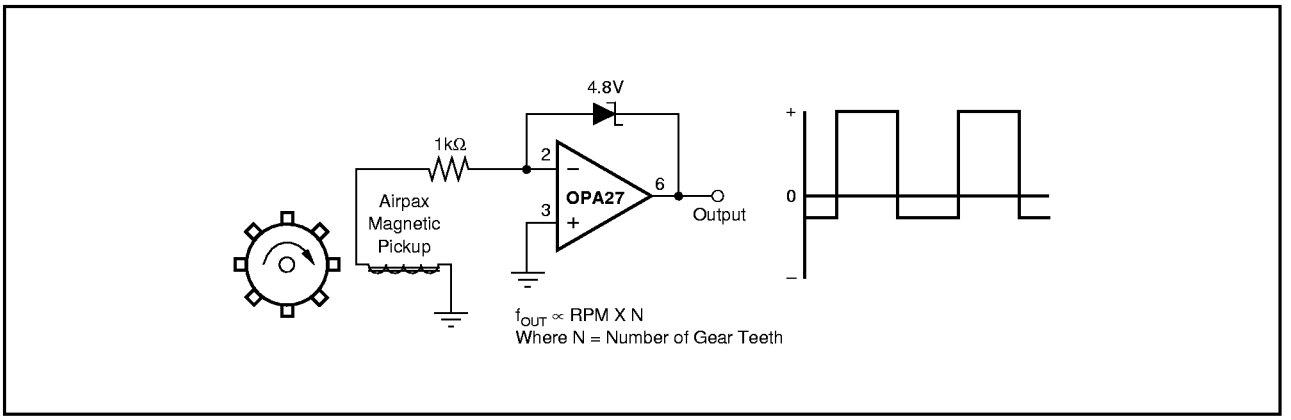
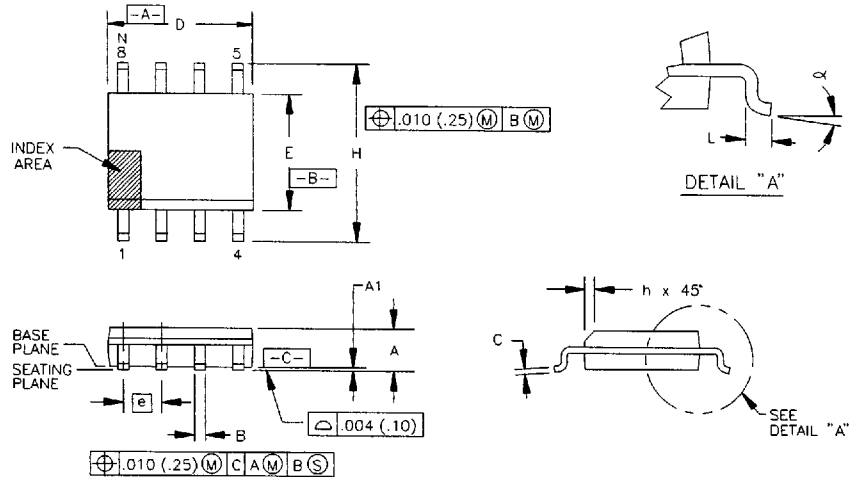


FIGURE 21. Magnetic Tachometer.

Package Number 182 - 8-Lead SOIC



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.0532	.0688	1.35	1.75	
A1	.004	.0098	0.10	0.23	
B	.013	.020	0.33	0.51	7
C	.0075	.0098	0.20	0.25	
D	.189	.1968	4.80	4.98	2
E	.1497	.1574	3.80	4.00	3
e	.050 BASIC		1.27 BASIC		
H	.2284	.244	5.80	6.20	
h	.0099	.0196	0.25	0.50	4
L	.016	.050	0.41	1.27	5
N	8		8		6
α	0°	8°	0°	8°	

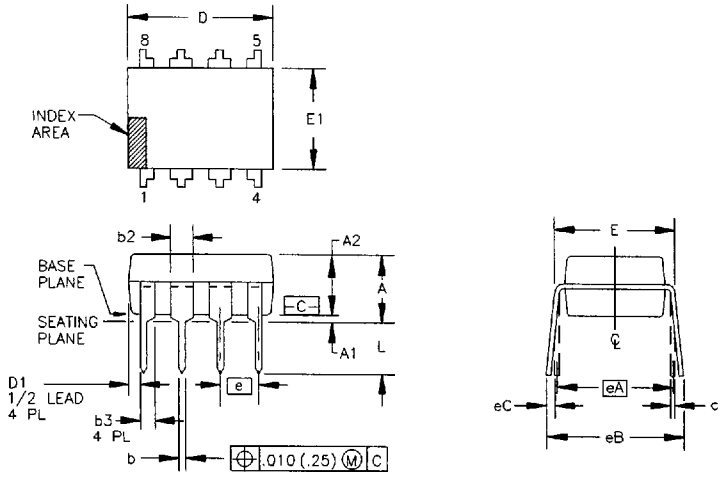
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER:	ZZ182	REV.: H
JEDEC NUMBER:	MS-012-AA	

Package Number 006 - 8-Pin Plastic, Single-Wide DIP



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
b	.014	.022	0.36	0.56	
b2	.045	.070	1.14	1.78	9
b3	.030	.045	0.76	1.14	9
c	.008	.014	0.20	0.36	
D	.355	.400	9.02	10.16	4
D1	.005	--	0.13	--	4
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100 BASIC		2.54 BASIC		
eA	.300 BASIC		7.63 BASIC		5
eB	--	.430	--	10.92	6

DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
eC	.000	.060	0.00	1.52	6
L	.115	.150	2.92	3.81	3
N	8		8		7

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ006	REV.: E
JEDEC NUMBER: MS-001-BA	