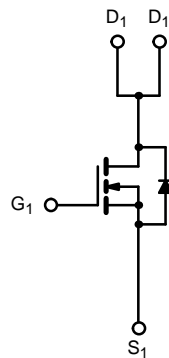
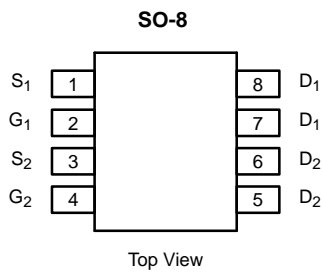




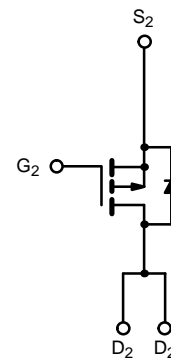
## N-Channel 60-V (D-S), 175°C MOSFET

**175°C Rated**  
Maximum Junction Temperature  
**TrenchFET®**  
Power MOSFETs

PRODUCT SUMMARY			
	V <sub>DS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)
N-Channel	60	0.055 @ V <sub>GS</sub> = 10 V	±4.5
		0.075 @ V <sub>GS</sub> = 4.5 V	±3.9
P-Channel	-60	0.120 @ V <sub>GS</sub> = -10 V	±3.1
		0.150 @ V <sub>GS</sub> = -4.5 V	±2.8



N-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	N-Channel	P-Channel	Unit	
Drain-Source Voltage	V <sub>DS</sub>	60	-60	V	
Gate-Source Voltage	V <sub>GS</sub>	±20	±20		
Continuous Drain Current (T <sub>J</sub> = 175°C) <sup>a</sup>	I <sub>D</sub>	T <sub>A</sub> = 25°C	±4.5	±3.1	A
		T <sub>A</sub> = 70°C	±3.8	±2.6	
Pulsed Drain Current	I <sub>DM</sub>	±30	±30		
Continuous Source Current (Diode Conduction) <sup>a</sup>	I <sub>S</sub>	2.0	-2.0		
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	T <sub>A</sub> = 25°C	2.4		W
		T <sub>A</sub> = 70°C	1.7		
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 175		°C	

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	N- or P- Channel	Unit
Maximum Junction-to-Ambient <sup>a</sup>	R <sub>thJA</sub>	62.5	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.



SPECIFICATIONS (T <sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Condition		Min	Typ <sup>a</sup>	Max	Unit
<b>Static</b>							
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	N-Ch	1			V
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	P-Ch	-1			
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V	N-Ch			±100	nA
			P-Ch			±100	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V	N-Ch			2	μA
		V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0 V	P-Ch			-2	
		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	N-Ch			25	
		V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	P-Ch			-25	
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	N-Ch	20			A
		V <sub>DS</sub> ≤ -5 V, V <sub>GS</sub> = -10 V	P-Ch	-20			
Drain-Source On-State Resistance <sup>b</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4.5 A	N-Ch		0.045	0.055	Ω
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -3.1 A	P-Ch		0.100	0.120	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 3.9 A	N-Ch		0.055	0.075	
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -2.8 A	P-Ch		0.125	0.150	
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 4.5 A	N-Ch		13		S
		V <sub>DS</sub> = -15 V, I <sub>D</sub> = -3.1 A	P-Ch		7.5		
Diode Forward Voltage <sup>b</sup>	V <sub>SD</sub>	I <sub>S</sub> = 2.0 A, V <sub>GS</sub> = 0 V	N-Ch		0.9	1.2	V
		I <sub>S</sub> = -2.0 A, V <sub>GS</sub> = 0 V	P-Ch		-0.8	-1.2	
<b>Dynamic<sup>a</sup></b>							
Total Gate Charge	Q <sub>g</sub>	N-Channel V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4.5 A  P-Channel V <sub>DS</sub> = -30 V, V <sub>GS</sub> = -10 V I <sub>D</sub> = -3.1 A	N-Ch		19	30	nC
Gate-Source Charge	Q <sub>gs</sub>		N-Ch		4		
Gate-Drain Charge	Q <sub>gd</sub>		N-Ch		3		
Turn-On Delay Time	t <sub>d(on)</sub>	N-Channel V <sub>DD</sub> = 30 V, R <sub>L</sub> = 30 Ω I <sub>D</sub> ≅ 1 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 6 Ω  P-Channel V <sub>DD</sub> = -30 V, R <sub>L</sub> = 30 Ω I <sub>D</sub> ≅ -1 A, V <sub>GEN</sub> = -10 V, R <sub>G</sub> = 6 Ω	P-Ch		1.6		ns
Rise Time	t <sub>r</sub>		N-Ch		13	20	
Turn-Off Delay Time	t <sub>d(off)</sub>		P-Ch		8	15	
			N-Ch		11	20	
Fall Time	t <sub>f</sub>		P-Ch		10	20	
			N-Ch		36	60	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	P-Ch		12	25		
		N-Ch		11	20		
		I <sub>F</sub> = 2 A, di/dt = 100 A/μs	N-Ch		35	60	
		I <sub>F</sub> = -2 A, di/dt = 100 A/μs	P-Ch		60	90	

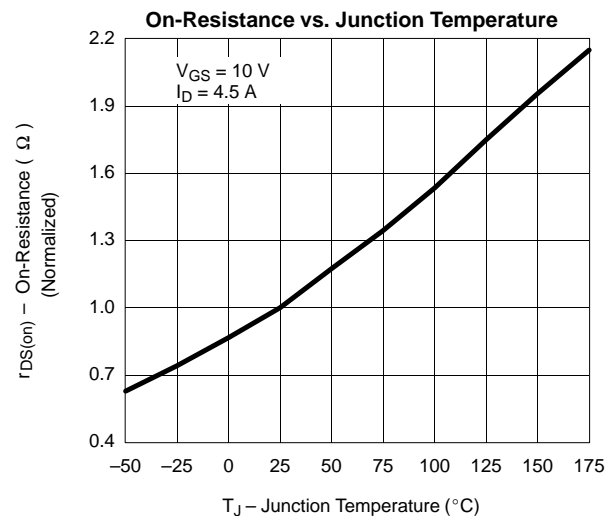
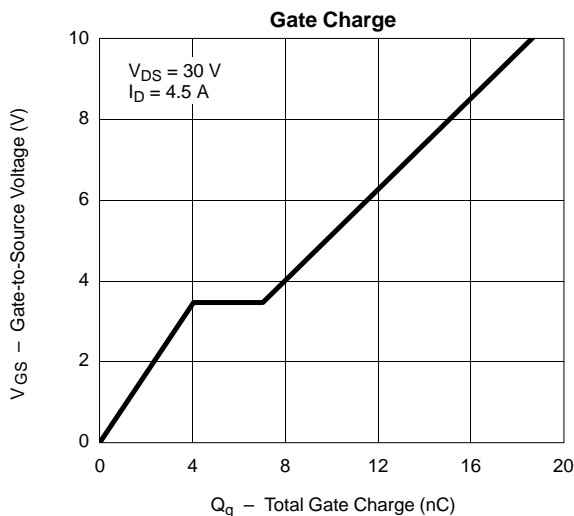
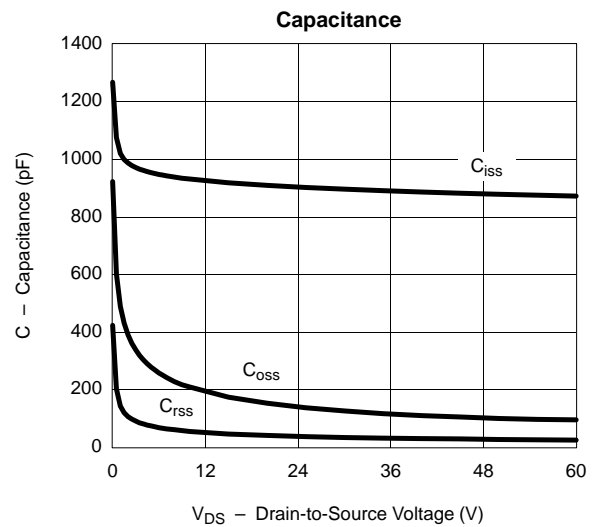
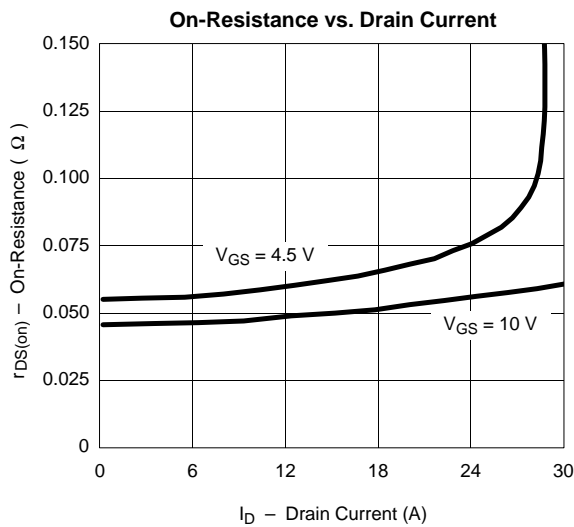
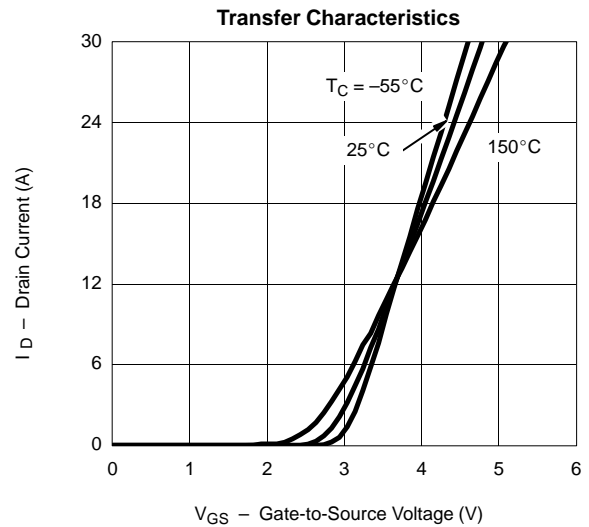
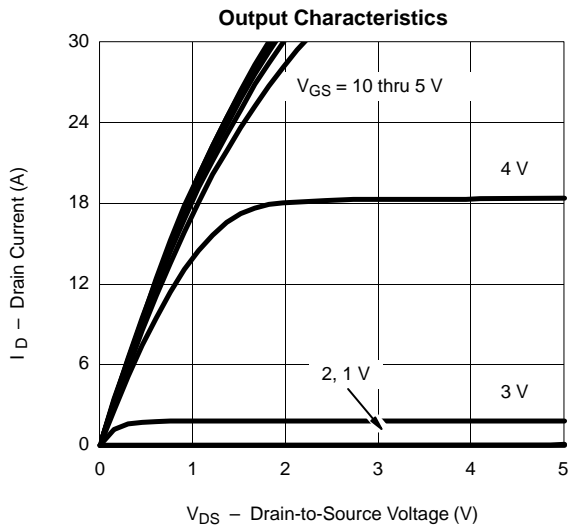
Notes

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

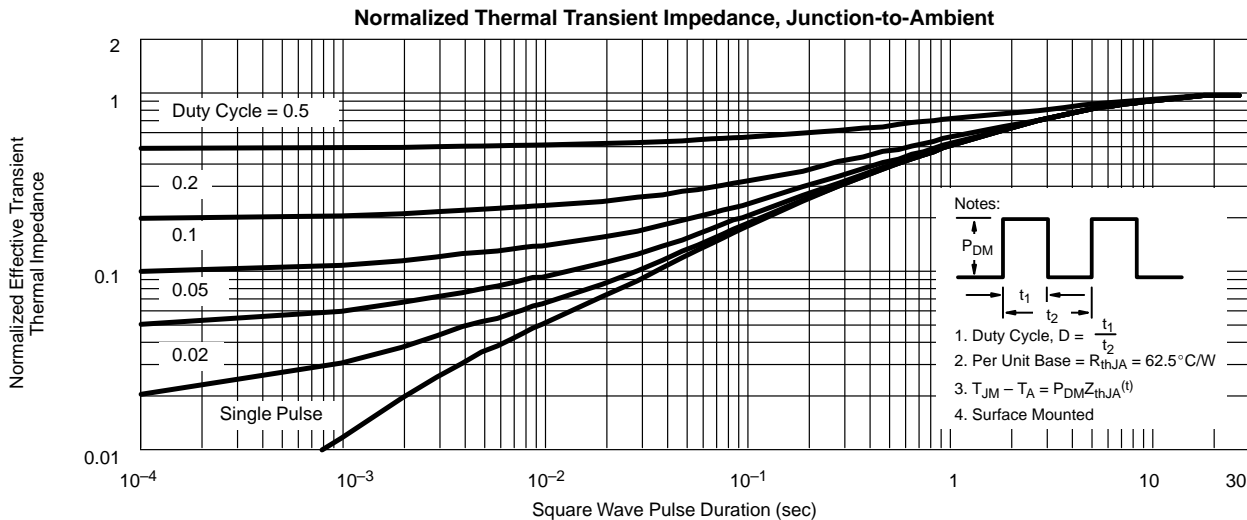
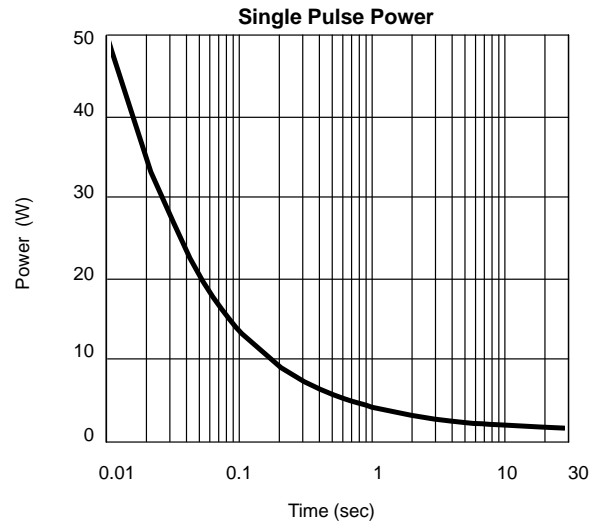
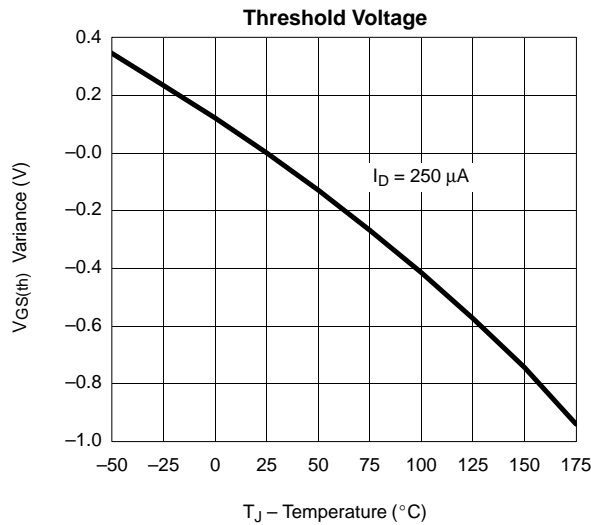
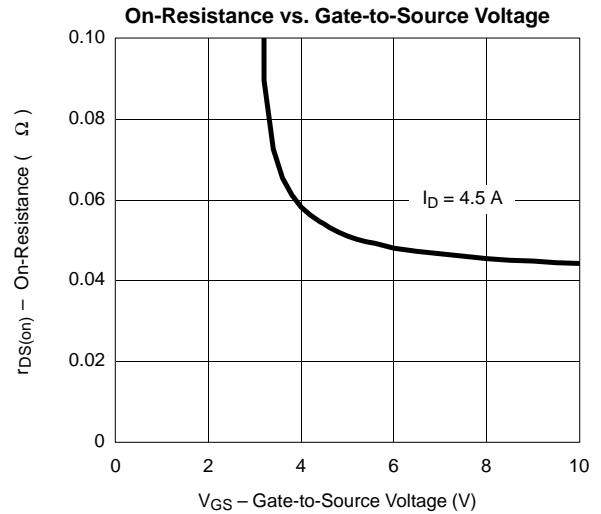
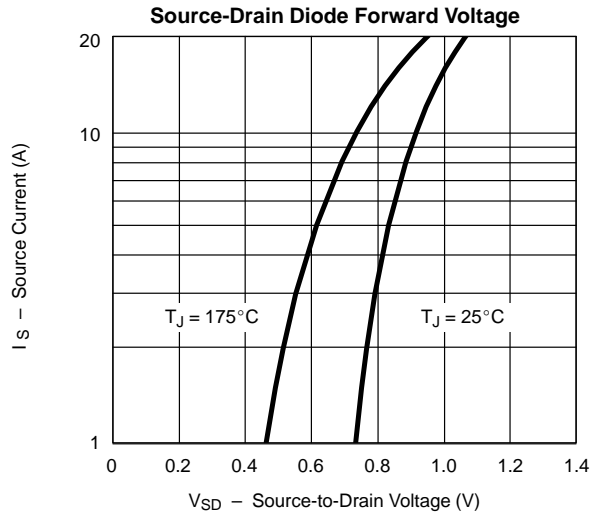


**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

**N-CHANNEL**

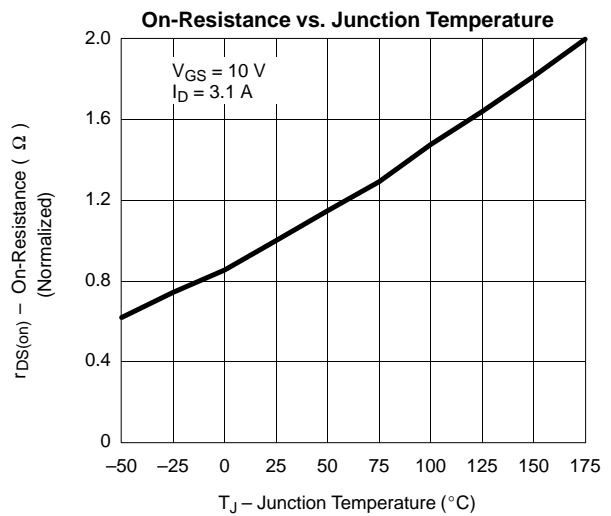
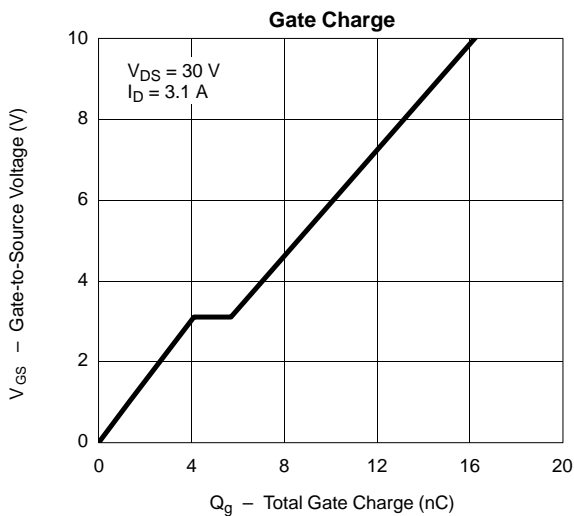
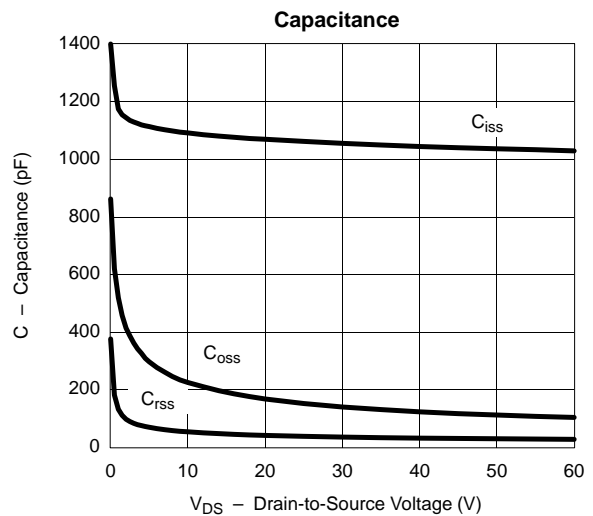
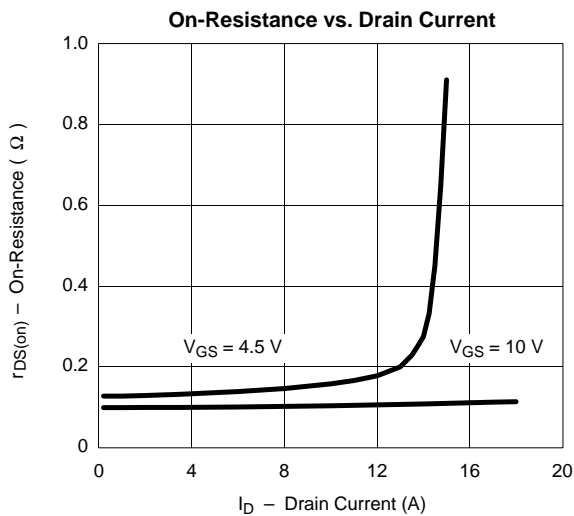
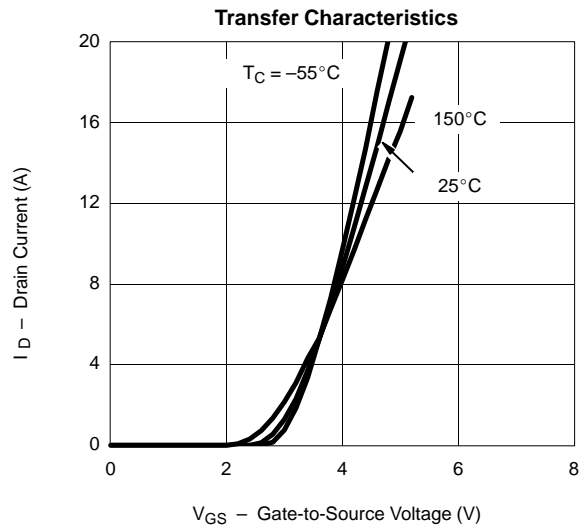
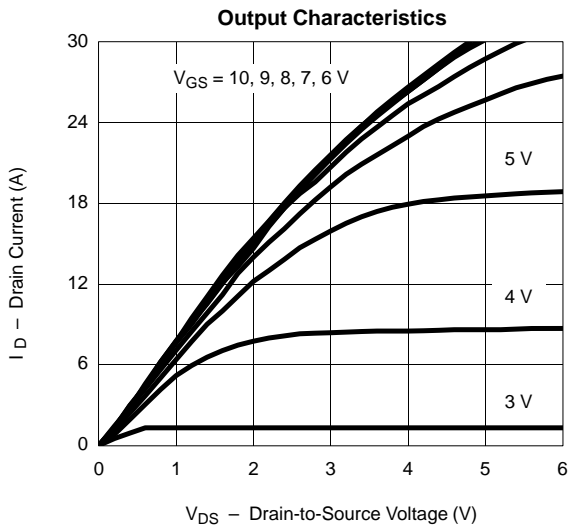


**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) N-CHANNEL**

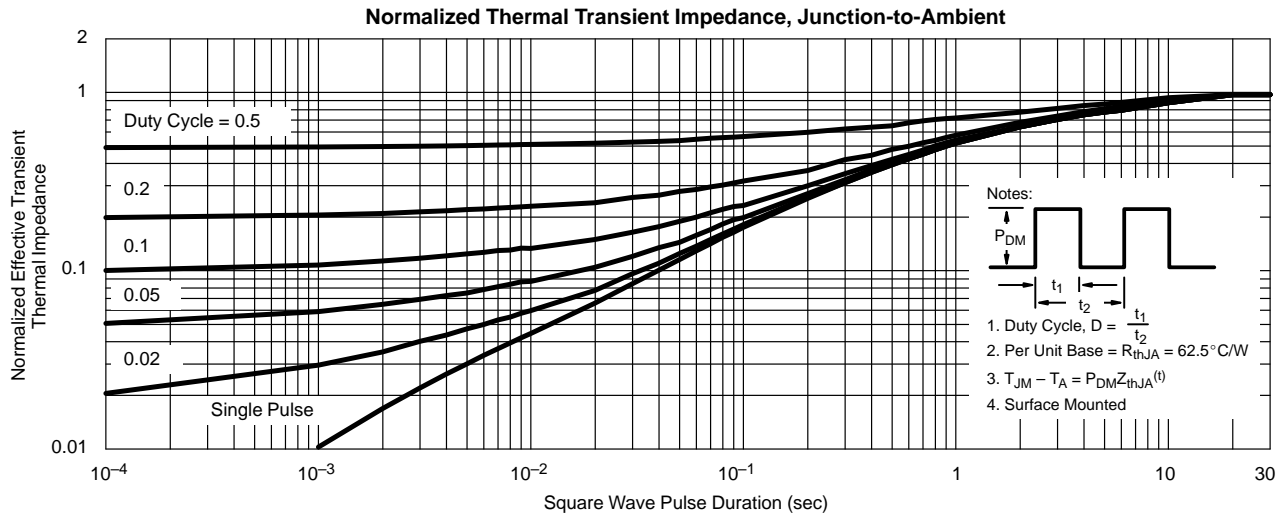
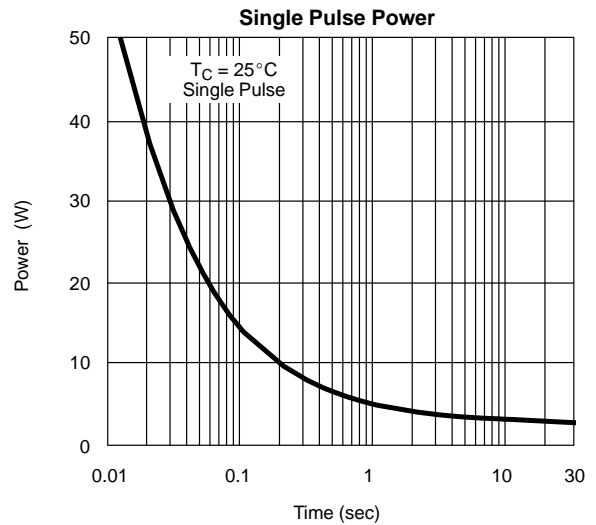
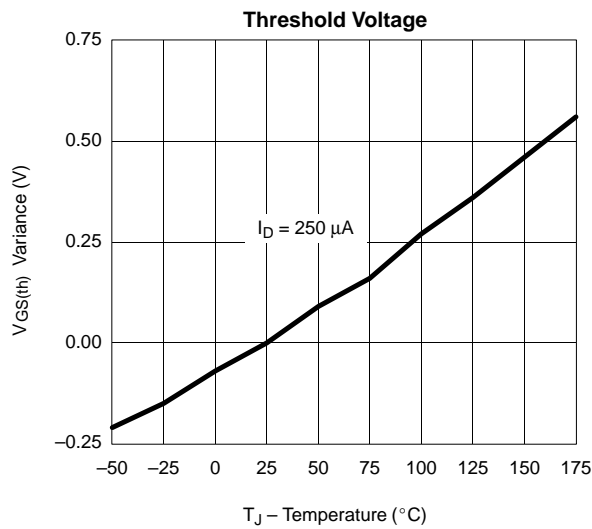
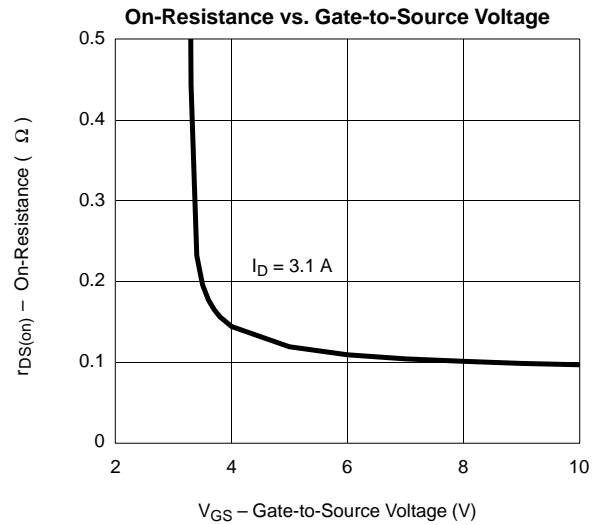
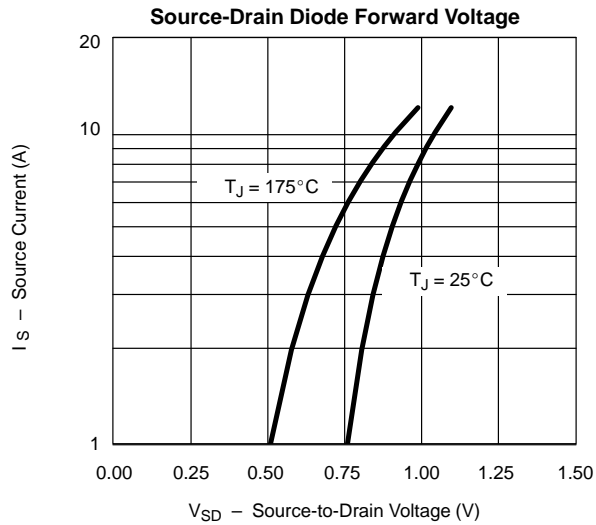




**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) P-CHANNEL**



**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) P-CHANNEL**





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