QUALITY SEMICONDUCTOR, INC.

QuickSwitch® Products High-Speed CMOS 10-Bit Low Resistance QuickSwitch with Precharged Outputs

FEATURES/BENEFITS

- 2.5Ω bidirectional switches connect inputs to outputs
- Zero propagation delay
- Undershoot clamp diodes on all switch and control pins
- Outputs precharge voltage to minimize signal distortion during live insertion
- TTL-compatible input and output levels
- Zero ground bounce
- Available in 24-pin SOIC(SO) and QSOP

DESCRIPTION

The QS3R800 is a 10-bit high-speed CMOS bus switch controlled by a single enable ($\overline{ON}$) input. When $\overline{ON}$ is LOW, the switch is on and port A is connected to port B. When $\overline{ON}$ is HIGH, the switch between port A and port B is open and port B is precharged to the bias voltage. The low ON resistance (2.5Ω) of the QS3R800 allows inputs to be connected to outputs without adding propagation delay and without generating additional noise. The QS3R800 also precharges the B port to a user-selectable bias voltage to minimize live-insertion noise which is uselful in VME bus applications.

Figure 1. Functional Block Diagram

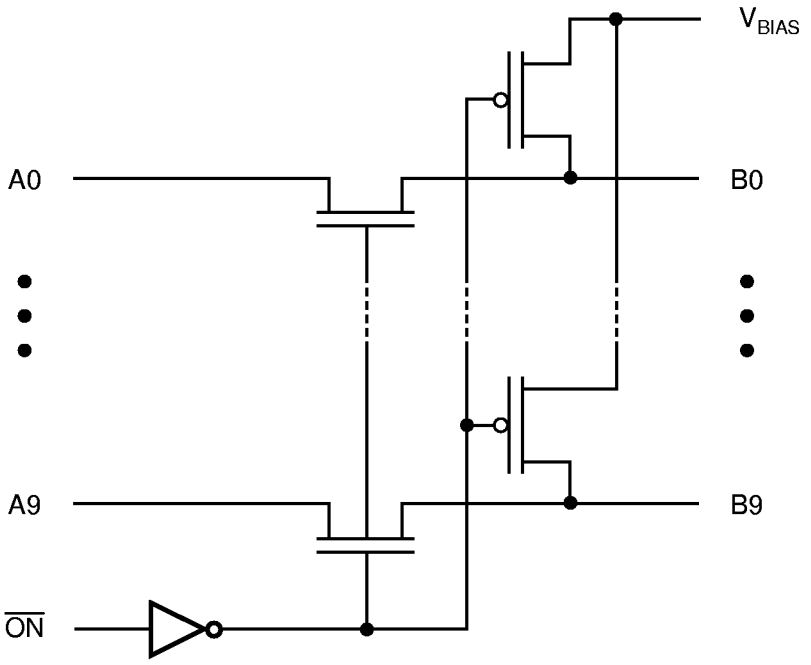

Table 1. Pin Description

Name	I/O	Function
A0-A9	I/O	Bus A
B0-B9	I/O	Bus B
$\overline{ON}$	I	Bus Switch Enable
V_{BIAS}	I	Bias Voltage

Figure 2. Pin Configuration

(All Pins Top View)

SOIC, QSOP

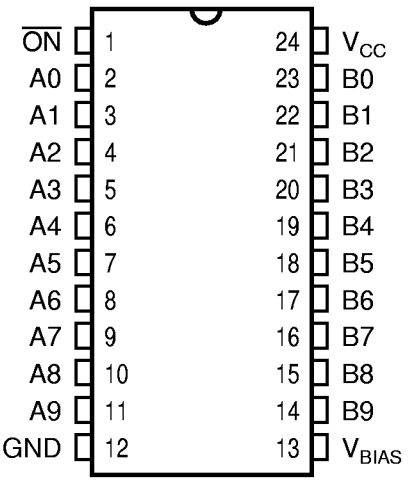

Table 2. Function Table

$\overline{ON}$	B0-B9	Function
L	A0-A9	Connect
H	V_{BIAS}	Precharge

Table 3. Absolute Maximum Ratings

Supply Voltage to Ground	–0.5V to 7.0V
Bias Voltage Range, BIAS V	–0.5V to V_{CC}
DC Input Voltage V_{IN}	–0.5V to V_{CC} + 0.5V
AC Input Voltage (for a pulse width ≤ 20ns)	–3.0V
DC Output Current Max. Sink Current/Pin	128mA
Input Clamp Current	–50mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	–65° to 150°C

Note: ABSOLUTE MAXIMUM CONTINUOUS RATINGS are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum conditions is not implied.

Table 4. Capacitance

T_A = 25°C, f = 1MHz, V_{IN} = 0V

Pins	QSOP, SOIC		Unit
	Typ	Max	
Control Inputs	3	4	pF
QuickSwitch Channels (Switch OFF)	5	6	pF

Note: Capacitance is characterized but not tested. For total capacitance while the switch is ON, please see Section 1 under "input and switch capacitance."

Table 5. DC Electrical Characteristics Over Operating Range

Commercial: T_A = –40°C to 85°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V
V_{BIAS}	Bias Voltage	V_{CC} = 5V	1.3	—	V_{CC}	V
I_O	Bias Current	V_{CC} = 4.5V, V_{BIAS} = 2.4V, V_0 =0 $\overline{ON}$ = High	0.25	—	—	mA
$\lvert I_{IN} \rvert$	Input Leakage Current (Control inputs)	$0 \le V_{IN} \le V_{CC}$	—	—	1	µA
$\lvert I_{OZ} \rvert$	Off-State Current (Hi-Z)	$0 \le V_{OUT} \le V_{CC}$	—	—	1	µA
R_{ON}	Switch ON Resistance(2)	V_{CC} = Min., V_{IN} = 0.0V I_{ON} = 30mA	—	2.5	4	Ω
R_{ON}	Switch ON Resistance(2)	V_{CC} = Min., V_{IN} = 2.4V I_{ON} = 15 mA	—	4	5.5	Ω

Notes:
1. Typical values indicate V_{CC} = 5.0V and T_A = 25°C.
2. During input/output leakage, testing all pins are at HIGH or LOW state.
3. For a diagram explaining the procedure for R_{ON} measurement, please see Section1 under "DC Electrical Characteristics."
3. Max. value of R_{ON} guaranteed by characterization, but not production tested.

Figure 3. Typical ON Resistance vs V_{IN} at V_{CC} = 5.0V

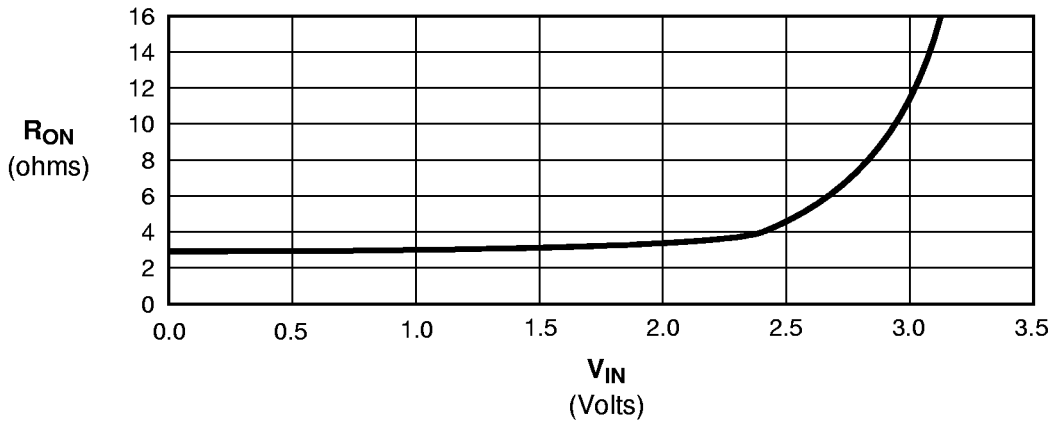

Table 6. Power Supply Characteristics Over Operating Range

T_A = –40°C to 85°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions[1]	Typ[2]	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}, f = 0	0.2	3.0	µA
ΔI_{CC}	Power Supply Current per Input HIGH	V_{CC} = Max., V_{IN} = 3.4V[3], f = 0 per Control Input	—	2.5	mA
Q_{CCD}	Dynamic Power Supply Current per MHz[4]	V_{CC} = Max., A and B Pins Open, Data Inputs = GND, per Control Inputs Toggling @ 50% Duty Cycle	—	0.25	mA/ MHz

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Typical Values are at V_{CC} = 5.0V, 25°C Ambient.
3. Per TTL driven input (V_{IN} = 3.4V, control inputs only). A and B pins do not contribute to ΔI_{CC}.
4. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed by design, but not tested.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Table 7. Switching Characteristics Over Operating Range

Commercial: T_A = –40°C to 85°C, V_{CC} = 5.0V ±10%
C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description[1]	Min	Typ	Max	Unit
t_{PLH} t_{PHL}	Data Propagation Delay[2,3] A to B or B to A	—	—	0.12[3]	ns
t_{PZL} t_{PZH}	Switch Turn-on Delay $\overline{ON}$ to A or B	1.5	—	7.5	ns
t_{PLZ} t_{PHZ}	Switch Turn-off Delay[2] $\overline{ON}$ to A or B	1.5	—	6.5	ns

Notes:
1. See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.12ns for 50pF. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.