

358 8-CHANNEL SINGLE-ENDED MULTIPLEXER  
Logic Diagram

#### FEATURES:

- RAD-PAK<sup>®</sup> technology-hardened against natural space radiation
- Total dose hardness:
  - > 50 krad (Si), depending upon space mission
- Excellent Single Event Effect
  - SEL<sub>TH</sub> > 80 MeV/mg/cm<sup>2</sup>
  - SEU<sub>TH</sub> > 80 MeV/mg/cm<sup>2</sup>
- Package:
  - 16 pin RAD-PAK<sup>®</sup> Flat Pack
- All switches off with power supplies off
- On channel turns OFF if overvoltage occurs
- Only nanoamperes of input current under all fault conditions
- Operates from ±4.5 to ±18V supplies
- All digital inputs are TTL and CMOS compatible
- Significantly reduced power consumption

#### DESCRIPTION:

DDC's 358 8-Channel single-ended (1 of 8) multiplexers with fault protection features a greater than 50 krad (Si) total dose tolerance, depending upon space mission. Using a series N-channel, P-channel, N-channel structure, these multiplexers provide significantly improved fault protection. If the power supplies to the fault-protected multiplexer are inadvertently turned off while input voltages are still applied, all channels in the multiplexer are turned off, and only a few nanoamperes of leakage current will flow into the inputs. This protects not only the multiplexer and the circuitry driven by the multiplexer, but also protects the sensors or signal sources which drive the multiplexer. All digital inputs have logic thresholds of 0.8V and 2.4V, ensuring both TTL and CMOS compatibility without requiring pullup resistors. Break-before-make operation is guaranteed. Power supply currents have been reduced and typical power dissipation is less than 2 mW.

DDC's patented RAD-PAK<sup>®</sup> packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or a space mission. In a GEO orbit, Rad-Pak<sup>®</sup> provides true greater than 50 krad (Si) total radiation dose tolerance, dependent upon space mission. This product is available with packaging and screening up to Class S.

TABLE 1. PINOUT DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1, 16, 15	A0-A2	Address Inputs
2	Enable	Enable Inputs
3	-V Supply	Negative Supply Voltage
4-7, 12-9	IN1-IN8	Analog Inputs-bidirectional
8	OUT	Output-bidirectional
13	+V Supply	Positive Supply Voltage
14	GND	Ground

TABLE 2. 358 ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MAX	UNITS
Voltage between Supply Pins V+ V-		+44 +22 -22	V
Digital Input Overvoltage VEN, VA Vsupply (+) Vsupply (-)		+4 -4	V
Analog Input Overvoltage with Multiplexer Power On: VS Vsupply (+) Vsupply (-)		+20 -20	V
Analog Input Overvoltage with Multiplexer Power Off: VS Vsupply (+) Vsupply (-)		+35 -35	V
Continuous Current Peak Current (Pulse at 1 ms, 10% duty cycle max)		20 40	mA
Thermal Impedance	$\Theta_{JC}$	2.69	°C/W
Weight		2.25	Grams
Operating Temperature Range:	$T_A$	-55 to +125	°C
Storage Temperature Range:	$T_S$	-65 to +150	°C

TABLE 3. 358 ELECTRICAL CHARACTERISTICS

 $(V^+ = 15V, V^- = -15V, V_{AH} = 2.4V, V_{AL} = 0.8V, T_A = -55 \text{ TO } +125^\circ\text{C}, \text{ UNLESS OTHERWISE SPECIFIED})$ 

PARAMETER	TEST CONDITIONS	SUBGROUPS	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
STATIC								
ON Resistance	$V_D = \pm 10V, I_S = \pm 100\mu A$ $V_{AL} = 0.8V, V_{AH} = 2.4V$	1, 2, 3	$r_{DS(ON)}$	+25°C Full		1.2 1.5	1.5 1.8	k $\Omega$
OFF Input Leakage Current	$V_S = \pm 10V, V_D = +10V$ $V_{EN} = 0.8V$	1, 2, 3	$I_{S(OFF)}$	+25°C Full		0.03	50	nA
OFF Output Leakage Current	$V_D = \pm 10V, V_S = +10V$ $V_{EN} = 0.8V$	1, 2, 3	$I_{D(OFF)}$	+25°C Full		0.1	200	nA
ON Channel Leakage Current	$V_{S(ALL)} = V_D = \pm 10V^1$ $V_{AH} = V_{EN} = 2.4V$ $V_{AL} = 0.8V$	1, 2, 3	$I_{D(ON)}$	+25°C Full		0.1	200 <sup>2</sup>	nA
Analog Signal Range	<sup>2</sup>	1, 2, 3	$V_{AN}$	Full	-15		15	V
FAULT								
Output Leakage Current (with Overvoltage)	$V_D = 0V^1$ Analog Overvoltage = $\pm 33V$	1, 2, 3	$I_{D(OFF)}$	+25°C Full		4.0	2.0	nA $\mu A$
Input Leakage Current (with Overvoltage)	$V_{IN} = \pm 25V, V_O = \pm 10V^1$	1, 2, 3	$I_{S(OFF)}$	+25°C			5.0	$\mu A$
Input Leakage Current (w/ Power Supplies Off)	$V_{IN} = \pm 25V, V_{EN} = V_O = 0V$ $A_0 = A_1 = A_2 = 0V \text{ or } 5V$	1, 2, 3	$I_{S(OFF)}$	+25°C			2.0	$\mu A$
INPUT								
Input Low Threshold		1, 2, 3	$V_{AL}$	Full			0.8	V
Input High Threshold		1, 2, 3	$V_{AH}$	Full	2.4			V
Input Leakage Current (High or Low)	$V_A = 4V \text{ or } 0V^3$	1, 2, 3	$I_A$	Full			1.0	$\mu A$
DYNAMIC								
Access Time		1, 2, 3	$t_A$	+25°C		0.5	1.0	$\mu s$
Break-Before-Make Delay	$V_{EN} = \pm 5V, V_{IN} = \pm 10V$ $A_0, A_1, A_2$ Strobed	9, 10, 11	$t_{on}, t_{off}$	+25°C	25	80		ns
Enable Delay (ON)		9, 10, 11	$t_{on(EN)}$	+25°C Full		300	500 1000	ns
Enable Delay (OFF)		9, 10, 11	$t_{off(EN)}$	+25°C Full		300	500 1000	ns
Setting Time: (0.1%) (0.01%)		9, 10, 11	$t_{sett}$	+25°C		1.2 3.5		$\mu s$
"OFF Isolation" <sup>4</sup>	$V_{EN} = 0.8V, R_L = 1k\Omega$ $C_L = 15pF, V = 7V_{RMS}$ $f = 100kHz$	4, 5, 6		+25°C	50	68		db

TABLE 3. 358 ELECTRICAL CHARACTERISTICS  
 ( $V^+ = 15V$ ,  $V^- = -15V$ ,  $V_{AH} = 2.4V$ ,  $V_{AL} = 0.8V$ ,  $T_A = -55$  TO  $+125^\circ C$ , UNLESS OTHERWISE SPECIFIED)

PARAMETER	TEST CONDITIONS	SUBGROUPS	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
Channel Input Capacitance <sup>4</sup>		4, 5, 6	$C_{S(OFF)}$	$+25^\circ C$		5		pF
Channel Output Capacitance <sup>4</sup>		4, 5, 6	$C_{D(OFF)}$	$+25^\circ C$		25		pF
Digital Input Capacitance <sup>4</sup>		4, 5, 6	$C_A$	$+25^\circ C$		5		pF
Digital Output Capacitance <sup>4</sup>		4, 5, 6	$C_{DS(OFF)}$	$+25^\circ C$		0.1		pF
SUPPLY								
Positive Supply Current	$V_{EN} = 0.8V$ or $2.4V$ $V_A = 0V$ or $5V$	1, 2, 3	I+	$+25^\circ C$ Full		0.1 0.3	0.6 0.7	mA
Negative Supply Current	$V_{EN} = 0.8V$ or $2.4V$ $V_A = 0V$ or $5V$	1, 2, 3	I-	$+25^\circ C$ Full		0.01 0.02	0.1 0.2	mA
Power Supply Range for Continuous Operation	<sup>5</sup>	1, 2, 3	$V_{OP}$	$+25^\circ C$	$\pm 4.5$		$\pm 18$	V

1. The value shown is the steady state value. The transient leakage is typically  $10 \mu A$ .
2. When the analog signal exceeds  $+13.5V$  or  $-12V$  the blocking action of the gate structure goes into operation. Only leakage currents flow and the channel on resistance rises to infinity.
3. Digital input leakage is primarily due to the clamp diodes. Typical leakage is less than  $1 nA$  @  $+25^\circ C$ .
4. Guaranteed by design.
5. Electrical characteristics, such as ON Resistance, will change when power supplies other than  $\pm 15V$  are used.

FIGURE 1. INPUT LEAKAGE VS. INPUT VOLTAGE WITH  $V_+ = V_- = 0V$

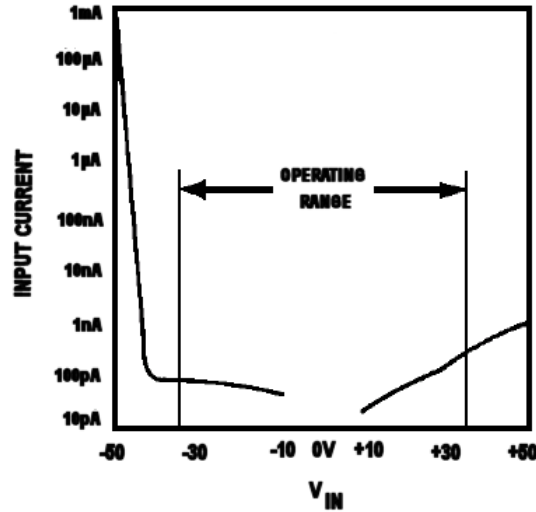


FIGURE 2. OFF CHANNEL LEAKAGE CURRENT VS. INPUT VOLTAGE WITH  $\pm 15V$  SUPPLIES

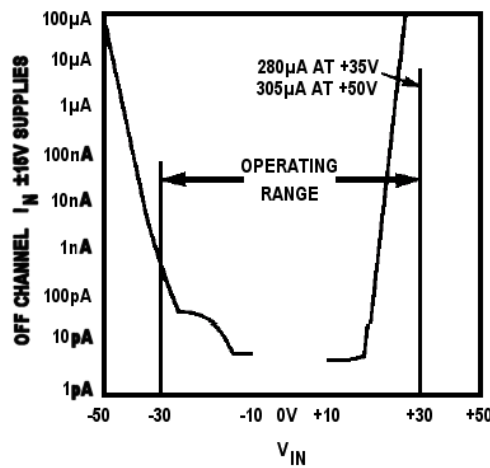


FIGURE 3. OUTPUT LEAKAGE VS. OFF CHANNEL OVERVOLTAGE WITH  $\pm 15V$  SUPPLIES

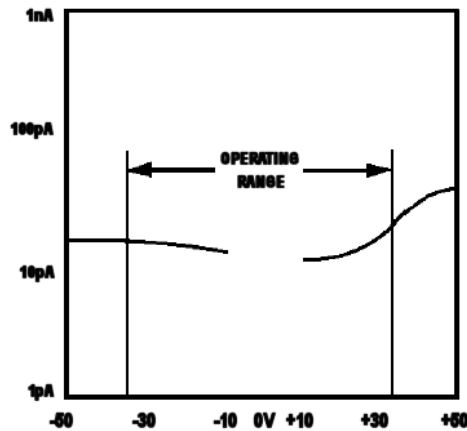
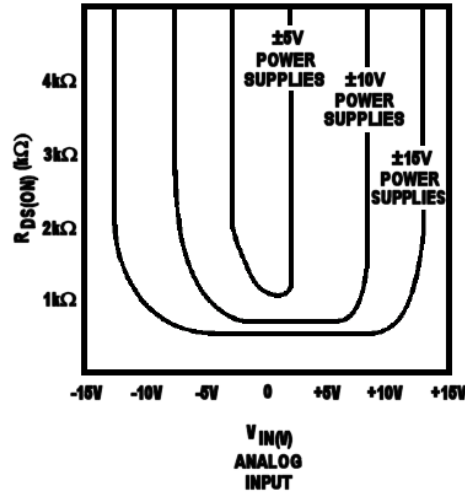


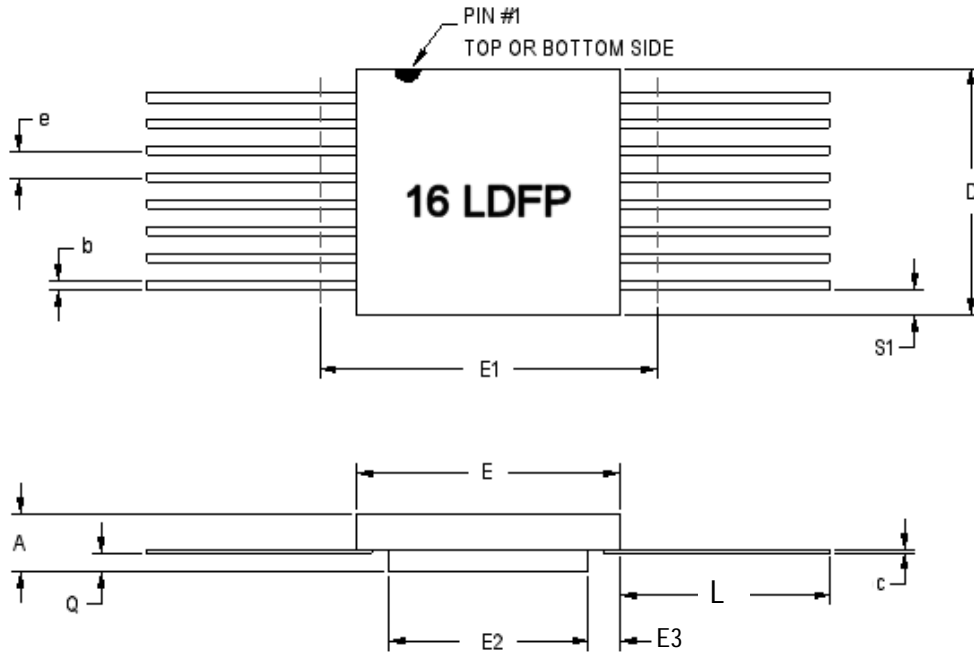
FIGURE 4.  $R_{DS(ON)}$  VS. INPUT VOLTAGE



## TRUTH TABLE

A2	A1	A0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" =  $V_{AL} \leq 0.8V$ , Logic "1" =  $V_{AH} \geq 2.4V$



16-PIN RAD-PAK<sup>®</sup> FLAT PACK PACKAGE

SYMBOL	DIMENSIONS		
	MIN	NOM	MAX
A	.115	.135	.150
b	.015	.017	.019
c	.004	.005	.007
D	0.407	.415	.423
E	.275	.280	.285
E1	--	--	0.500
E2	.150	.156	0.162
E3	.030	.062	--
e	.050 BSC		
L	.325	.335	.345
Q	.020	.033	.045
S1	.005	.024	0.045
N	16		

All dimensions in inches

## Important Notice:

These data sheets are created using the chip manufacturer's published specifications. DDC verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and DDC assumes no responsibility for the use of this information.

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Any claim against DDC must be made within 90 days from the date of shipment from DDC. DDC's liability shall be limited to replacement of defective parts.



# 8-Channel Fault-Protected Analog Multiplexer

# 358

## Product Ordering Options

