



CY74FCT16952T CY74FCT162952T CY74FCT162H952T

16-Bit Registered Transceivers

Features

- Low power, pin-compatible replacement for ABT functions
- FCT-C speed at 6.3 ns
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000 V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Extended commercial range of -40°C to +85°C
- $V_{CC} = 5V \pm 10\%$

CY74FCT16952T Features:

- 64 mA sink current (Com'1), 32 mA source current (Com'1)
- Typical V_{OLP} (ground bounce) < 1.0V at $V_{CC} = 5V, T_A = 25^\circ C$

CY74FCT162952T Features:

- **Balanced output drivers: 24 mA**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) < 0.6V at $V_{CC} = 5V, T_A = 25^\circ C$**

CY74FCT162H952T Features:

- **Bus hold retains last active state**
- **Eliminates the need for external pull-up or pull-down resistors**

Functional Description

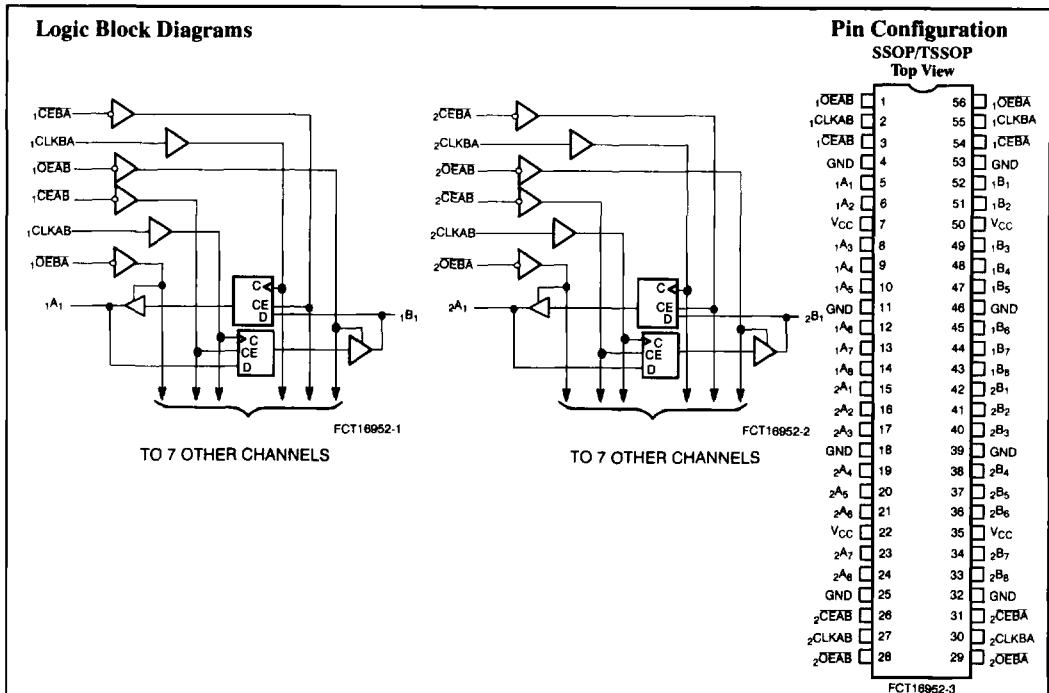
These 16-bit registered transceivers are high-speed, low-power devices. 16-bit operation is achieved by connecting the control lines of the two 8-bit registered transceivers together. For data flow from bus A-to-B, \overline{CEAB} must be LOW to allow data to be stored when CLKAB transitions from LOW-to-HIGH. The stored data will be present on the output when \overline{OEAB} is LOW. Control of data from B-to-A is similar and is controlled by

using the \overline{CEBA} , CLKBA, and \overline{OEBA} inputs. The output buffers are designed with a power-off disable feature to allow for live insertion of boards.

The CY74FCT16952T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162952T has 24-mA balanced output drivers with current-limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162952T is ideal for driving transmission lines.

The CY74FCT162H952T is a 24-mA balanced output part that has "bus hold" on the data inputs. The device retains the input's last state whenever the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.



Pin Description

Name	Description
\overline{OEAB}	A-to-B Output Enable Input (Active LOW)
\overline{OEBA}	B-to-A Output Enable Input (Active LOW)
\overline{CEAB}	A-to-B Clock Enable Input (Active LOW)
\overline{CEBA}	B-to-A Clock Enable Input (Active LOW)
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A	A-to-B Data Inputs or B-to-A Three-State Outputs ^[1]
B	B-to-A Data Inputs or A-to-B Three-State Outputs ^[1]

Maximum Ratings^[5, 6]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	Com'l	-55°C to +125°C
Ambient Temperature with Power Applied	Com'l	-55°C to +125°C
DC Input Voltage		-0.5V to +7.0V
DC Output Voltage		-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)		-60 to +120 mA

Notes:

- On the CY74FCT162H952T these pins have bus hold.
- A-to-B data flow is shown; B-to-A data flow is similar but uses, \overline{CEBA} , CLKBA, and \overline{OEBA} .
- H = HIGH Voltage Level.
L = LOW Voltage Level.
X = Don't Care.
↕ = LOW-to-HIGH Transition.
Z = HIGH Impedance.

Function Table^[2, 3]

For A-to-B (Symmetric with B-to-A)

Inputs			Outputs	
CEAB	CLKAB	\overline{OEAB}	A	B
H	X	L	X	B ^[4]
X	L	L	X	B ^[4]
L	↕	L	L	L
L	↕	L	H	H
X	X	H	X	Z

Power Dissipation	1.0W
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2001V

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	-40°C to +85°C	5V ± 10%

- Level of B before the indicated steady-state input conditions were established.
- Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.



Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[10]	Max.	Unit
V _{IH}	Input HIGH Voltage		2.0			V
V _{IL}	Input LOW Voltage				0.8	V
V _H	Input Hysteresis ^[7]			100		mV
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V
I _{IH}	Input HIGH Current	Standard	V _{CC} =Max., V _I =V _{CC}		±1	μA
		Bus Hold			±100	
I _{IL}	Input LOW Current	Standard	V _{CC} =Max., V _I =GND		±1	μA
		Bus Hold			±100	
I _{BBH} I _{BBL}	Bus Hold Sustain Current on Bus Hold Input ^[8]	V _{CC} =Min.	V _I =2.0V	-50		μA
			V _I =0.8V	+50		
I _{BHIH} I _{BHLO}	Bus Hold Overdrive Current on Bus Hold Input ^[7]	V _{CC} =Max., V _I =1.5V			TBD	mA
I _{OZH}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =2.7V			±1	μA
I _{OZL}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =0.5V			±1	μA
I _{OS}	Short Circuit Current ^[9]	V _{CC} =Max., V _{OUT} =GND	-80	-140	-200	mA
I _O	Output Drive Current ^[9]	V _{CC} =Max., V _{OUT} =2.5V	-50		-180	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} ≤ 4.5V			±1	μA

Output Drive Characteristics for CY74FCT16952T

Parameter	Description	Test Conditions	Min.	Typ. ^[10]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-3 mA	2.5	3.5		V
		V _{CC} =Min., I _{OH} =-15 mA	2.4	3.5		V
		V _{CC} =Min., I _{OH} =-32 mA	2.0	3.0		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162952T, CY74FCT162H952T

Parameter	Description	Test Conditions	Min.	Typ. ^[10]	Max.	Unit
I _{ODL}	Output LOW Current ^[9]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	60	115	150	mA
I _{ODH}	Output HIGH Current ^[9]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	-60	-115	-150	mA
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-24 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =24 mA		0.3	0.55	V

Capacitance^[7] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ. ^[10]	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8.0	pF

Notes:

- This parameter is guaranteed but not tested.
- Pins with bus hold are described in the Pin Description.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.



Power Supply Characteristics

Parameter	Description	Test Conditions ^[11]		Typ. ^[10]	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max.	V _{IN} ≤0.2V V _{IN} ≥V _{CC} -0.2V	5	500	μA
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V _{CC} =Max.	V _{IN} =3.4V ^[12]	0.5	1.5	mA
I _{CCD}	Dynamic Power Supply Current ^[13]	V _{CC} =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, OEAB or OEBA = GND	V _{IN} =V _{CC} or V _{IN} =GND	75	120	μA/ MHz
I _C	Total Power Supply Current ^[14]	V _{CC} =Max., f ₁ =5 MHz, f ₀ =10 MHz (CLKAB) OEAB = CEAB = GND OEBA = V _{CC} 50% Duty Cycle, Outputs Open, One Bit Toggling	V _{IN} =V _{CC} or V _{IN} =GND	0.8	1.7	mA
			V _{IN} =3.4V or V _{IN} =GND	1.3	3.2	
		V _{CC} =Max., f ₀ =10 MHz (CLKAB) f ₁ =2.5 MHz, OEAB = CEAB = GND OEBA = V _{CC} 50% Duty Cycle, Outputs Open, Sixteen Bit Toggling	V _{IN} =V _{CC} or V _{IN} =GND	3.8	6.5 ^[15]	
			V _{IN} =3.4V or V _{IN} =GND	8.3	20.0 ^[15]	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)

- D_H = Duty Cycle for TTL inputs HIGH
 N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 f₀ = Clock frequency for registered devices, otherwise zero
 f₁ = Input signal frequency
 N₁ = Number of inputs changing at f₁
 All currents are in milliamps and all frequencies are in megahertz.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.



Switching Characteristics Over the Operating Range

Parameter	Description	Conditions ^[16]	74FCT16952AT 74FCT162952AT 74FCT162H952AT		74FCT16952BT 74FCT162952BT 74FCT162H952BT		74FCT16952CT 74FCT162952CT 74FCT162H952CT		Unit	Fig. No. ^[18]
			Min. ^[17]	Max.	Min. ^[17]	Max.	Min. ^[17]	Max.		
t _{PLH} t _{PHL}	Propagation Delay CLKAB, CLKBA to B, A	C _L = 50 pF R _L = 500Ω	2.0	10.0	2.0	7.5	2.0	6.3	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time OEBA, OEAB to A, B		1.5	10.5	1.5	8.0	1.5	7.0	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time OEBA, OEAB to A, B		1.5	10.0	1.5	7.5	1.5	6.5	ns	1, 7, 8
t _{SU}	Set-Up Time, HIGH or LOW A, B to CLKAB, CLKBA		2.5	—	2.5	—	2.5	—	ns	4
t _H	Hold Time, HIGH or LOW A, B to CLKAB, CLKBA		2.0	—	1.5	—	1.5	—	ns	4
t _{SU}	Set-Up Time, HIGH or LOW CEAB, CEBA to CLKAB, CLKBA		3.0	—	3.0	—	3.0	—	ns	4
t _H	Hold Time, HIGH or LOW CEAB, CEBA to CLKAB, CLKBA		2.0	—	2.0	—	2.0	—	ns	4
t _w	Pulse Width HIGH or LOW CLKAB or CLKBA ^[19]		3.0	—	3.0	—	3.0	—	ns	5
t _{SK(O)}	Output Skew ^[20]		—	0.5	—	0.5	—	0.5	ns	—

Notes:

16. See test circuits and waveforms.

17. Minimum limits are guaranteed but not tested on Propagation Delays.

18. See "Parameter Measurement Information" in the General Information Section.

19. This parameter is guaranteed but not tested.

20. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.



Ordering Information CY74FCT16952

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.3	CY74FCT16952CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16952CTPVC	O56	56-Lead (300-Mil) SSOP	
7.5	CY74FCT16952BTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16952BTPVC	O56	56-Lead (300-Mil) SSOP	
10.0	CY74FCT16952ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16952ATPVC	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162952

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6.3	CY74FCT162952CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162952CTPVC	O56	56-Lead (300-Mil) SSOP	
7.5	CY74FCT162952BTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162952BTPVC	O56	56-Lead (300-Mil) SSOP	
10.0	CY74FCT162952ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162952ATPVC	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162H952

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.3	CY74FCT162H952CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H952CTPVC	O56	56-Lead (300-Mil) SSOP	
7.5	CY74FCT162H952BTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H952BTPVC	O56	56-Lead (300-Mil) SSOP	
10.0	CY74FCT162H952ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H952ATPVC	O56	56-Lead (300-Mil) SSOP	

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