April 1994
Edition 2.0

FUJITSU

DATA SHEET

MB82208-20/-25
CMOS 4M-BIT HIGH SPEED SRAM

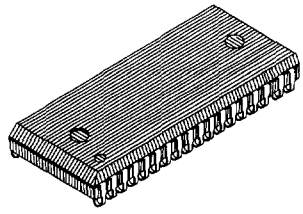
524,288-WORD x 8-BIT HIGH SPEED STATIC RANDOM ACCESS MEMORY

The Fujitsu MB82208 is 524,288-word x 8-bit high speed static random access memory fabricated with CMOS technology.
To obtain smaller chip size, cells consists of NMOS transistors and resistors. MB82208 has 400mil plastic SOJ as package option. All pins are TTL compatible and a single +5volt power supply is required.

The MB82208 is ideally suited for use in large computer and other applications where fast access time, large capacity and ease of use are required. All devices offer the advantages of low power dissipation, low cost, and high performance.

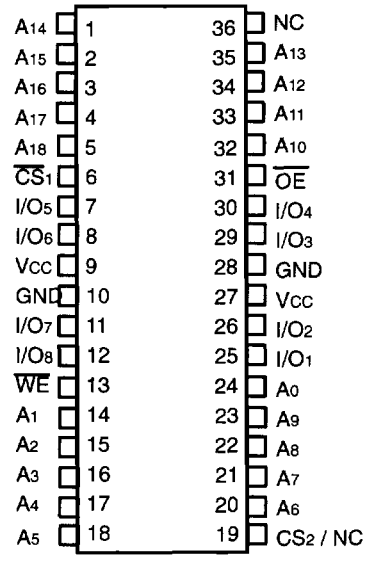
- Organization: 524,288 words x 8 bits
- Static operation: no clocks or timing strobe required
- Fast access time: tAA=tACS = 20ns max. (MB82208-20)
  tAA=tACS = 25ns max. (MB82208-25)
- Low power consumption: 825 mW max. (TTL Standby)
  27.5mW max. (CMOS Standby)
- Single +5V supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- All inputs and outputs have protection against static charge
- Standard 36-pin 400mil SOJ package (Suffix: PJ)

PRELIMINARY



PLASTIC PACKAGE
(LCC–36P–M01)

PIN ASSIGNMENT
(TOP VIEW)



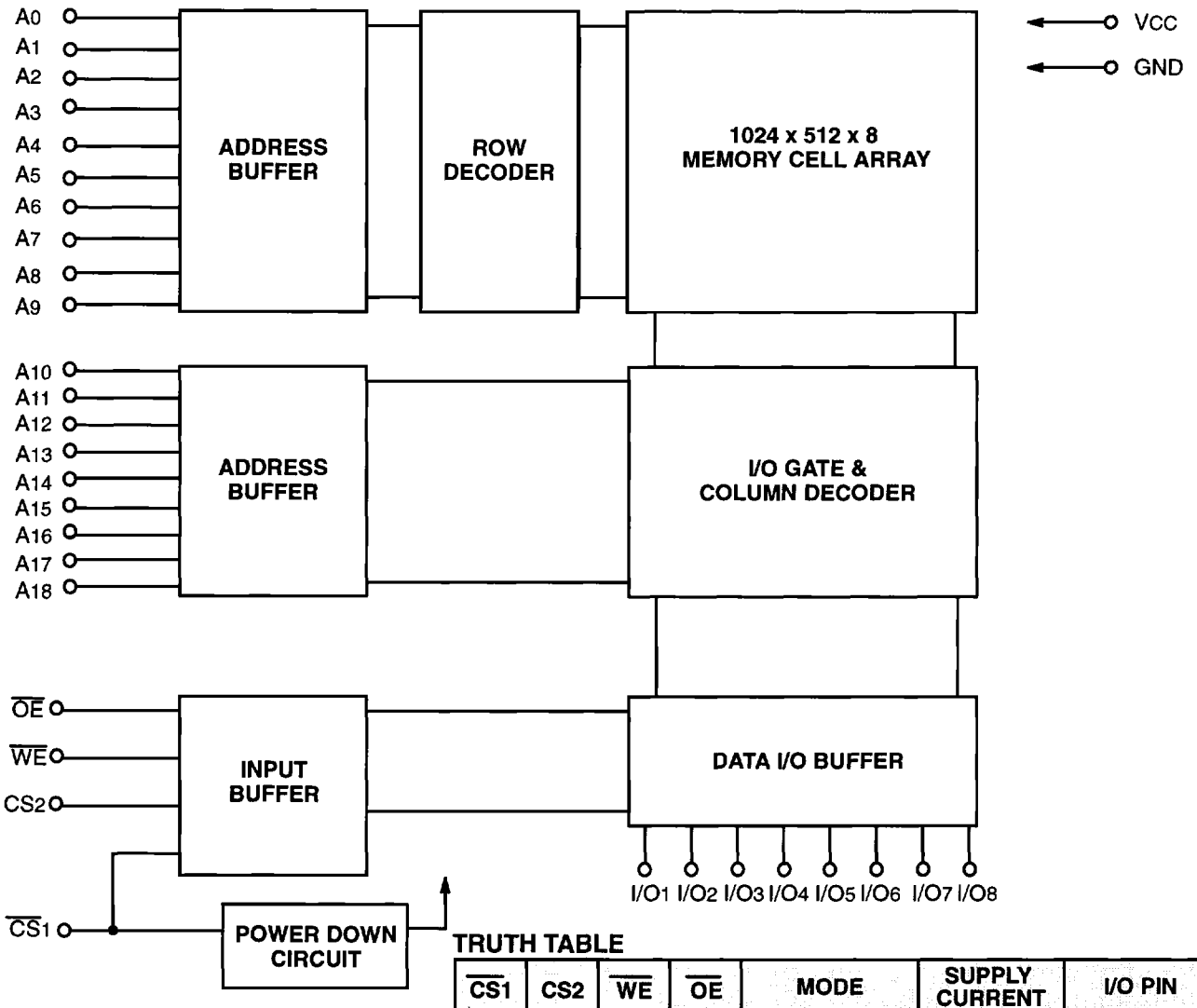
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Value	Unit
Supply Voltage	VCC	–0.5 to +7.0	V
Input Voltage on any pin with respect to GND	VIN	–0.5 to VCC+0.5	V
Output Voltage on any I/O pin with respect to GND	VOUT	–0.5 to VCC+0.5	V
Output Current	IOUT	±20	mA
Power Dissipation	PD	1.0	W
Temperature Under Bias	TBIAS	–10 to +85	°C
Storage Temperature Range	TSTG	–40 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 — MB82208 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	X	STANDBY	ISB	HIGH-Z
L	L	X	X	STANDBY	ICC	HIGH-Z
L	H	H	H	DOUT DISABLE	ICC	HIGH-Z
L	H	H	L	READ	ICC	DOUT
L	H	L	X	WRITE	ICC	DIN

CAPACITANCE (T_A= 25° C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Capacitance, A0 – A18 (V1 = 0V)	C1			6	pF
Capacitance, other pins (V2 = 0V)	C2			10	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Ambient Temperature	TA	0		70	°C

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

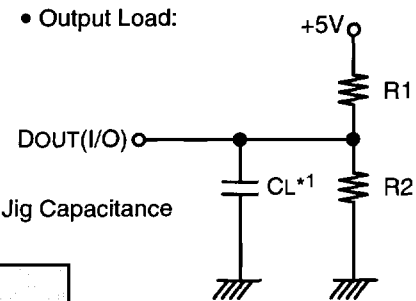
Parameter	Symbol	Test Conditions	Min	Max	Unit
Standby Supply Current	ISB1	$\overline{CS1} \geq VCC - 0.2V$, $VIN \geq VCC - 0.2V$ or $VIN \leq 0.2V$		5	mA
	ISB2	VCC= min.to max, $\overline{CS1}$ = VIH, tCyc = min.		25	mA
Operating SupplyCurrent	ICC1	IOUT = 0mA, $\overline{CS1}$ = VIL tCyc = min. VIN = VIL or VIH		150	mA
Input Leakage Current	ILI	VIN = 0V to VCC, VCC = Max.	–10	10	µA
Output Leakage Current	ILO	$\overline{CS1}$ = VIH, VOUT = 0V to VCC, VCC = max.	–10	10	µA
Input Low Voltage	VIL		–0.5*1	0.8	V
Input High Voltage	VIH		2.2	VCC +0.3	V
Output High Voltage	VOH	IOH = –4mA	2.4		V
Output Low Voltage	VOL	IOL = 8mA		0.4	V

Note: *1 –2.0V Min. for pulse width less than 10ns. (VIL min.=–0.5V at DC level)

Fig. 2 – AC TEST CONDITIONS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Times: 2ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input :VIL=0.8V, VIH=2.2V
  Output :VOL=0.8V, VOH=2.2V

- Output Load:



*1 Including Scope and Jig Capacitance

	R1	R2	CL	Parameters Measured
Load I	480Ω	255Ω	30pF	except tCLZ, tCHZ, tWLZ, tWHZ, tOLZ and tOHZ
Load II	480Ω	255Ω	5pF	tCLZ, tCHZ, tWLZ, tWHZ, tOLZ and tOHZ

AC CHARACTERISTICS

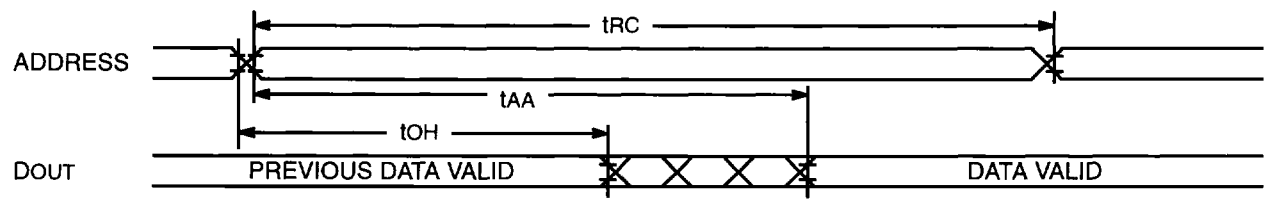
(Recommended operating conditions unless otherwise noted.)

READ CYCLE

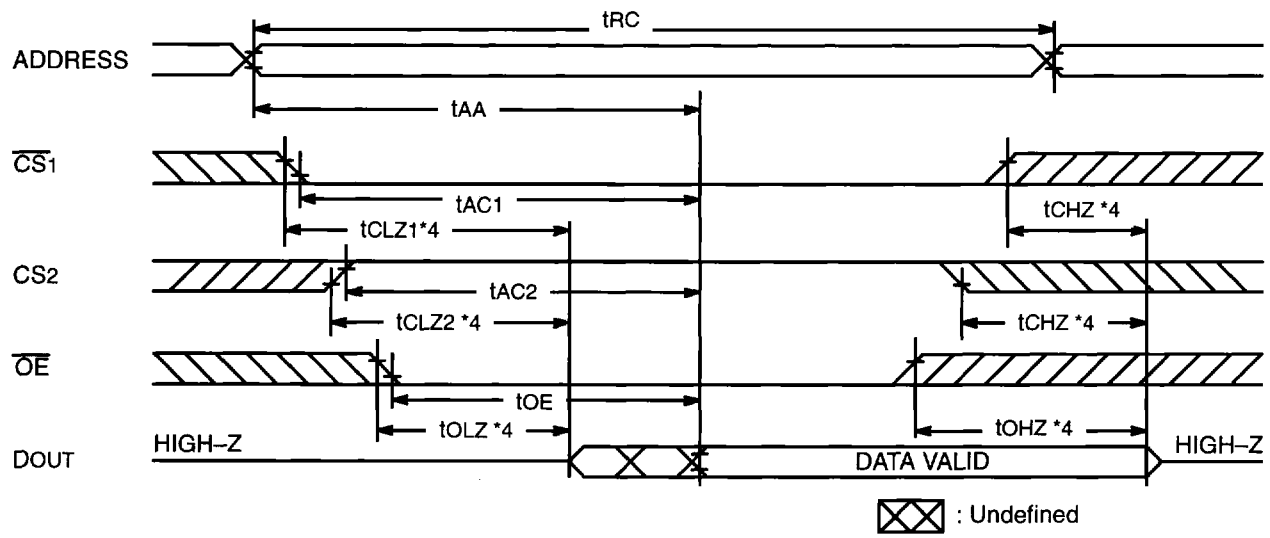
Parameter	Symbol	MB82208-20		MB82208-25		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	20		25		ns
Address Access Time *2	tAA		20		25	ns
$\overline{CS1}$ Access Time *3	tAC1		20		25	ns
CS2 Access Time *3	tAC2		10		12	ns
Output Enable to Output Valid	tOE		10		12	ns
Output Hold from Address Change	tOH	5		5		ns
$\overline{CS1}$ to OutputLow–Z *4	tCLZ1	5		5		ns
CS2 to OutputLow–Z *4	tCLZ2	2		2		ns
Output Enable to Output Low–Z *4	tOLZ	2		2		ns
Chip Select to Output High–Z *4	tCHZ	0	10	0	12	ns
Output Enable to Output High–Z *4	tOHZ	0	10	0	12	ns

READ CYCLE TIMING DIAGRAM *1

READ CYCLE 1: ADDRESS CONTROLLED *2



READ CYCLE 2: $\overline{CS1}$, CS2 CONTROLLED *3



Notes: *1 $\overline{WE}$ is high for Read Cycle.
*2 Device is continuously selected, $\overline{CS1}$ = $\overline{OE}$ = VIL, CS2 = VIH.
*3 Address valid prior to or coincident with $\overline{CS1}$ transition low, CS2 transition high.
*4 Transition is measured at the point of ±500mV from steady state voltage with load II as specified in Fig. 2.

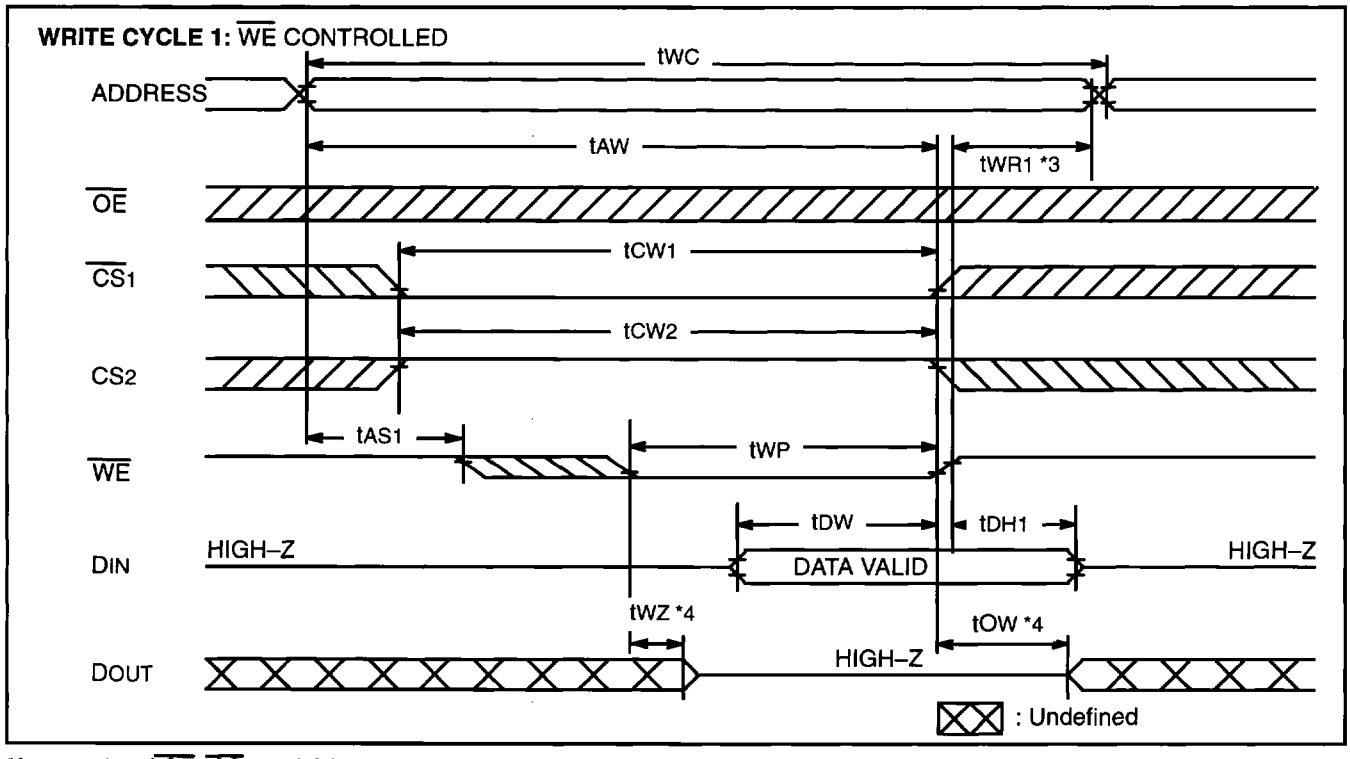
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

WRITE CYCLE *1 *2

Parameter	Symbol	MB82208-20		MB82208-25		Unit
		Min	Max	Min	Max	
Write Cycle Time	tWC	20		25		ns
Address Valid to End of Write	tAW	15		17		ns
$\overline{CS1}$ to End of Write	tCW1	15		17		ns
CS2 to End of Write	tCW2	10		12		ns
Data Valid to End of Write	tDW	10		12		ns
Data Hold Time	tDH1	0		0		ns
Data Hold Time for CS2	tDH2	2		2		ns
Write Pulse Width	tWP	13		15		ns
Address Setup Time 1	tAS1	0		0		ns
Address Setup Time 2	tAS2	5		5		ns
Write Recovery Time *3	tWR1	3		3		ns
Write Recovery Time for CS2	tWR2	5		5		ns
Write Enable to Output Low–Z *4	tOW	0		0		ns
Write Enable to Output High–Z *4	tWZ	0	10	0	12	ns

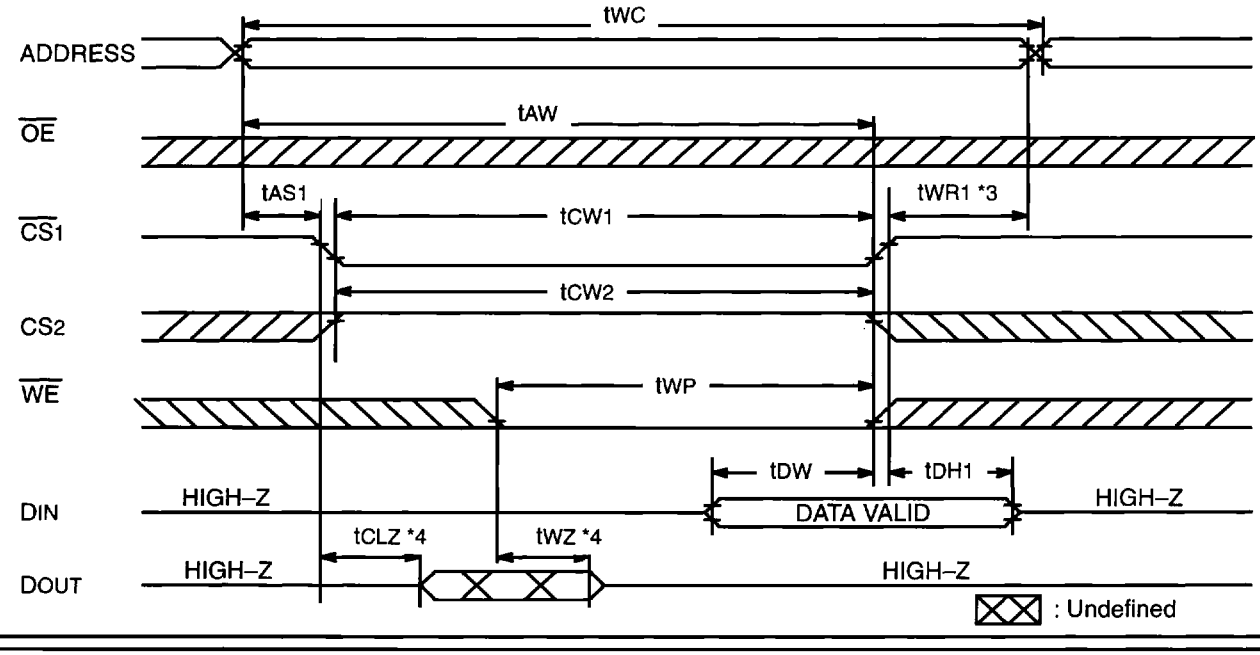
WRITE CYCLE TIMING DIAGRAM *1 *2



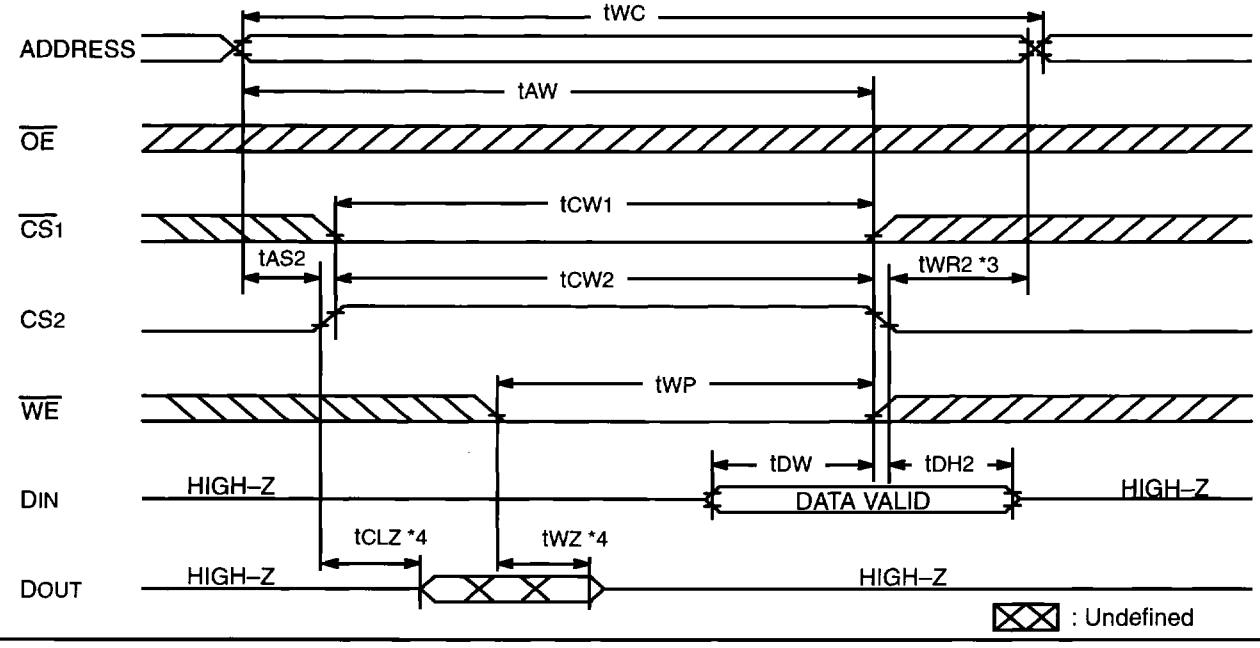
Notes: *1 If $\overline{OE}$, $\overline{CS1}$ and CS2 are in the READ Mode during this period, the I/O pins are in the output state and the input signals of opposite phase to the outputs must not be applied.
*2 If $\overline{CS1}$ goes high or CS2 goes low simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 tWR is defined from the end point of WRITE Mode.
*4 Transition is measured at the point of ±500mV from steady state voltage with Load II as specified in Fig. 2.

WRITE CYCLE TIMING DIAGRAM *1 *2

WRITE CYCLE 2: $\overline{CS1}$ CONTROLLED



WRITE CYCLE 3: CS2 CONTROLLED



Notes: *1 If $\overline{OE}$, $\overline{CS1}$ and CS2 are in the READ Mode during this period, the I/O pins are in the output state and the input signals of opposite phase to the outputs must not be applied.

*2 If CS1 goes high or CS2 goes low simultaneously with WE high, the output remains in high impedance state.

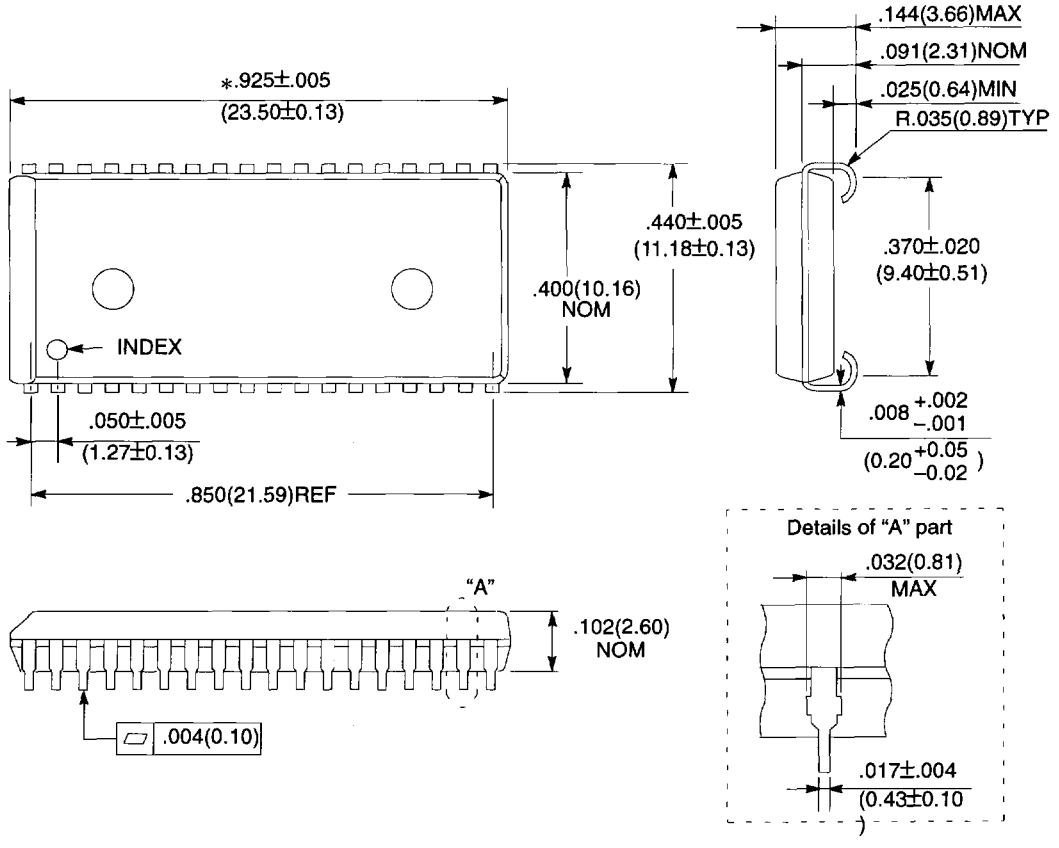
*3 tWR is defined from the end point of WRITE Mode.

*4 Transition is measured at the point of ±500mV from steady state voltage with Load II as specified in Fig. 2.

PACKAGE DIMENSIONS

PLASTIC SOJ (Suffix: PJ)

36-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-36P-M01)



*Resin protrusion. (Each side:.006(0.15)MAX.)

Dimensions in
inches (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications. Complete information sufficient for construction purposes is not necessarily given.

The information contained in this document has been carefully checked and is believed to be reliable. However, Fujitsu assumes no responsibility for inaccuracies.

The information contained in this document does not convey any license under the copyrights, patent rights or trademarks claimed and owned by Fujitsu.

Fujitsu reserves the right to change products or specifications without notice.

No part of this publication may be copied or reproduced in any form or by any means, or transferred to any third party without prior written consent of Fujitsu.

FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Technical Communication Dept.
1015,Kamikodanaka Nakahara-ku,
Kawasaki 211, Japan
Tel: (044)754-2660
FAX: (044)754-2662

North and South America

FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804, USA.
Tel: 408 -922-9000
FAX: 408-428-0640

Europe

FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10,
63303 Dreieich-Buchschlag,
Germany
Tel: (06103) 690-0,
Telex: 411963 fmg d
FAX: (06103) 690-122

Asia

FUJITSU MICROELECTRONICS ASIA PTE LIMITED
#06-04 to #06-07
Plaza By The Park
No.51 Bras Basah Road
Singapore 0719
Tel: 336-1600
Telex: 55573
FAX: 336-1609

Printed in Japan JV0063-944J2