National Semiconductor

MICROCIRCUIT DATA SHEET

MN54AC273-X REV 1C1

Original Creation Date: 07/01/96
Last Update Date: 03/18/02
Last Major Revision Date: 07/01/96

Octal D Flip-Flop

General Description

The AC273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flops' Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Industry Part Number

54AC273

NS Part Numbers

54AC273DMQB
54AC273FMQB
54AC273LMQB
54AC273WG-QML

Prime Die

Z273

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883 5005

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Ideal Buffer for MOS Microprocessor or Memory
- Eight edge-triggered D-flip-flops
- Buffered common clock
- Buffered, Asynchronous Master Reset

Standard Military Drawing (SMD)

54AC273DMQB	5962-8775601RA
54AC273FMQB	5962-8775601SA
54AC273LMQB	5962-87756012A
54AC273WG-QML	5962-8775601ZA

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage (Vcc)	-0.5V to +7.0V
DC Input Diode Current (Iik)	
Vi = -0.5V	-20 mA
Vi = Vcc +0.5V	+20 mA
DC Input Voltage (Vi)	-0.5V to Vcc +0.5V
DC Output Diode Current (Iok)	
Vo = -0.5V	-20 mA
Vo = Vcc +0.5V	+20 mA
DC Output Voltage (Vo)	-0.5V to Vcc +0.5V
DC Output Source or Sink Current (Io)	±50 mA
DC Vcc or Ground Current per Output Pin (Icc or Ignd)	±50 mA
Storage Temperature (Tstg)	-65 C to +150 C
Junction Temperature (Tj)	
CDIP	175 C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met. without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT TM circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (Vcc)	2.0V to 6.0V
Input Voltage (Vi)	0V to Vcc
Output Voltage (Vo)	0V to Vcc
Operating Temperature (Ta)	-55 C to +125 C
Minimum Input Edge Rate (Delta V/Delta t)	
AC Devices	
Vin from 30% to 70% of Vcc	
Vcc @ 3.0V, 4.5V, 5.5V	125 mV/ns

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: VCC 3.0V to 5.5V, Temp. Range: -55C to 125C. NOTE: -55C TEMPERATURE, SUBGROUP 3 IS GUARANTEED BUT NOT TESTED.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IIH	High Level Input Current	VCC=5.5V, VM=5.5V	1, 2	INPUTS		0.1	uA	1
			1, 2	INPUTS		1.0	uA	2, 3
IIL	Low Level Input Current	VCC=5.5V, VM=0.0V	1, 2	INPUTS		-0.1	uA	1
			1, 2	INPUTS		-1.0	uA	2, 3
VOL	Low Level Output Voltage	VCC=3.0V, VINH=3.0V, VIL=0.9V, IOL=50.0uA	1, 2	OUTPUTS		.10	V	1, 2, 3
		VCC=4.5V, VINH=4.5V, VIL=1.35V, IOL=50.0uA	1, 2	OUTPUTS		.10	V	1, 2, 3
		VCC=5.5V, VINH=5.5V, VIL=1.65V, IOL=50.0uA	1, 2	OUTPUTS		.10	V	1, 2, 3
		VCC=3.0V, VINH=3.0V, VIL=0.9V, IOL=12.0mA	1, 2	OUTPUTS		.36	V	1
			1, 2	OUTPUTS		.50	V	2, 3
		VCC=4.5V, VINH=4.5V, VIL=1.35V, IOL=24.0mA	1, 2	OUTPUTS		.36	V	1
			1, 2	OUTPUTS		.50	V	2, 3
		VCC=5.5V, VINH=5.5V, VIL=1.65V, IOL=24.0mA	1, 2	OUTPUTS		.36	V	1
			1, 2	OUTPUTS		.50	V	2, 3
VIOL	Dynamic Output Current LOW	VCC=5.5V, VINL=0.0V, VIH=3.85, VIL=1.65V, IOL=50.0mA	1, 2, 5	OUTPUTS		1.65	V	1, 2, 3
VOH	High Level Output Voltage	VCC=3.0V, VIH=2.1V, VINL=0.0V, VIOH=-50.0uA	1, 2	OUTPUTS	2.90		V	1, 2, 3
		VCC=4.5V, VIH=3.15V, VINL=0.0V, IOH=-50.0uA	1, 2	OUTPUTS	4.40		V	1, 2, 3
		VCC=5.5V, VIH=3.85V, VINL=0.0V, IOH=-50.0uA	1, 2	OUTPUTS	5.40		V	1, 2, 3
		VCC=3.0V, VIH=2.1V, IOH=-12.0mA	1, 2	OUTPUTS	2.56		V	1
			1, 2	OUTPUTS	2.40		V	2, 3
		VCC=4.5V, VIH=3.15V, IOH=-24.0mA	1, 2	OUTPUTS	3.86		V	1
			1, 2	OUTPUTS	3.70		V	2, 3
		VCC=5.5V, VIH=3.85V, IOH=-24.0mA	1, 2	OUTPUTS	4.86		V	1
			1, 2	OUTPUTS	4.70		V	2, 3
VIOH	Dynamic Output Current HIGH	VCC=5.5V, VIH=3.85V, VINH=5.5V, IOH=-50.0mA	1, 2, 5	OUTPUTS	3.85		V	1, 2, 3
ICCH	Supply Current Outputs HIGH	VCC=5.5V, VINH=5.5V, VINL=0.0V	1, 2	VCC		4.0	uA	1
			1, 2	VCC		80	uA	2, 3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: VCC 3.0V to 5.5V, Temp. Range: -55C to 125C. NOTE: -55C TEMPERATURE, SUBGROUP 3 IS GUARANTEED BUT NOT TESTED.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
ICCL	Supply Current Outputs LOW	VCC=5.5V, VINL=0.0V	1, 2	VCC		4.0	uA	1
			1, 2	VCC		80	UA	2, 3

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: CL=50pf, RL=500 OHMS, TR=3.0ns, TF=3.0ns, Temp Range: -55C to 125C. NOTE: -55C TEMPERATURE, SUBGROUP 11 IS GUARANTEED BUT NOT TESTED.

tpLH(1)	Propagation Delay	VCC=4.5V	3, 4, 7	CP to Qn	1.5	9.0	ns	9
			3, 4, 7	CP to Qn	1.5	11.0	ns	10, 11
tpHL(1)	Propagation Delay	VCC=4.5V	3, 4, 7	CP to Qn	1.5	10.0	ns	9
			3, 4, 7	CP to Qn	1.5	11.5	ns	10, 11
tpHL (2)	Propagation Delay	VCC=4.5V	3, 4, 7	$\overline{MR}$ to Qn	1.5	10.0	ns	9
			3, 4, 7	$\overline{MR}$ to Qn	1.5	11.5	ns	10, 11
ts(H/L)(1)	Setup Time HIGH or LOW	VCC=4.5V	6	Dn to CP	4.0		ns	9
			6	Dn to CP	5.0		ns	10, 11
th(H/L)(1)	Hold Time HIGH or LOW	VCC=4.5V	6	Dn to CP	1.0		ns	9, 10, 11
tw(H/L)(1)	CP Pulse Width HIGH or LOW	VCC=4.5V	6	Clock Pulse Width	5.0		ns	9, 10, 11
tw(L) (2)	$\overline{MR}$ Pulse Width LOW	VCC=4.5V	6	$\overline{MR}$	5.0		ns	9
tw(L) (2)	$\overline{MR}$ Pulse Width LOW	VCC=4.5V	6	$\overline{MR}$	6.5		ns	10, 11
trec (1)	Recovery Time	VCC=4.5V	6	$\overline{MR}$ to CP	3.5		ns	9
			6	$\overline{MR}$ to CP	4.0		ns	10, 11
FMAX(1)	Maximum Clock Frequency	VCC=4.5V	6		95		MHZ	9
			6		90		MHZ	10, 11

Electrical Characteristics

AC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: CL=50pf, RL=500 OHMS, TR=3.0ns, TF=3.0ns, Temp Range: -55C to 125C. NOTE: -55C TEMPERATURE, SUBGROUP 11 IS GUARANTEED BUT NOT TESTED.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tpLH(3)	Propagation Delay	VCC=3.0V	3, 4	CP to Qn	1.0	12.5	ns	9
			3, 4	CP to Qn	1.0	15.0	ns	10, 11
tpHL(3)	Propagation Delay	VCC=3.0V	3, 4	CP to Qn	1.0	13.0	ns	9
			3, 4	CP to Qn	1.0	16.0	ns	10, 11
tpHL(4)	Propagation Delay	VCC=3.0V	3, 4	$\overline{MR}$ to Qn	1.0	13.0	ns	9
			3, 4	$\overline{MR}$ to Qn	1.0	16.0	ns	10, 11
ts(H/L)(2)	Setup Time HIGH or LOW	VCC=3.0V	6	Dn to CP	6.5		ns	9
			6	Dn to CP	8.0		ns	10, 11
th(H/L)(2)	Hold Time HIGH or LOW	VCC=3.0V	6	Dn to CP	0.0		ns	9, 10, 11
tw(H/L)(3)	CP Pulse Width HIGH or LOW	VCC=3.0V	6	Clock Pulse Width	5.5		ns	9
			6	Clock Pulse Width	6.5		ns	10, 11
tw(L) (4)	$\overline{MR}$ Pulse Width LOW	VCC=3.0V	6	$\overline{MR}$	8.0		ns	9
tw(L) (4)	$\overline{MR}$ Pulse Width LOW	VCC=3.0V	6	$\overline{MR}$	10.0		ns	10, 11
trec (2)	Recovery Time	VCC=3.0V	6	$\overline{MR}$ to CP	5.0		ns	9
			6	$\overline{MR}$ to CP	6.0		ns	10, 11
FMAX(2)	Maximum Clock Frequency	VCC=3.0V	6		90		MHZ	9
			6		75		MHZ	10, 11

Note 1: SCREEN TESTED 100% ON EACH DEVICE AT +25C & +125C TEMPERATURE, SUBGROUPS 1, 2, 7, & 8.
Note 2: SAMPLE TESTED (METHOD 5005, TABLE 1) ON EACH MFG. LOT AT +25C & +125C TEMPERATURE, SUBGROUPS A1, 2, 7, & 8.
Note 3: SCREEN TESTED 100% ON EACH DEVICE AT +25C TEMPERATURE ONLY SUBGROUP A9.
Note 4: SAMPLE TESTED (METHOD 5005, TABLE 1) ON EACH MFG. LOT AT +25C & +125C TEMPERATURE, SUBGROUPS A9 & 10.
Note 5: TRANSMISSION LINE DRIVING TEST, GUARDBAND LIMITS SET FOR +25C, 2 MSEC DURATION MAX.
Note 6: GUARANTEED BUT NOT TESTED. (DESIGN CHARACTERIZATION DATA)

(Continued)

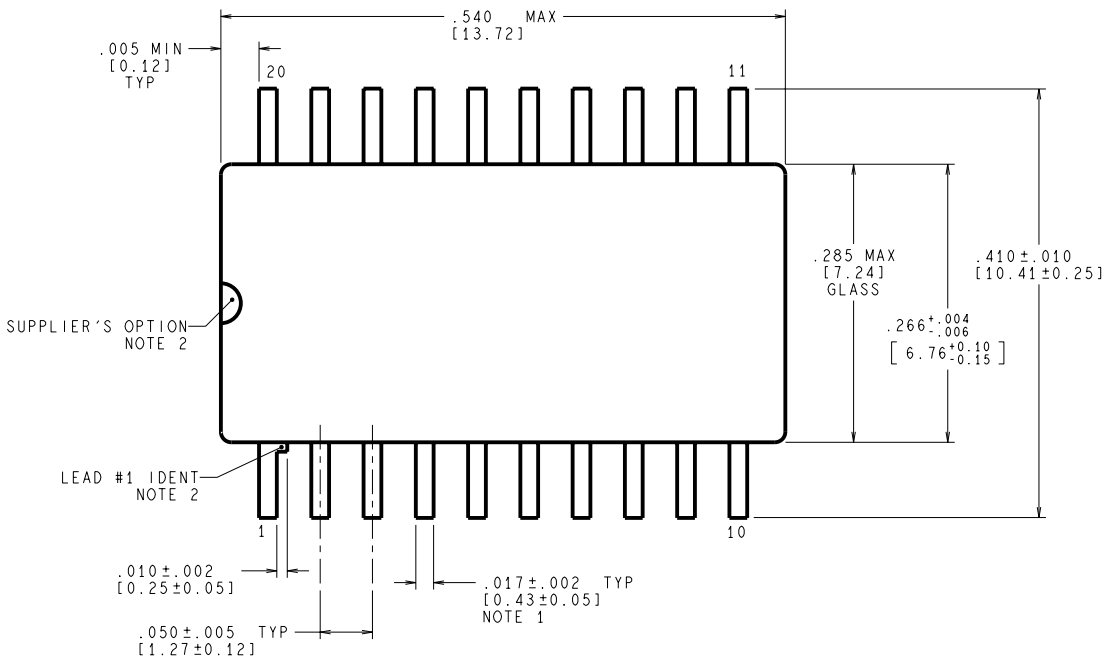
Note 7: +25C & +125C MIN LIMITS GUARANTEED FOR 5.5V BY GUARDBANDING 4.5V MIN. LIMITS.

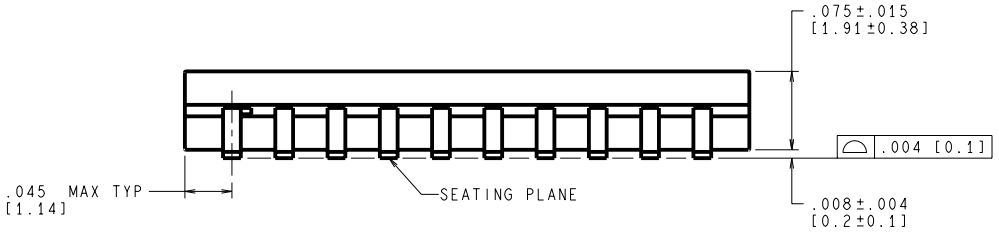
Graphics and Diagrams

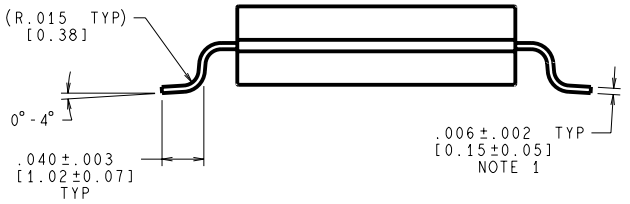
GRAPHICS#	DESCRIPTION
WG20ARB	CERPACK, 20 LEAD GULL WING (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11842	10/13/1997	TL/KH
B	DIM .410 WAS .391; UPDATE NOTE 3.	12013	06/15/1998	MS/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF JUNE 1998.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN T LEQUANG	10/13/1997
DFTG. CHK.	
ENGR. CHK.	

PROJECTION INCH [MM]

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK,
20 LEAD,
GULL WING

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG20A	B

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
1C1	M0003971	03/18/02	Rose Malone	Update MDS: MN54AC273-X, Rev. 1B0 to MN54AC273-X, Rev. 1C1. Added SMD Numbers and WG pkg to Main Table and Features Section, also added WG Mkt Dwg to Graphics Section.