

bq4011H/bq4011HY

High-Speed 32Kx8 Nonvolatile SRAM

Features

- ➤ Access/cycle times of 20 and 25 ns
- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- ➤ Industry-standard 28-pin 32K x 8 pinout
- ➤ Conventional SRAM operation; unlimited write cycles
- ➤ 10-year minimum data retention in absence of power
- ➤ Battery internally isolated until power is applied

General Description

The CMOS bq4011H is a nonvolatile 262,144-bit fast static RAM organized as 32,768 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM. Access times as fast as 20 ns are available.

The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When $V_{\rm CC}$ falls out of tolerance, the SRAM is unconditionally write-protected to prevent inadvertent write operation.

At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The bq4011H uses an extremely low standby current CMOS SRAM, coupled with a small lithium coin cell to provide nonvolatility without long write cycle times and the write cycle limitations associated with EEPROM.

The bq4011H requires no external circuitry and is socket-compatible with industry-standard SRAMs.

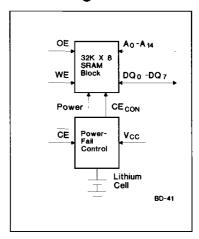
Pin Connections

A ₁₄	28
A₄□ 6	23 🗆 A ₁₁
A3 0 7	22 DE
A ₂ = 8	21 A ₁₀
A, E 9	20 ☐ CE
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A ₀ 4 10	19 🗎 DQ7
DQ 0 🗆 11	18 🗎 DQ e
DQ 1 12	17 🗅 DQ ₅
DQ 2 [13	16 🗆 DQ 4
V _{SS} 14	15 🗆 DQ ₃
	PN-7

Pin Names

A ₀ -A ₁₄	Address inputs
DQ0-DQ7	Data input/output
CE	Chip enable input
ŌĒ	Output enable input
$\overline{\text{WE}}$	Write enable input
V_{CC}	+5 volt supply input
V_{SS}	Ground

Block Diagram



Selection Guide

Part Number	Minimum Access Time (ns)	Negative Supply Tolerance	Part Number	Minimum Access Time (ns)	Negative Supply Tolerance
bq4011H -20	20	-5%	bq4011HY -20	20	-10%
bq4011H -25	25	-5%	bq4011HY -25	25	-10%

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