

KM23C8001B(G)**CMOS MASK ROM****8M-Bit (1M × 8) CMOS MASK ROM****FEATURES**

- 1,048,576 × 8 bit organization
- Fast access time: 100ns (max.)
- Supply voltage: single +5V
- Current consumption
Operating: 60 mA(max.)
- Fully static operation
- All inputs and outputs TTL compatible
- Three state outputs
- Polarity programmable
output enable pin
- Package: 32-pin, 600 mil, plastic DIP
(JEDEC standard)
32-pin, 525 mil, plastic SOP

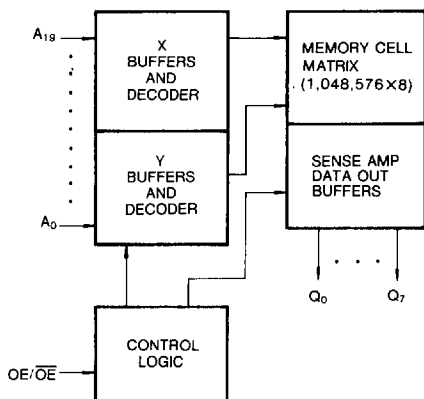
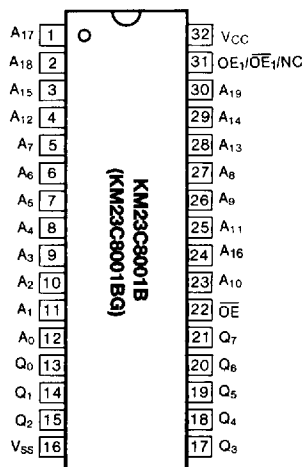
GENERAL DESCRIPTION

The KM23C8001B is a fully static mask programmable ROM organized 1,048,576×8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of micro-processor, and data memory, character generator.

The KM23C8001B is packaged in a 32-DIP and the KM23V8001BG in a 32-SOP, provides polarity programmable OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM**PIN CONFIGURATION**

Pin Name	Pin Function
A ₀ -A ₁₉	Address Inputs
Q ₀ -Q ₇	Data Outputs
OE/OE*	Output Enable
V _{CC}	Power (+5V)
V _{SS}	Ground
NC	No Connection

* User Selectable Polarity

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CMOS MASK ROM

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V _{SS}	V _{IN}	-0.3 to +7.0	V
Temperature Under Bias	T _{bias}	-10 to + 85	°C
Storage Temperature	T _{stg}	-55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Supply Voltage	V _{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I _{CC}	$\overline{OE} = V_{IL}$, f = 6.7MHz all output open	—	60	mA
Input Leakage Current	I _{LI}	V _{IN} = 0 to V _{CC}	—	10	μA
Output Leakage Current	I _{LO}	V _{OUT} = 0 to V _{CC}	—	10	μA
Input High Voltage, All Inputs	V _{IH}		2.2	V _{CC} + 0.3	V
Input Low Voltage, All Inputs	V _{IL}		-0.3	0.8	V
Output High Voltage Level	V _{OH}	I _{OH} = -400μA	2.4	—	V
Output Low Voltage Level	V _{OL}	I _{OL} = 2.1mA	—	0.4	V

CAPACITANCE (T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C _{OUT}	V _{OUT} = 0V	—	12	pF
Input Capacitance	C _{IN}	V _{IN} = 0V	—	12	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

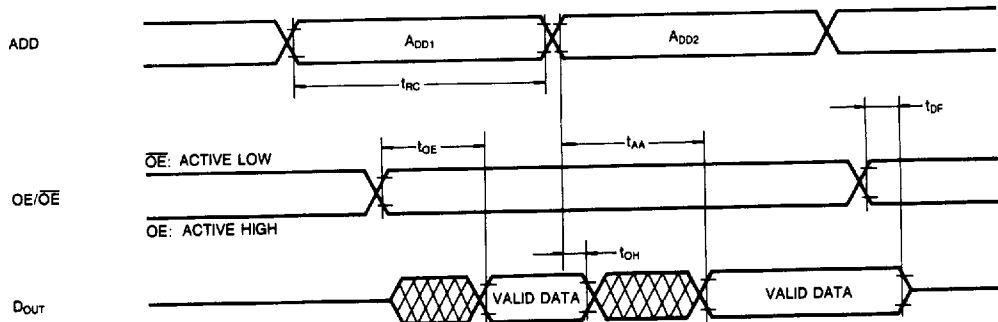
OE/ \overline{OE}	Mode	Data	Power
L/H	Operating	High-Z	Active
H/L	Operating	D _{OUT}	Active

KM23C8001B(G)**CMOS MASK ROM****AC CHARACTERISTICS** ($T_a=0^\circ$ to $+70^\circ\text{C}$, $V_{CC}=5V \pm 10\%$, unless otherwise noted.)**TEST CONDITIONS**

Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100\text{pF}$

READ CYCLE

Parameter	Symbol	KM23C8001B(G)-10		KM23C8001B(G)-12		KM23C8001B(G)-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Address Access Time	t_{AA}		100		120		150	ns
Output Enable Access Time	t_{OE}		50		60		70	ns
Output Disable to Output High-Z	t_{DF}		20		20		30	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM**READ**

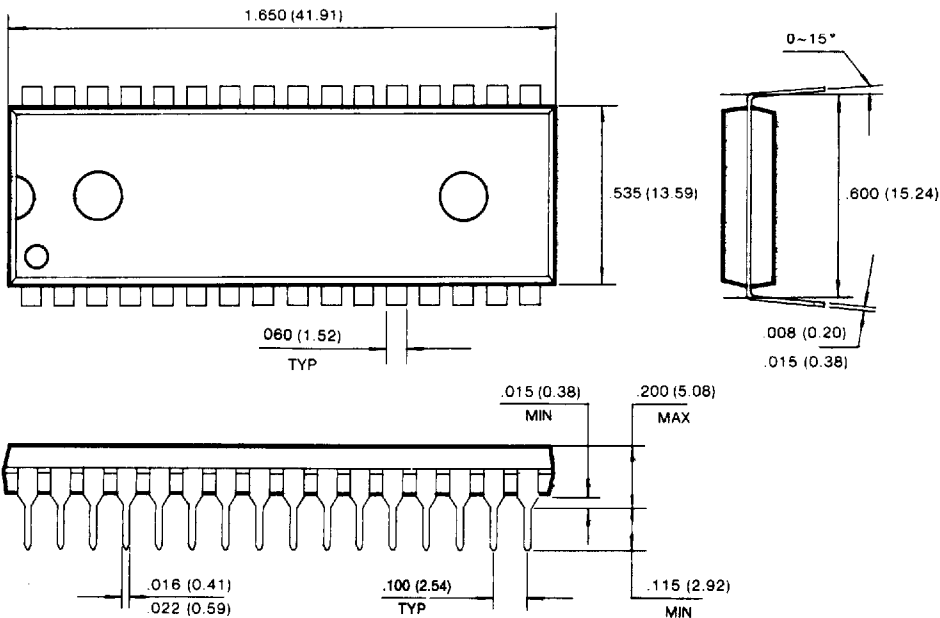
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CMOS MASK ROM

PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C8001B)

Units: Inches (millimeters)



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32 LEAD SMALL OUTLINE PACKAGE (KM23C8001BG)

