

# TC40H160P/F · TC40H162P/F TC40H161P/F · TC40H163P/F

C<sup>2</sup>MOS DIGITAL INTEGRATED CIRCUIT  
SILICON MONOLITHIC

## SYNCHRONOUS PRESETTABLE 4-BIT COUNTER

TC40H160 DECADE. ASYNCHRONOUS CLEAR.  
TC40H161 BINARY. ASYNCHRONOUS CLEAR.  
TC40H162 DECADE. SYNCHRONOUS CLEAR.  
TC40H163 BINARY. SYNCHRONOUS CLEAR.

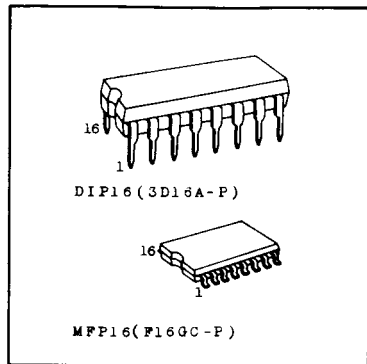
The TC40H160/161/162/163 are synchronous type presettable 4-bit counters.

The TC40H160/162 are DECADE counters.

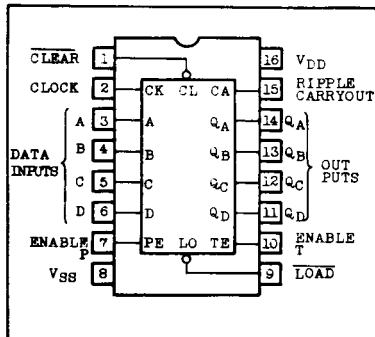
The TC40H161/163 are BINARY counters.

The CLEAR and LOAD of each counter are active at "L" level.

The CLEAR functions of the TC40H160/161 are asynchronous, but those of the TC40H162/163 synchronize with the rising edge of clock pulse.



## PIN CONNECTION



## MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V <sub>DD</sub>	V <sub>SS</sub> -0.5 ~ V <sub>SS</sub> +10	V
Input Voltage	V <sub>IN</sub>	V <sub>SS</sub> -0.5 ~ V <sub>DD</sub> +0.5	V
Output Voltage	V <sub>OUT</sub>	V <sub>SS</sub> -0.5 ~ V <sub>DD</sub> +0.5	V
Input Current	I <sub>IN</sub>	±10	mA
Power Dissipation	P <sub>D</sub>	300(DIP)/180(MFP)	mW
Storage Temperature	T <sub>stg</sub>	-65 ~ 150	°C
Lead Temp./Time	T <sub>sol</sub>	260°C · 10 sec	

## TRUTH TABLE

CLEAR	INPUTS				OUTPUTS								
	ENABLE		LOAD	CLOCK	DATA INPUTS				DATA OUTPUTS				RIPPLE CARRY OUT
PE	TE	A			B	C	D	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>		
*	*	L	*	↓	Don't Care				No change				L
*	*	H	*	↓	Don't Care				No change				Able
L	*	*	*	◇	Don't Care				All Reset				L
H	*	L	L	↑	Program Data				Program Output				L
H	*	H	L	↑	Program Data				Program Output				Able
H	*	L	H	↑	Don't Care				No count				L
H	L	H	H	↑	Don't Care				No count				Able
H	H	H	H	↑	Don't Care				Count up				Able

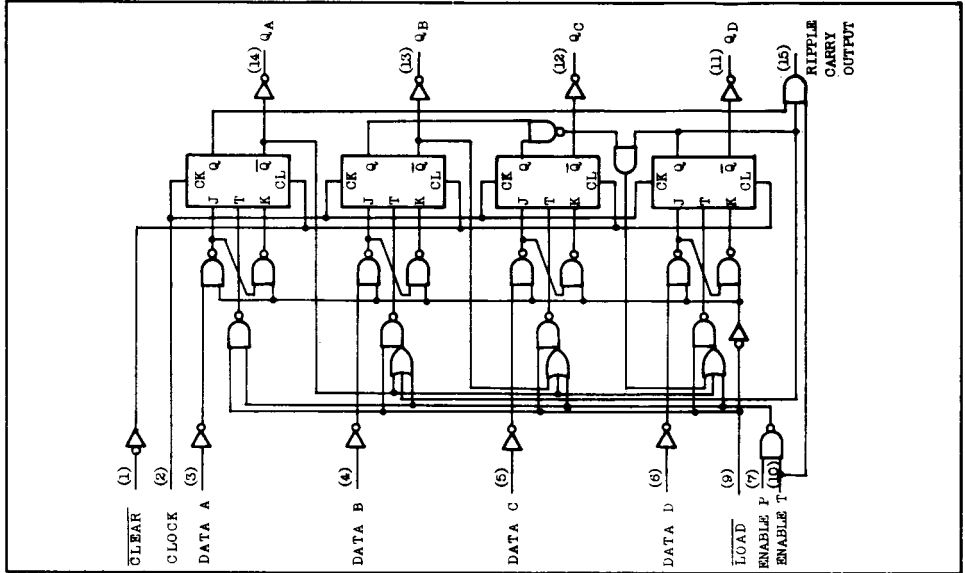
\* Don't care

◇ TC40H160/163 Don't Care

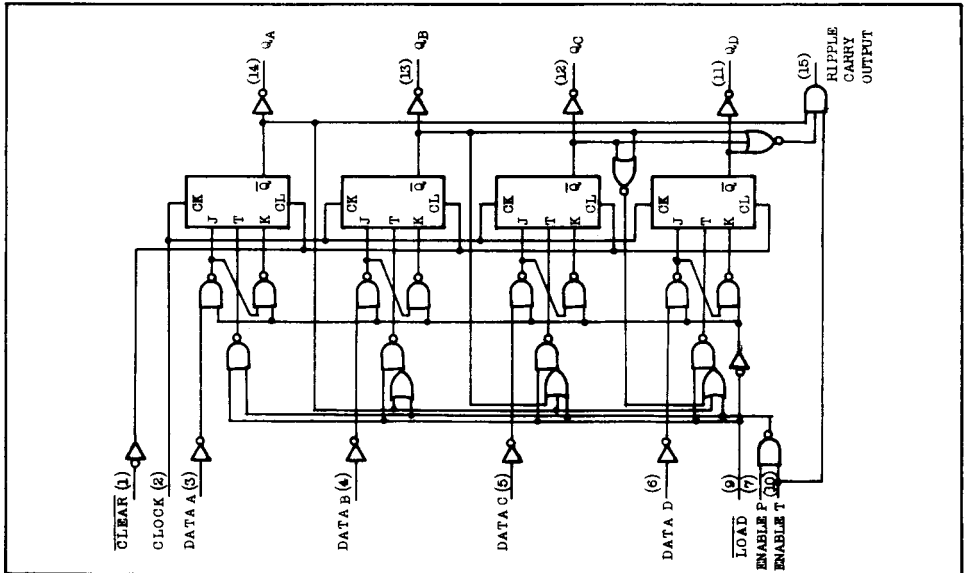
TC40H162/163 Synchronise with the rising edge of clock.

# TC40H160P/F • TC40H162P/F TC40H161P/F • TC40H163P/F

TC40H160 BLOCK DIAGRAM

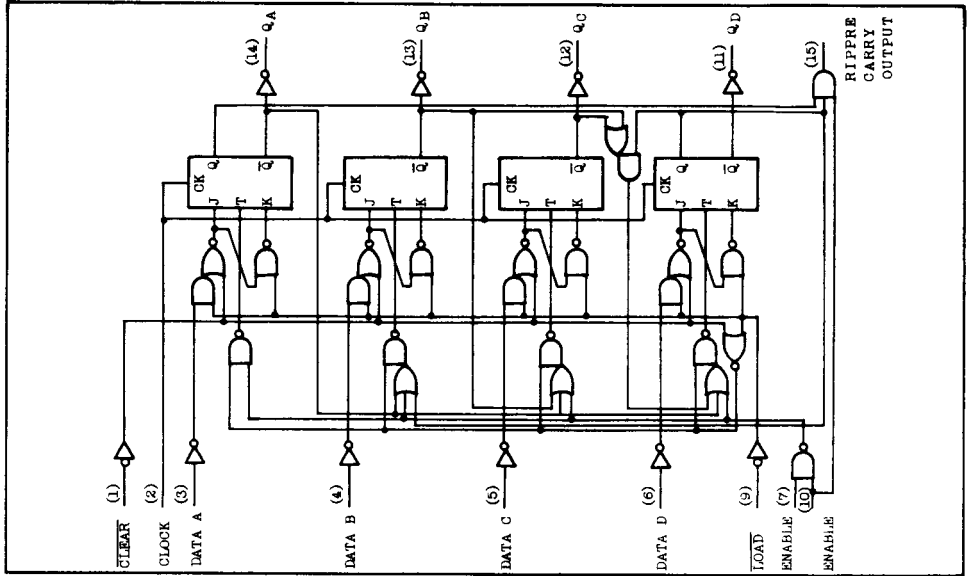


TC40H161 BLOCK DIAGRAM

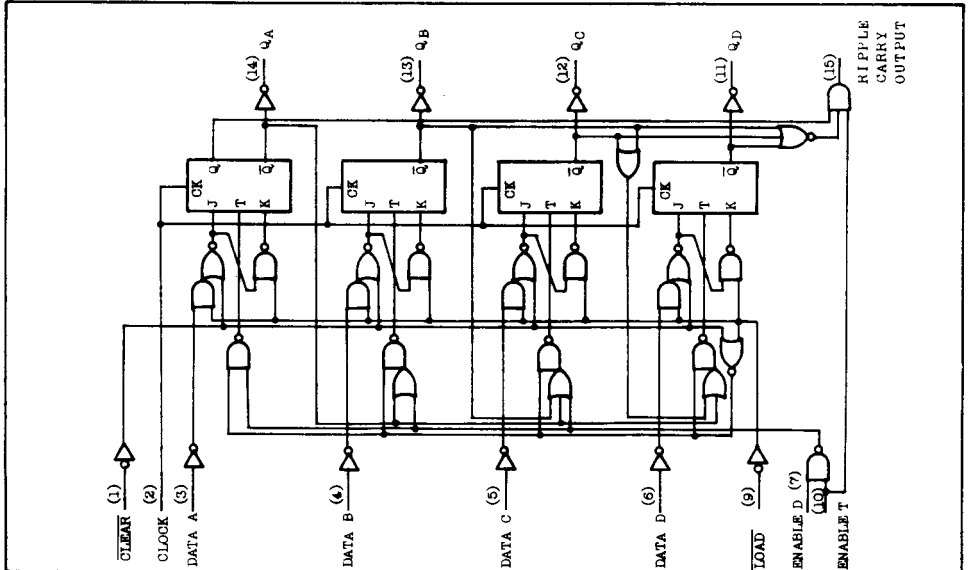


# TC40H160P/F • TC40H162P/F TC40H161P/F • TC40H163P/F

TC40H162 BLOCK DIAGRAM



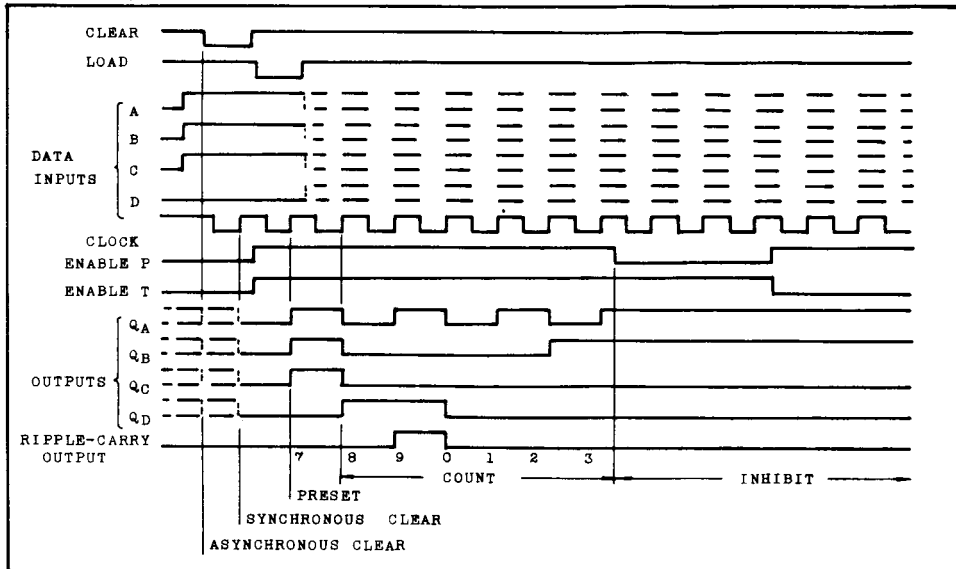
TC40H163 BLOCK DIAGRAM



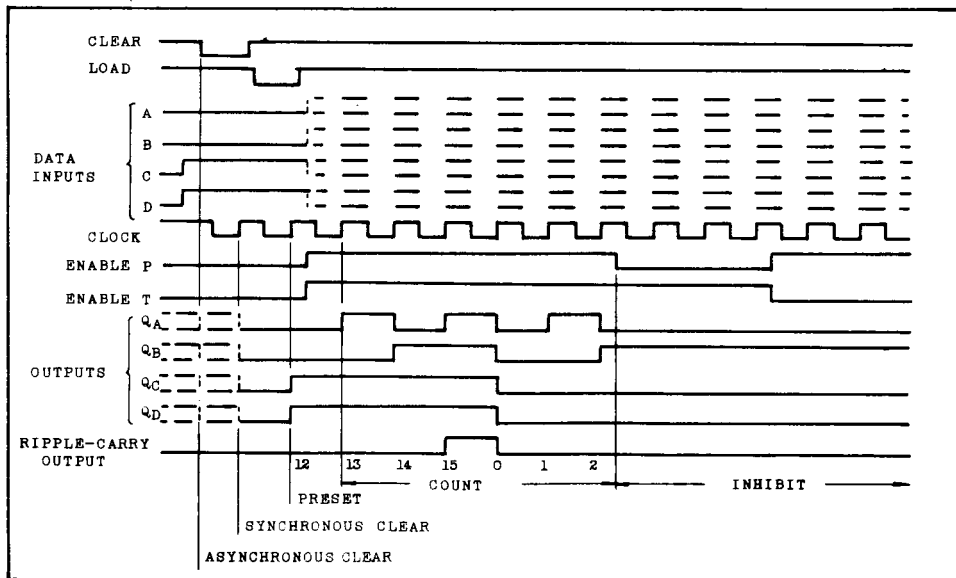
# TC40H160P/F • TC40H162P/F

## TC40H161P/F • TC40H163P/F

TC40H160/162 TIMING CHART



TC40H161/163 TIMING CHART



# TC40H160P/F • TC40H162P/F TC40H161P/F • TC40H163P/F

RECOMMENDED OPERATING CONDITIONS ( $V_{SS}=0V$ )

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	$V_{DD}$	-	2.0	-	8.0	V
Input Voltage	$V_{IN}$	-	0	-	$V_{DD}$	V
Operating Temperature	$T_{OPR}$	-	-40	-	85	°C

ELECTRICAL CHARACTERISTICS ( $V_{SS}=0.0V$ )

CHARACTERISTIC	SYMBOL	TEST CONDITION	$V_{DD}$ (B)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage	$V_{OH}$	$ I_{OUT}  < 1\mu A$ $V_{IN}=V_{SS}, V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage	$V_{OL}$	$ I_{OUT}  < 1\mu A$ $V_{IN}=V_{SS}, V_{DD}$	5	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Current	$I_{OH}$	$V_{OH}=4.6V$ $V_{IN}=V_{SS}, V_{DD}$	5	-0.52	-	-0.44	-	-	-0.36	-	mA
Low Level Output Current	$I_{OL}$	$V_{OL}=0.4V$ $V_{IN}=V_{SS}, V_{DD}$	5	1.4	-	1.1	-	-	0.8	-	mA
Input Voltage	"H" Level $V_{IH}$	$ I_{OUT}  < 1\mu A$ $V_{OUT}=0.5V$	5	4.0	-	4.0	-	-	4.0	-	V
	"L" Level $V_{IL}$		5	-	1.0	-	-	1.0	-	1.0	
Input Current	"H" Level $I_{IH}$	$V_{IH}=8.0V$	8	-	0.3	-	$10^{-5}$	0.3	-	1.0	$\mu A$
	"L" Level $I_{IL}$	$V_{IL}=0.0V$	8	-	-0.3	-	$-10^{-5}$	-0.3	-	-1.0	
Quiescent Supply Current	$I_{DD}$	$*V_{IN}=V_{SS}, V_{DD}$	5	-	12.5	-	$10^{-3}$	12.5	-	75	$\mu A$

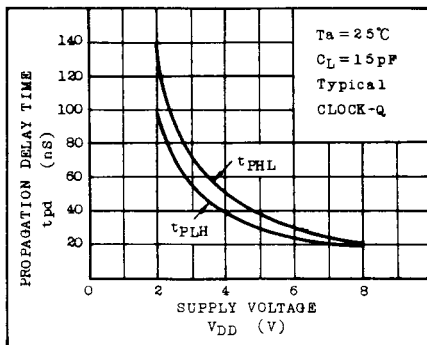
\* All valid input combinations.

SWITCHING CHARACTERISTICS ( $T_a=25^\circ C$ ,  $V_{SS}=0V$ ,  $V_{DD}=5V$ ,  $C_L=15pF$ )

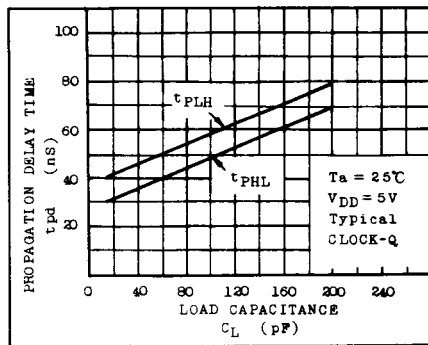
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time	$t_{OR}$		-	20	35	ns
Output Fall Time	$t_{OF}$		-	15	30	
Propagation Delay Time	(Low-High) $t_{PLH}$	CLOCK - Q	-	30	45	ns
	(High-Low) $t_{PHL}$		-	40	60	
Propagation Delay Time	(Low-High) $t_{PLH}$	CLOCK - CARRY OUTPUT	-	50	75	ns
	(High-Low) $t_{PHL}$		-	42	63	
Propagation Delay Time	(Low-High) $t_{PLH}$	ENABLE RIPPLE TE or PE - CARRY OUTPUT	-	26	39	ns
	(High-Low) $t_{PHL}$		-	34	51	
	(High-Low) $t_{PHL}$		CLEAR - Q	-	45	
Setup Time	$t_{SET-UP}$	DATA, ENABLE - CLOCK LOAD, CLEAR	-	40	60	ns
Min. Clock Clear Pulse Width	$t_W$	CLOCK, CLEAR	-	17	26	ns
Max. Clock	Rise Time $t_{r\phi}$		1.0	20	-	ns
	Fall Time $t_{f\phi}$					
Max. Clock Frequency	$f_{MAX}$		10	17	-	MHz

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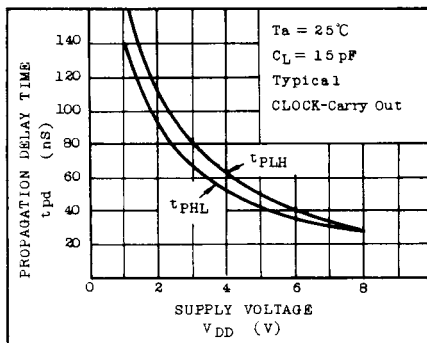
$t_{pd} - V_{DD}$



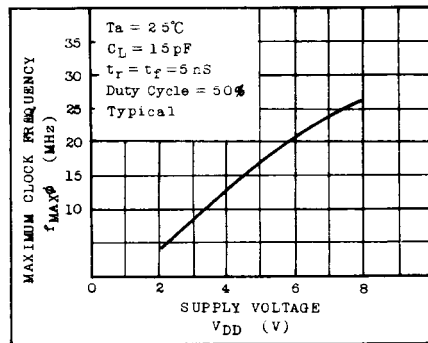
$t_{pd} - C_L$



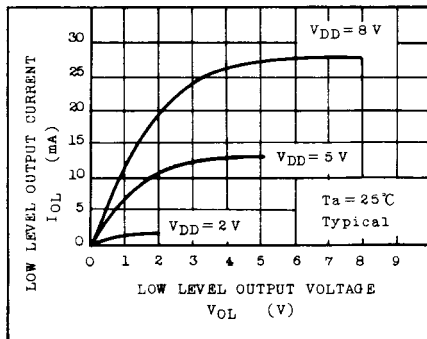
$t_{pd} - V_{DD}$



$f_{max\phi} - V_{DD}$



$I_{OL} - V_{OL}$



$I_{OH} - (V_{DD} - V_{OH})$

