TYPES SN54S226, SN74S226
4-BIT PARALLEL LATCHED BUS TRANSCEIVERS

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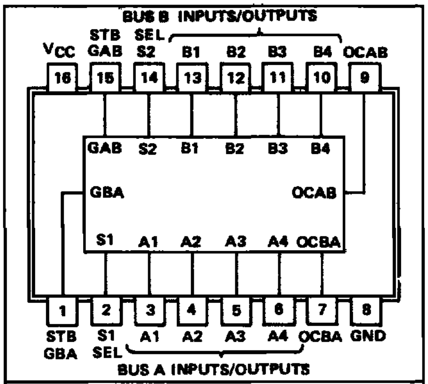
- Universal Transceivers for Implementing System Bus Controllers
- Dual-Rank 4-Bit Transparent Latches Provide
  - Exchange of Data Between 2 Buses In One Clock Pulse
  - Bus-to-Bus Isolation
  - Rapid Data Transfer
  - Full Storage Capability
- Hysteresis at Data Inputs Enhances Noise Rejection
- Separate Output Control Inputs Provide Independent Enable/Disable for Either Bus Output
- 3-State Outputs Drive Bus Lines Directly

SN54S226 . . . J PACKAGE
SN74S226 . . . J OR N PACKAGE

(TOP VIEW)



SEE FUNCTION TABLES

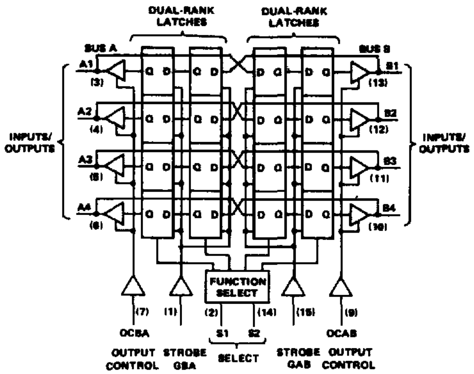
description

These high-performance Schottky TTL quadruple bus transceivers employ dual-rank bidirectional four-bit transparent latches and feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The bus-management functions implemented and the high-impedance controls offered provide the designer with a controller/transceiver that interfaces and drives system bus-organized lines directly. They are particularly attractive for implementing:

Bidirectional bus transceivers
Data-bus controllers

The bus-management functions, under control of the function-select (S1, S2) inputs, provide complete data integrity for each of the four modes described in the function table. Directional transparency provides for routing data from or to either bus, and the dual store and dual readout capabilities can be used to perform the exchange of data between the two bus lines in the equivalent of a single clock pulse. Storage of data is accomplished by selecting the latch function, setting up the data, and taking the appropriate strobe input low. As long as the strobe is held low, the data is latched for the selected function. Further control is offered through the availability of independent output controls that can be used to enable or

functional block diagram



BUS-MANAGEMENT FUNCTION TABLE

OPERATION	S2	S1	LATCH FUNCTIONS
DRIVE BUS A	L	L	Pass Bus B Data to Bus A
DRIVE BUS B	H	L	Pass Bus A Data to Bus B
EXCHANGE	H	H	Store Bus A and Bus B Data
BUS A AND B	L	H	Readout Stored Data

OUTPUT-CONTROL FUNCTION TABLE

OCAB	OCBA	OUTPUT FUNCTION
L	X	Disable Bus B Outputs (Hi-Z)
H	X	Enable Bus B Outputs
X	L	Disable Bus A Outputs (Hi-Z)
X	H	Enable Bus A Outputs

disable the outputs as shown in the output-control function table, regardless of the latch function in process. Store operations can be performed with the outputs disabled to a high impedance (Hi-Z). In the Hi-Z state the inputs/outputs neither load nor drive the bus lines significantly. The p-n-p inputs feature typically 400 millivolts of hysteresis to enhance noise rejection.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage		5.5 V
Off-state output voltage		5.5 V
Operating free-air temperature range:	SN54S226 (see Note 2)	−55°C to 125°C
	SN74S226	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. An SN54S226 in the J package operating at temperatures above 113°C requires a heat-sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more than 48°C/W.

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recommended operating conditions

		SN54S226			SN74S226			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
High-level output current, I_{OH}				−6.5			−10.3	mA
Data setup time, t_{su}	Data (A or B)	0↓			0↓			ns
	Select	0↓			0↓			ns
Data hold time, t_h	Data (A or B)	30↓			30↓			ns
	Select	30↓			30↓			ns
Operating free-air temperature, T_A (see Note 2)		−55		125	0		70	°C

↓The arrow indicates that the high-to-low transition of the enable input is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	SN54S226	V_{CC} = MIN, V_{IH} = 2 V,	SN54S226	2.4	3.3		V
		SN74S226	V_{IL} = 0.8 V, I_{OH} = MAX	SN74S226	2.4	2.9		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5	V
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V				100	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V				−100	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V				100	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5 V				−380	μA
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−50		−180	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3			125	185	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTES: 2. An SN54S226 in the J package operating at temperatures above 113°C requires a heat-sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more than 48°C/W.

3. I_{CC} is measured with all inputs (and outputs) grounded.

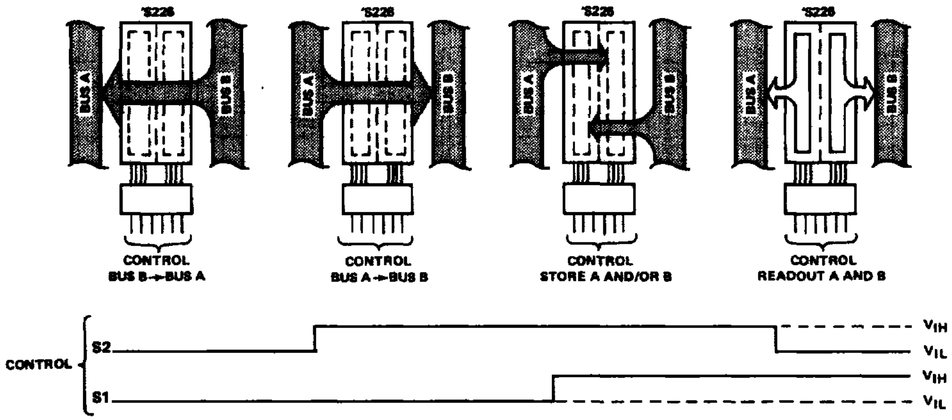
switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	B or A	$C_L = 50$ pF, $R_L = 280\ \Omega$, See Note 4		20	30	ns
t_{PHL}					15	30	
t_{PLH}	Select	Any			25	37	ns
t_{PHL}					19	30	
t_{PLH}	Strobe GBA or GAB	A or B			25	37	ns
t_{PHL}					19	30	
t_{PZH}	Output Control OCBA or OCAB	A or B			12	20	ns
t_{PZL}					12	20	
t_{PHZ}	Output Control OCBA or OCAB	A or B	$C_L = 5$ pF, $R_L = 280\ \Omega$, See Note 4		10	15	ns
t_{PLZ}					10	15	

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, low-to-high-level output
t_{ZH} ≡ output enable time to high level
t_{ZL} ≡ output enable time to low level
t_{HZ} ≡ output disable time from high level
t_{LZ} ≡ output disable time from low level
NOTE 4: Load circuits and voltage waveforms are shown on page 3-10.

applications

The following examples demonstrate four fundamental bus-management functions that can be performed with the 'S226. Exchange of data on the two bus lines can be accomplished with a single high-to-low transition at S2 when S1 is high.



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