Description

The GM71V(S)16160C/CL is the new generation dynamic RAM organized 1,048,576 x 16 bit. GM71V(S)16160C/CL has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71V(S)16160C/CL offers Fast Page Mode as a high speed access mode. Multiplexed address inputs permit the GM71V(S)16160C/CL to be packaged in standard 400 mil 42pin plastic SOJ, and standard 400mil 44(50)pin plastic TSOP II. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

Features

* 1,048,576 Words x 16 Bit Organization
* Fast Page Mode Capability
* Single Power Supply (3.3V+/-0.3V)
* Fast Access Time & Cycle Time

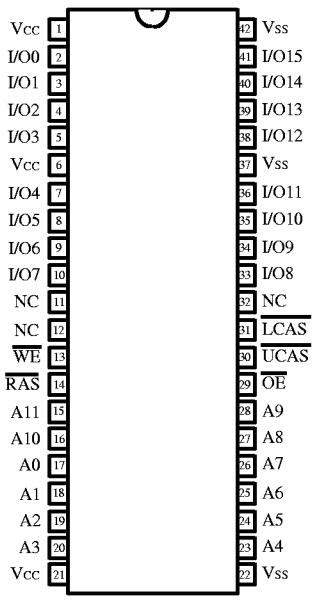
(Unit: ns)

	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
GM71V(S)16160C/CL-5	50	13	90	35
GM71V(S)16160C/CL-6	60	15	110	40
GM71V(S)16160C/CL-7	70	18	130	45

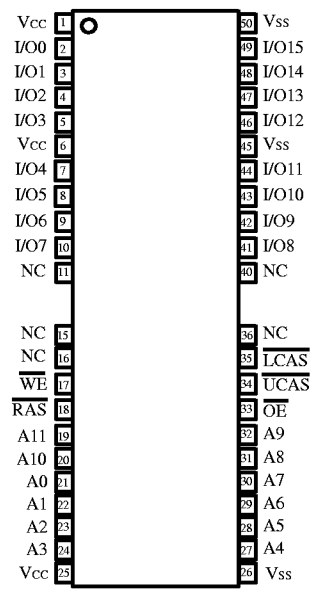
* Low Power
  Active : 396/360/324mW (MAX)
  Standby : 7.2mW (CMOS level : MAX)
  0.54mW (L-version : MAX)
* $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
* All inputs and outputs TTL Compatible
*4096 Refresh Cycles/64ms
* 4096 Refresh Cycles/128ms (L-version)
* Self Refresh Operation (L-version)
* Battery Back Up Operation (L-version)
* 2 $\overline{CAS}$ byte Control

Pin Configuration

42 SOJ



44(50) TSOP II



(Top View)

Pin Description

Pin	Function	Pin	Function
A0-A11	Address Inputs	$\overline{WE}$	Read/Write Enable
A0-A11	Refresh Address Inputs	$\overline{OE}$	Output Enable
I/O0-I/O15	Data Input/ Data Output	V_{CC}	Power (+3.3V)
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground
$\overline{UCAS}$, $\overline{LCAS}$	Column Address Strobe	NC	No Connection

Ordering Information

Type No.	Access Time	Package
GM71V(S)16160CJ/CLJ -5 GM71V(S)16160CJ/CLJ -6 GM71V(S)16160CJ/CLJ -7	50ns 60ns 70ns	400 Mil 42 Pin Plastic SOJ
GM71V(S)16160CT/CLT -5 GM71V(S)16160CT/CLT -6 GM71V(S)16160CT/CLT -7	50ns 60ns 70ns	400 Mil 44(50) Pin Plastic TSOP II

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	C
T_{STG}	Storage Temperature	-55 ~ 125	C
$V_{IN/OUT}$	Voltage on any Pin Relative to V_{SS}	-0.5 ~ Vcc+0.5 (<=4.6V(MAX))	V
V_{CC}	Supply Voltage Relative to V_{SS}	-0.5 ~ 4.6	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.0	W

Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended DC Operating Conditions (T_A = 0 ~ +70C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	-	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V

Note: All voltage referred to Vss.
The supply voltage with all VCC pins must be on the same level. The supply voltage with all VSS pins must be on the same level.

Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	Output	Operation		Notes
H	D	D	D	D	Open	Standby		1,3
L	L	H	H	L	Valid	Lower byte	Read cycle	1,3
L	H	L	H	L	Valid	Upper byte		
L	L	L	H	L	Valid	Word		
L	L	H	L	D	Open	Lower byte	Early write cycle	1,2,3
L	H	L	L	D	Open	Upper byte		
L	L	L	L	D	Open	Word		
L	L	H	L	H	Undefined	Lower byte	Delayed Write cycle	1,2,3
L	H	L	L	H	Undefined	Upper byte		
L	L	L	L	H	Undefined	Word		
L	L	H	H to L	L to H	Valid	Lower byte	Read-modify -write cycle	1,3
L	H	L	H to L	L to H	Valid	Upper byte		
L	L	L	H to L	L to H	Valid	Word		
H to L	H	L	D	D	Open	Word	CBR Refresh or Self Refresh (L-series)	1,3
H to L	L	H	D	D	Open	Word		
H to L	L	L	D	D	Open	Word		
L	H	H	D	D	Open	Word	$\overline{RAS}$-only Refresh cycle	1,3
L	L	L	H	H	Open	Read cycle (Output disabled)		1,3

Notes: 1. H: High (inactive) L: Low(active) D: H or L
2. twcs >= 0ns Early write cycle
twcs <= 0ns Delayed write cycle
3. Mode is determined by the OR function of the $\overline{UCAS}$ and $\overline{LCAS}$. (Mode is set by earliest of $\overline{UCAS}$ and $\overline{LCAS}$ active edge and reset by the latest of $\overline{UCAS}$ and $\overline{LCAS}$ inactive edge.) However write OPERATION and output High-Z control are done independently by each $\overline{UCAS}$,$\overline{LCAS}$.
ex) if $\overline{RAS}$ = H to L, $\overline{UCAS}$ = H, $\overline{LCAS}$ = L, then $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle is selected.

DC Electrical Characteristics (V_{CC} = 3.3V+/-0.3V, V_{SS} = 0V, T_A = 0 ~ 70C)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = -2mA)		2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ Cycling: t_{RC} = t_{RC} min)	50ns	-	110	mA	1, 2
		60ns	-	100		
		70ns	-	90		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ = V_{IH}, D_{OUT} = High-Z)		-	2	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Refresh Mode (t_{RC} = t_{RC} min)	50ns	-	110	mA	2
		60ns	-	100		
		70ns	-	90		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode (t_{PC} = t_{PC} min)	50ns	-	115	mA	1, 3
		60ns	-	105		
		70ns	-	95		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ >= V_{CC} - 0.2V, D_{OUT} = High-Z)		-	1	mA	
			-	150	uA	5
I_{CC6}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	50ns	-	110	mA	
		60ns	-	100		
		70ns	-	90		
I_{CC7}	Battery Back Up Operating Current (Standby with CBR Refresh) (t_{RC}=31.3us, t_{RAS}<=0.3us, D_{OUT}=High-Z)		-	400	uA	4,5
I_{CC8}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{UCAS}$, $\overline{LCAS}$ = V_{IL} D_{OUT} = Enable		-	5	mA	1
I_{CC9}	Self-Refresh Mode Current ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$<=0.2V, D_{OUT}=High-Z)		-	250	uA	5
$I_{L(I)}$	Input Leakage Current Any Input (0V<=V_{IN}<= 4.6V)		-10	10	uA	
$I_{L(O)}$	Output Leakage Current (D_{OUT} is Disabled, 0V<=V_{OUT}<= 4.6V)		-10	10	uA	

Note: 1. I_{CC} depends on output load condition when the device is selected.
I_{CC}(max) is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{UCAS}$ and $\overline{LCAS}$ = V_{IH}.
4. $\overline{UCAS}$ = L (<=0.2) and $\overline{LCAS}$ = L (<=0.2) while $\overline{RAS}$ = L (<=0.2).
5. L-version.

Capacitance (V_{CC} = 3.3V+/-0.3V, T_A = 25C)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (Address)	-	5	pF	1
C_{I2}	Input Capacitance (Clocks)	-	7	pF	1
$C_{I/O}$	Output Capacitance (Data-In/Out)	-	7	pF	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{UCAS}$ and $\overline{LCAS}$ = V_{IH} to disable D_{OUT}.

AC Characteristics (V_{CC} = 3.3V+/-0.3V, T_A = 0 ~ +70C, Note 1, 2, 18, 19, 20)

Test Conditions

Input rise and fall times : 5 ns
Input timing reference levels : 0.8V, 2.0V
Output timing reference levels : 0.8V, 2.0V
Output load : 1TTL gate + C_L (100 pF)
(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GM71V(S)16160 C/CL-5		GM71V(S)16160 C/CL-6		GM71V(S)16160 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	90	-	110	-	130	-	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	30	-	40	-	50	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	8	-	10	-	10	-	ns	24
t_{RAS}	$\overline{RAS}$ Pulse Width	50	10,000	60	10,000	70	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	13	10,000	15	10,000	18	10,000	ns	
t_{ASR}	Row Address Set up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	8	-	10	-	10	-	ns	
t_{ASC}	Column Address Set-up Time	0	-	0	-	0	-	ns	21
t_{CAH}	Column Address Hold Time	8	-	10	-	15	-	ns	21
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	45	20	45	20	52	ns	3
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	30	15	30	15	35	ns	4
t_{RSH}	$\overline{RAS}$ Hold Time	13	-	15	-	18	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	50	-	60	-	70	-	ns	23
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	22
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	13	-	15	-	18	-	ns	5
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	0	-	0	-	0	-	ns	6
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	-	0	-	0	-	ns	6
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7

Read Cycle

Symbol	Parameter	GM71V(S)16160 C/CL-5		GM71V(S)16160 C/CL-6		GM71V(S)16160 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	-	50	-	60	-	70	ns	8,9
t_{CAC}	Access Time from $\overline{CAS}$	-	13	-	15	-	18	ns	9,10,17
t_{AA}	Access Time from Address	-	25	-	30	-	35	ns	9,11,17
t_{OAC}	Access Time from $\overline{OE}$	-	13	-	15	-	18	ns	9,25
t_{RCS}	Read Command Setup Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	-	0	-	0	-	ns	12,22
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	-	5	-	5	-	ns	12
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	25	-	30	-	35	-	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	25	-	30	-	35	-	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	0	-	ns	
t_{OH}	Output Data Hold Time	3	-	3	-	3	-	ns	
t_{OHO}	Output Data Hold Time from $\overline{OE}$	3	-	3	-	3	-	ns	
t_{OFF}	Output Buffer Turn-off Time	-	13	-	15	-	15	ns	13
t_{OEZ}	Output Buffer Turn-off Time to $\overline{OE}$	-	13	-	15	-	15	ns	13
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	13	-	15	-	18	-	ns	5

Write Cycle

Symbol	Parameter	GM71V(S)16160 C/CL-5		GM71V(S)16160 C/CL-6		GM71V(S)16160 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Setup Time	0	-	0	-	0	-	ns	14,21
t_{WCH}	Write Command Hold Time	8	-	10	-	15	-	ns	21
t_{WP}	Write Command Pulse Width	8	-	10	-	10	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	13	-	15	-	18	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	13	-	15	-	18	-	ns	23
t_{DS}	Data-in Setup Time	0	-	0	-	0	-	ns	15,23
t_{DH}	Data-in Hold Time	8	-	10	-	15	-	ns	15,23

Read- Modify-Write Cycle

Symbol	Parameter	GM71V(S)16160 C/CL-5		GM71V(S)16160 C/CL-6		GM71V(S)16160 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	131	-	155	-	181	-	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	73	-	85	-	98	-	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	36	-	40	-	46	-	ns	14
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	48	-	55	-	63	-	ns	14
t_{OEH}	$\overline{OE}$ Hold Time from $\overline{WE}$	13	-	15	-	18	-	ns	

Refresh Cycle

Symbol	Parameter	GM71V(S)16160 C/CL-5		GM71V(S)16160 C/CL-6		GM71V(S)16160 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	5	-	5	-	5	-	§	21
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	8	-	10	-	10	-	§	22
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	-	5	-	5	-	§	21

Fast Page Mode Cycle

Symbol	Parameter	GM71V(S)16160 C/CL-5		GM71V(S)16160 C/CL-6		GM71V(S)16160 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	35	-	40	-	45	-	§	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	-	100,000	-	100,000	-	100,000	§	16
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	-	30	-	35	-	40	§	9,17,22
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	30	-	35	-	40	-	§	

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	GM71V(S)16160 C/CL-5		GM71V(S)16160 C/CL-6		GM71V(S)16160 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	76	-	85	-	96	-	§	
t_{CPW}	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	53	-	60	-	68	-	§	14,22

Self Refresh Mode

Symbol	Parameter	GM71VS16160 CL-5		GM71VS16160 CL-6		GM71VS16160 CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RASS}	$\overline{RAS}$ Pulse Width(Self-Refresh)	100	-	100	-	100	-	us	26
t_{RPS}	$\overline{RAS}$ Precharge Time(Self-Refresh)	90	-	110	-	130	-	ns	
t_{CHS}	$\overline{CAS}$ Hold Time(Self-Refresh)	-50	-	-50	-	-50	-	ns	

Notes:

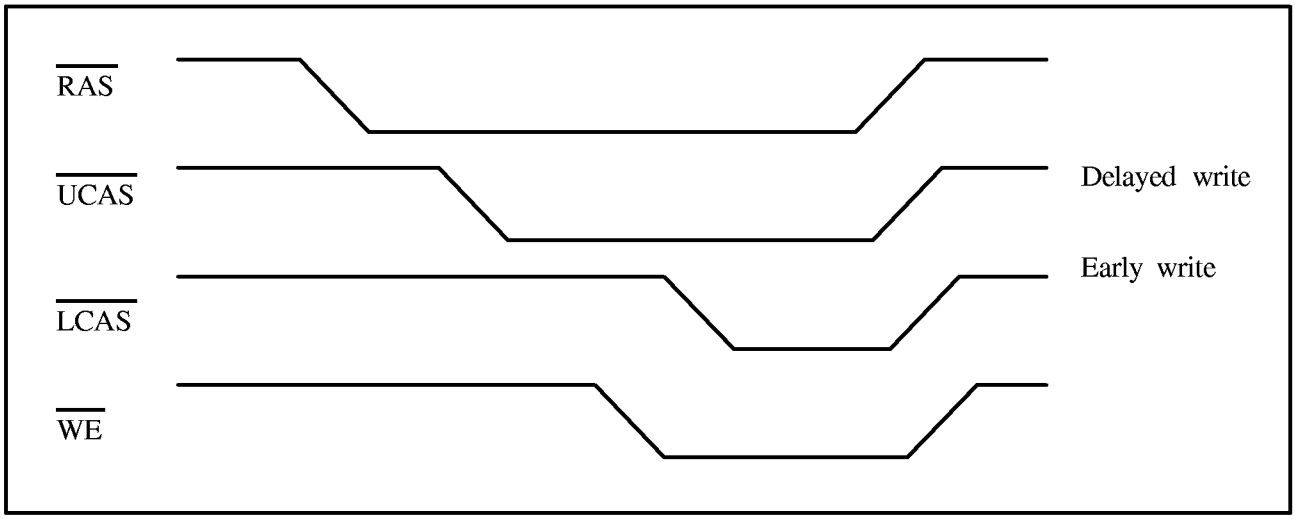
1. AC measurements assume tT = 5ns.
2. An initial pause of 200us is required after power up followed by a minimum of eight initialization cycles(any combination of cycles containing $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
3. Operation with the t_{RCD}(max)limit insures that tRAC(max)can be met, tRCD(max)is specified as a reference point only; if t_{RCD} >= t_{RAD}(max) + t_{AA}(max) - t_{CAC}(max), then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD}(max) limit insures that t_{RAC}(max)can be met, t_{RAD}(max)is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD}(max)limit, then access time is controlled exclusively by t_{AA}.
5. Either t_{ODD} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH}(min) and V_{IL}(max).
8. Assumes that t_{RCD} <= t_{RCD}(max) and t_{RAD} <= t_{RAD}(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, tRAC exceeds the value shown.
9. Measured with a load circuit equivalent to 2 TTL load and 100pF.
10. Assumes that t_{RCD} >= t_{RCD}(max) and t_{RCD} + t_{CAC}(max) >= t_{RAD} + t_{AA}(max).
11. Assumes that t_{RAD} >= t_{RAD}(max) and t_{RCD} + t_{CAC}(max) <= t_{RAD} + t_{AA}(max).
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. t_{OFF}(max) and t_{OEZ}(max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if t_{WCS} >= t_{WCS}(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle ; if t_{RWD} >= t_{RWD}(min), t_{CWD} >=t_{CWD}(min), and t_{AWD} >= t_{AWD}(min), or t_{CWD} >= t_{CWD}(min),t_{AWD} >= t_{AWD}(min) and t_{CPW} >= t_{CPW}(min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of data out (at access time)is indeterminate.

15. These parameters are referred to $\overline{UCAS}$ and $\overline{LCAS}$ leading edge in early write cycles and to WE leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines $\overline{RAS}$ pulse width in fast page mode cycles.
17. Access time is determined by the longest among t_{AA},t_{CAC},and t_{ACP}.
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device. After $\overline{RAS}$ is reset, if t_{OEH} >= t_{CWL}, the I/O pin will remain open circuit (high impedance); if t_{OEH}< t_{CWL}, invalid data will be out at each I/O.
19. When both $\overline{UCAS}$ and $\overline{LCAS}$ go low at the same time, all 16-bit data are written into the device. $\overline{UCAS}$ and $\overline{LCAS}$ cannot be staggered within the same write/read cycles.
20. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
21. t_{ASC}, t_{CAH}, t_{RCS}, t_{WCS},t_{WCH},t_{CSR} and t_{RPC} are determined by the earlier falling edge of $\overline{UCAS}$ or $\overline{LCAS}$.
22. t_{CRP},t_{CHR}, t_{RCH}, t_{ACP} and t_{CPW} are determined by the later rising edge of $\overline{UCAS}$ or $\overline{LCAS}$.
23. t_{CWL}, t_{DH},t_{DS} and t_{CSH} should be satisfied by both $\overline{UCAS}$ and $\overline{LCAS}$.
24. t_{CP} is determined by that time the both $\overline{UCAS}$ and $\overline{LCAS}$ are high.
25. When output buffers are enabled once, sustain the low impedance state until valid data is obtained.
    When output buffer is turned on and off within a very short time, generally it causes large V_{CC}/V_{SS} line noise, which causes to degrade V_{IH} min/V_{IL} max level.
26. Please do not use t_{RASS} timing, 10us <= t_{RASS} <=100us. During this period, the device is in transition state from normal operation mode to self refresh mode. If t_{RASS} >=100us, then $\overline{RAS}$ precharge time should use t_{RPS} instead of t_{RP}.
27. ▭ H or L (H: V_{IH}(min) <= V_{IN} <= V_{IH}(max), L: V_{IL}(min) <= V_{IN} <= V_{IL}(max))

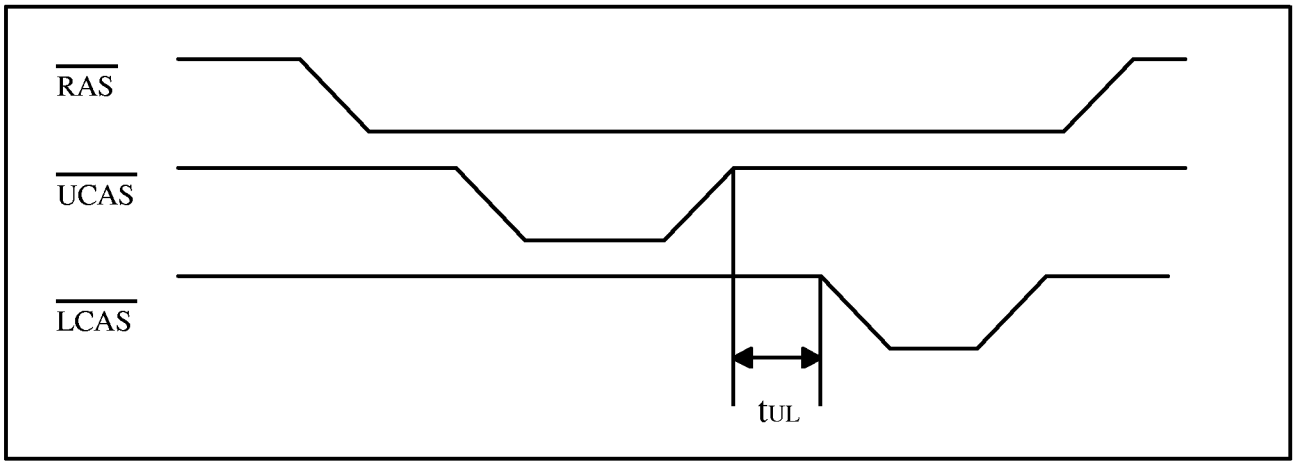
Notes concerning 2CAS control

Please do not separate the $\overline{UCAS}$ / $\overline{LCAS}$ operation timing intentionally. However skew between $\overline{UCAS}$ / $\overline{LCAS}$ are allowed under the following conditions.

1. Each of the $\overline{UCAS}$ / $\overline{LCAS}$ should satisfy the timing specifications individually.
2. Different operation mode for upper/lower byte is not allowed, such as following.



3. Closely separated upper/lower byte control is not allowed. However when the condition ($t_{CP} < t_{UL}$)is satisfied, fast page mode can be performed.



4. Byte control operation by remaining $\overline{UCAS}$ or $\overline{LCAS}$ high is guaranteed.

Timing Waveforms

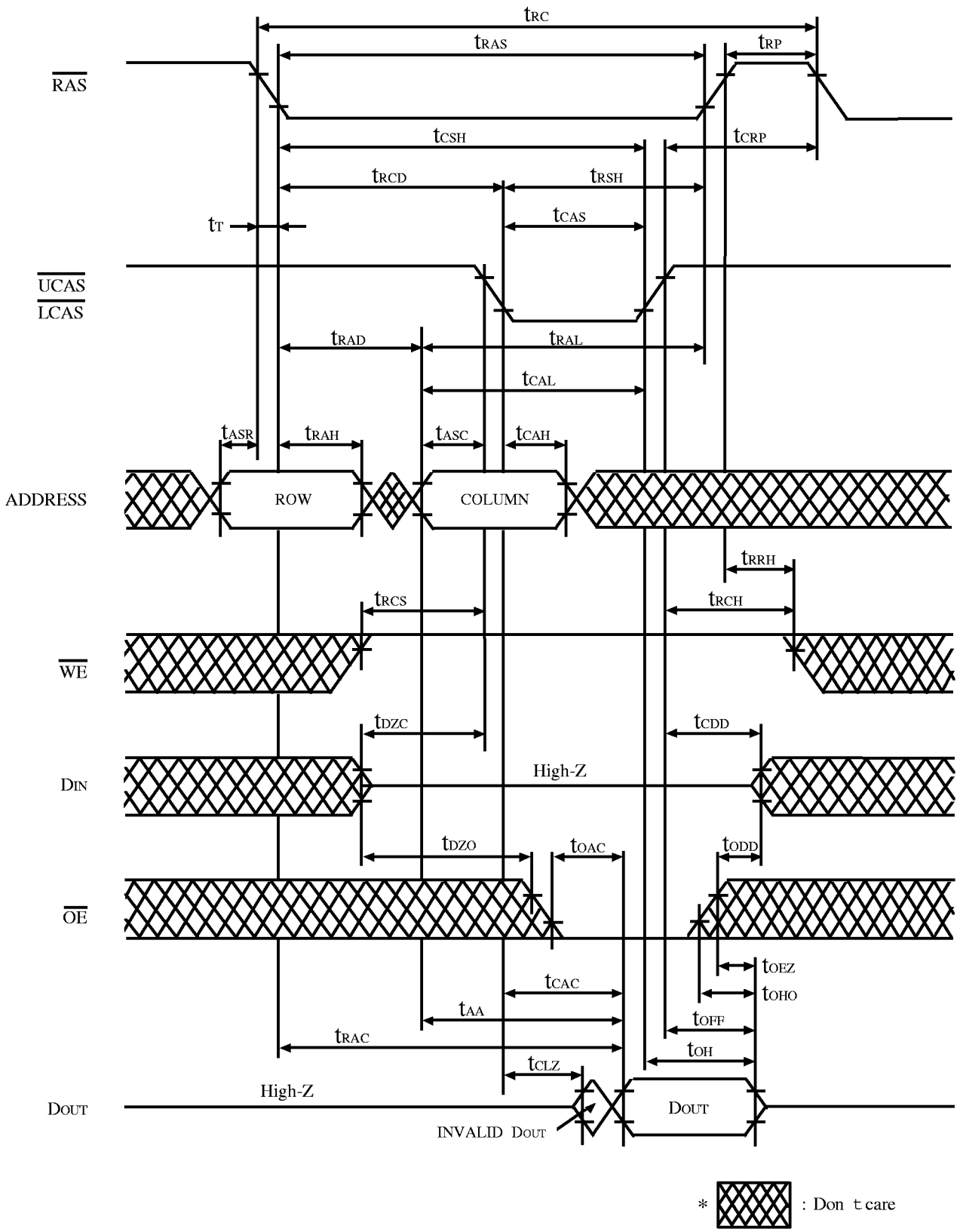


FIGURE 1. READ CYCLE

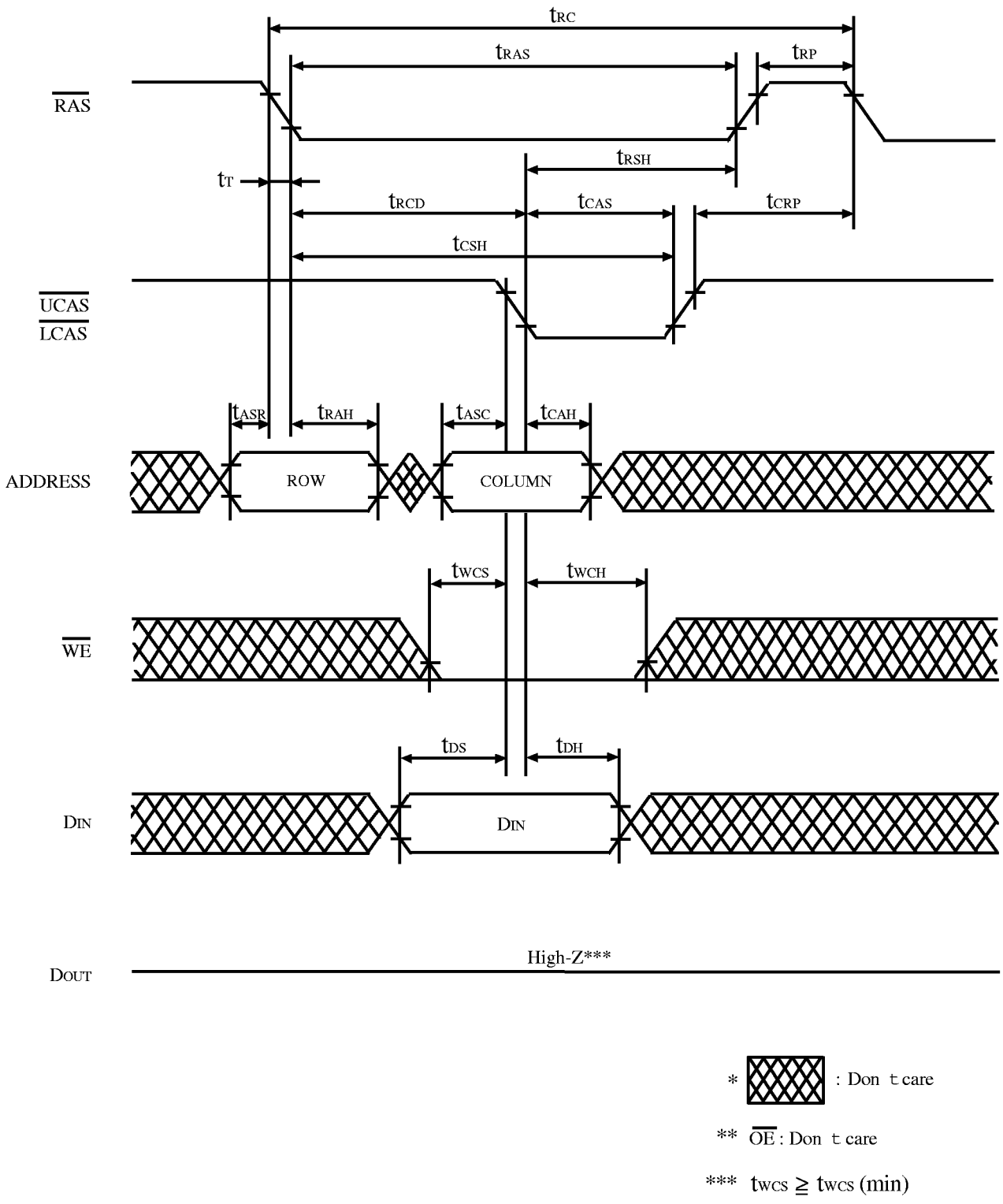


FIGURE 2. EARLY WRITE CYCLE

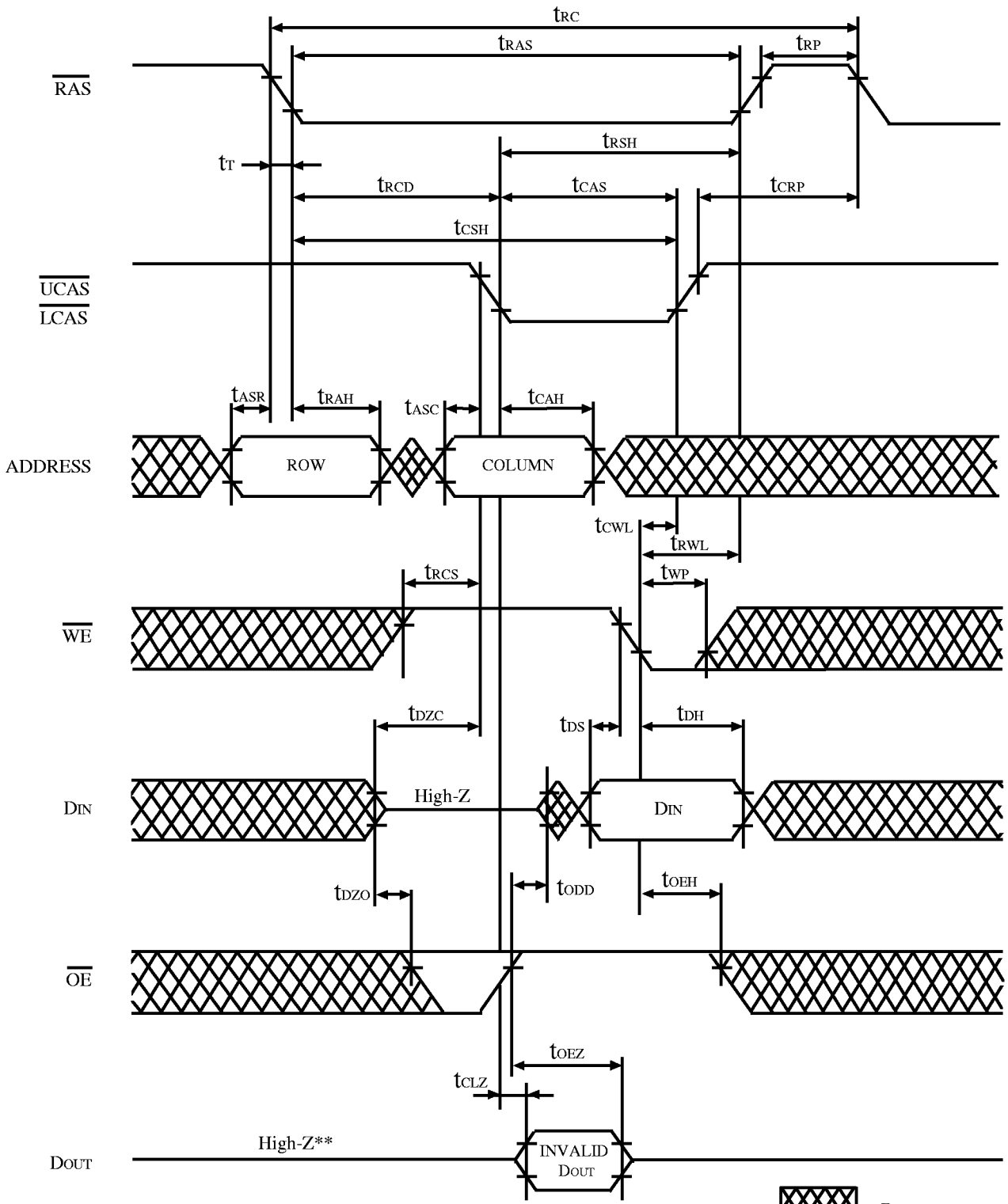


FIGURE 3. DELAYED WRITE CYCLE

*Note : In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device. After $\overline{RAS}$ is reset, if $t_{OEH} >= t_{CWL}$, the I/O pin will remain open circuit (high impedance); if $t_{OEH} <= t_{CWL}$, invalid data will be out at each I/O.

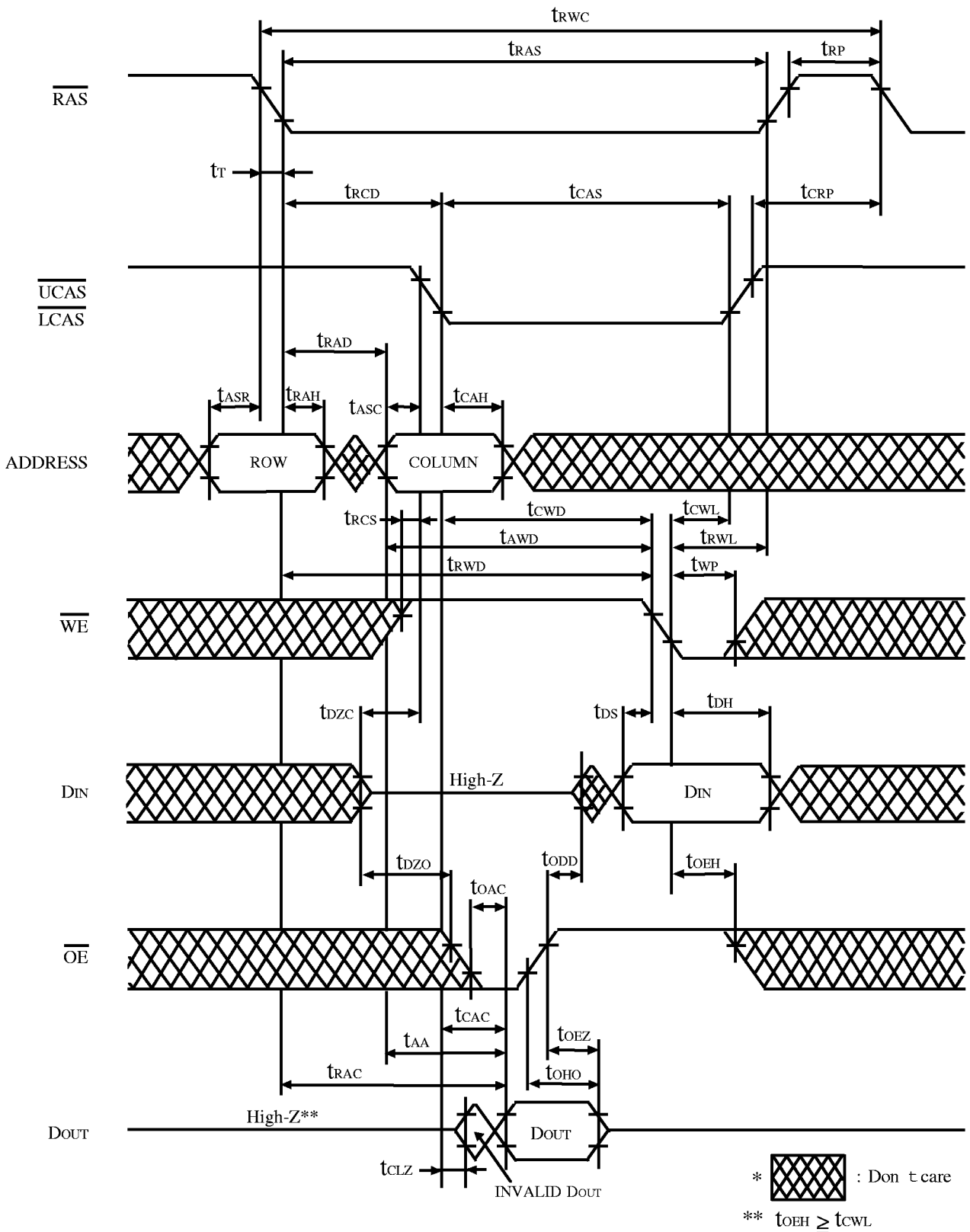


FIGURE 4. READ MODIFY WRITE CYCLE

*Note : In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device. After $\overline{RAS}$ is reset, if $t_{OEH} >= t_{CWL}$, the I/O pin will remain open circuit (high impedance); if $t_{OEH} <= t_{CWL}$, invalid data will be out at each I/O.

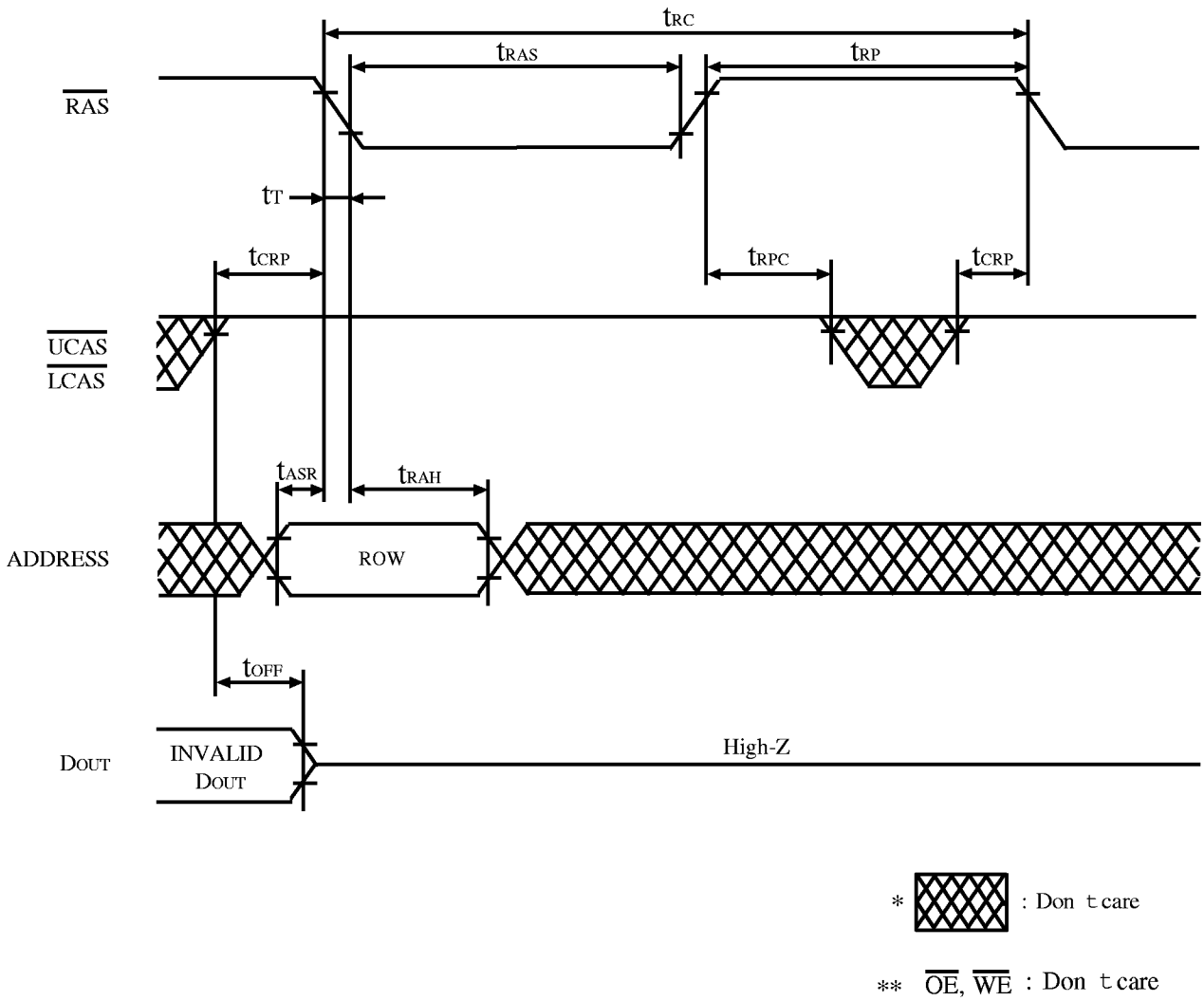


FIGURE 5. $\overline{RAS}$ ONLY REFRESH CYCLE

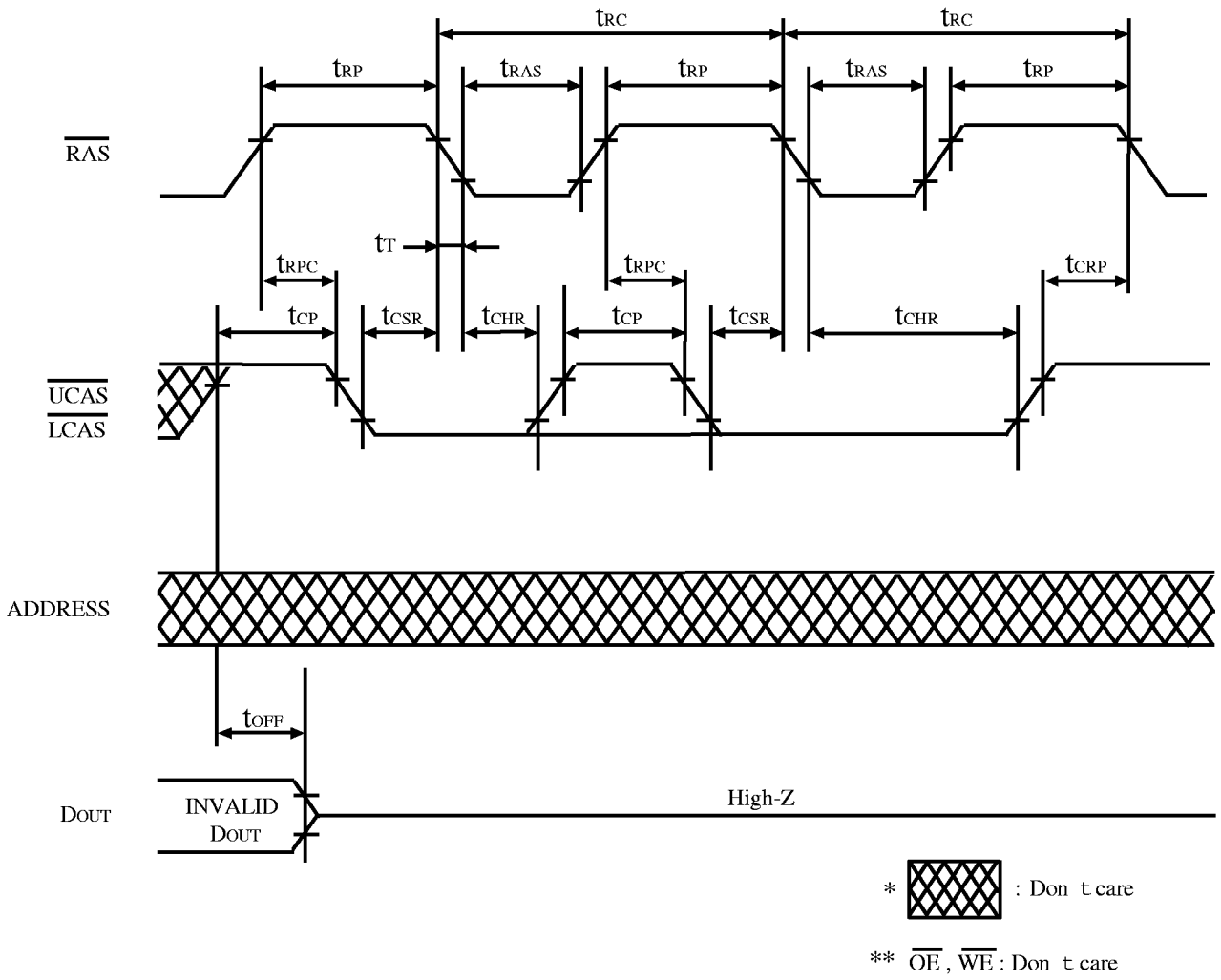


FIGURE 6. $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

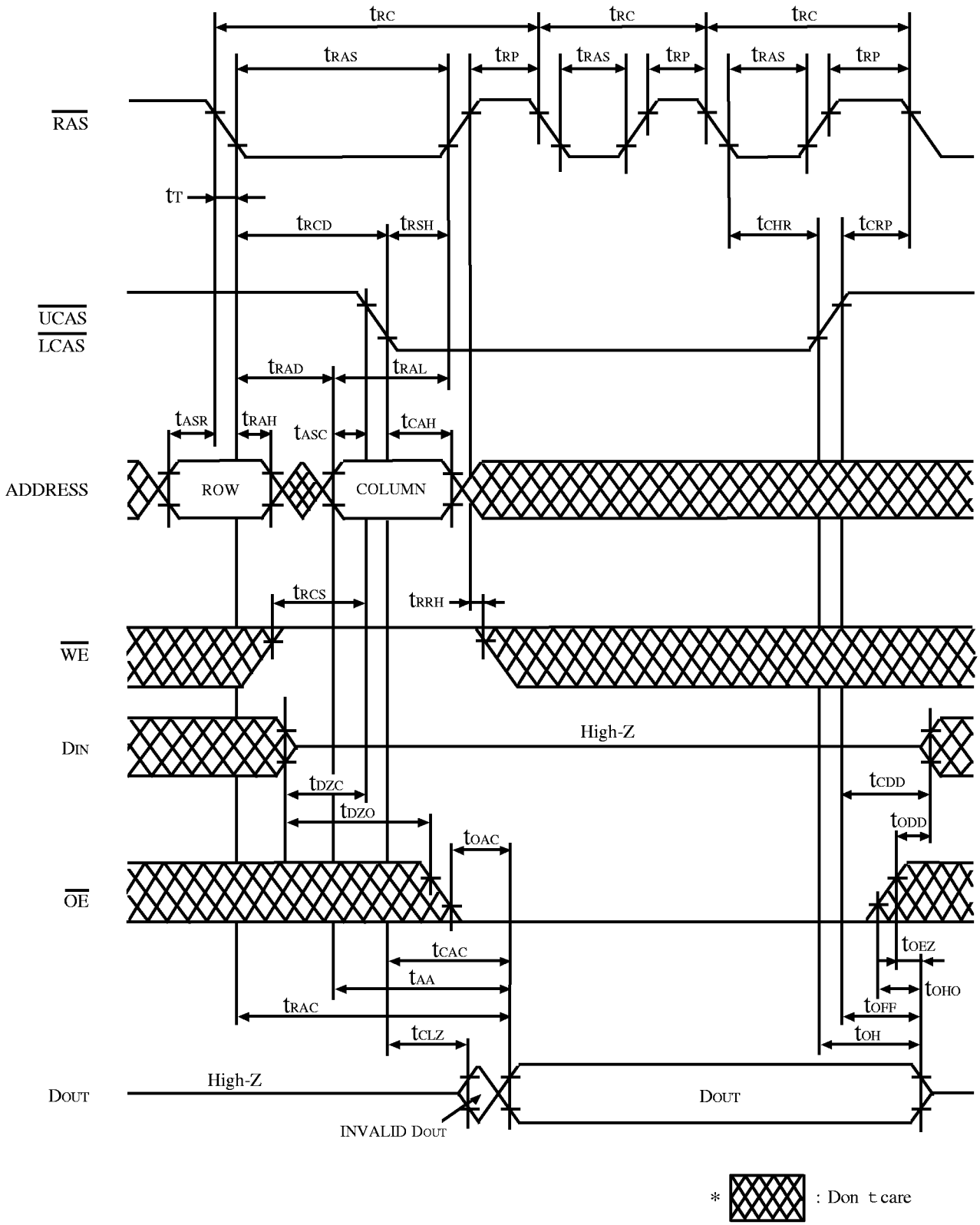


FIGURE 7. HIDDEN REFRESH CYCLE

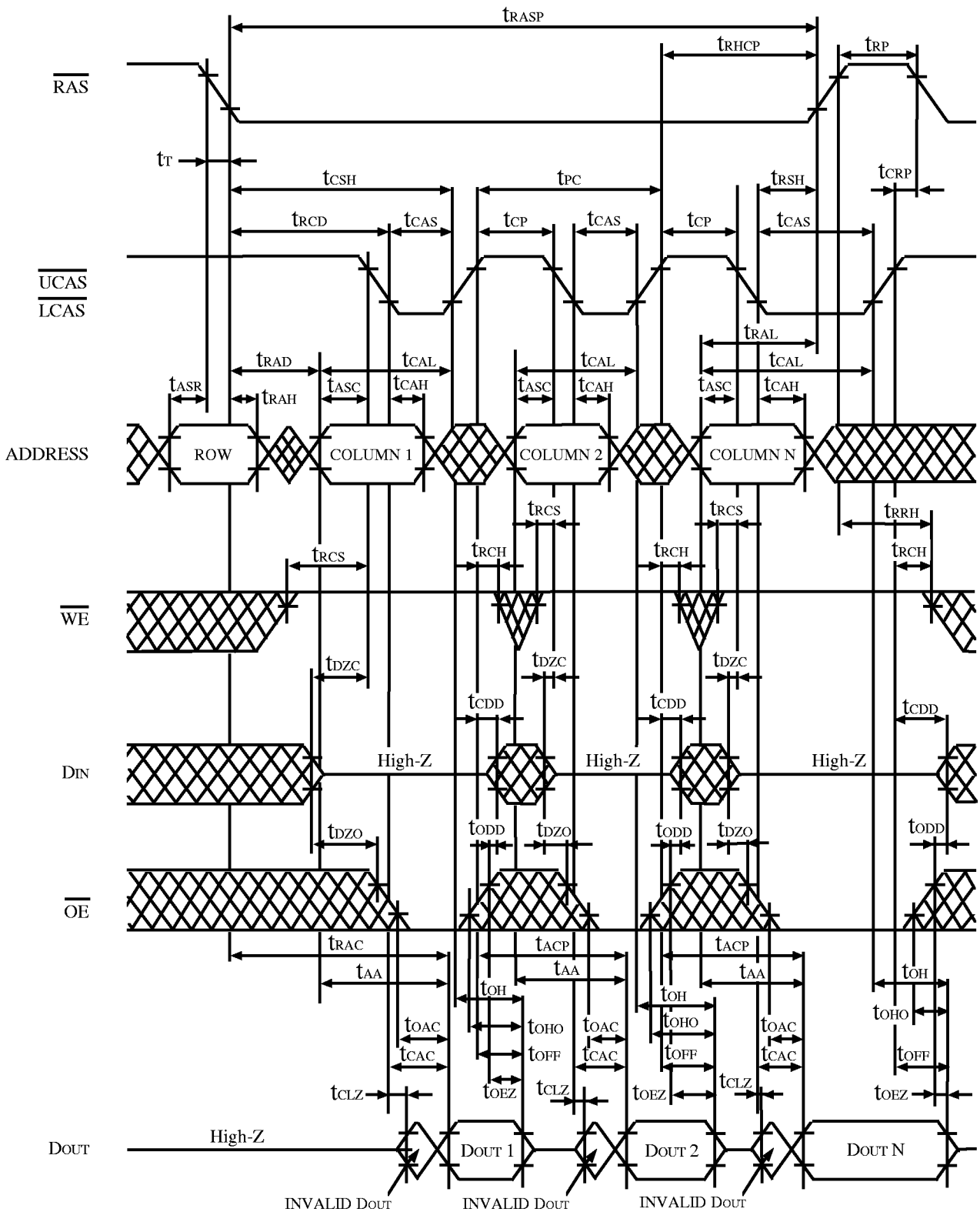
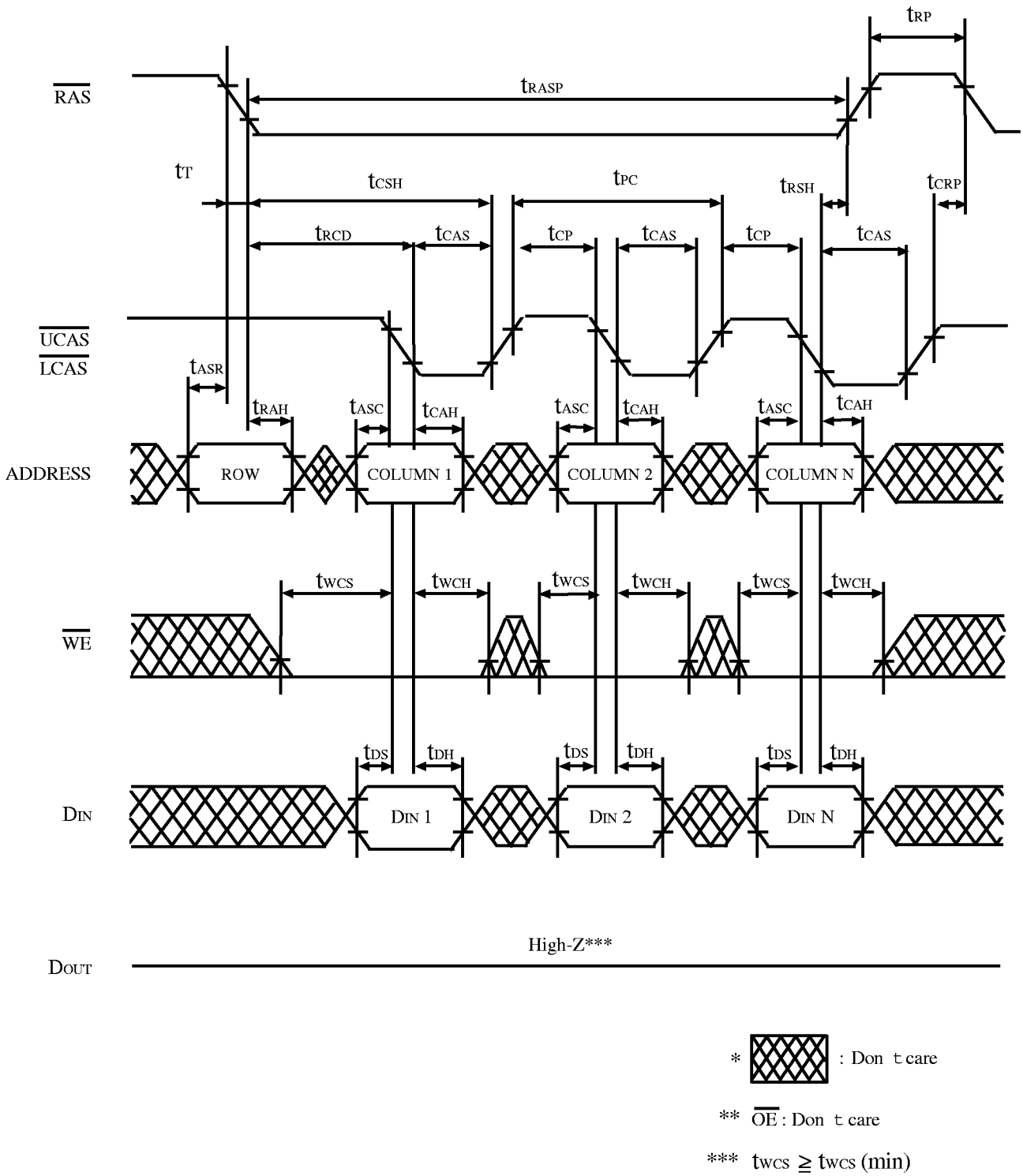


FIGURE 8. FAST PAGE MODE READ CYCLE



* : Don t care

** $\overline{OE}$: Don t care

*** tWCS ≧ tWCS (min)

FIGURE 9. FAST PAGE MODE EARLY WRITE CYCLE

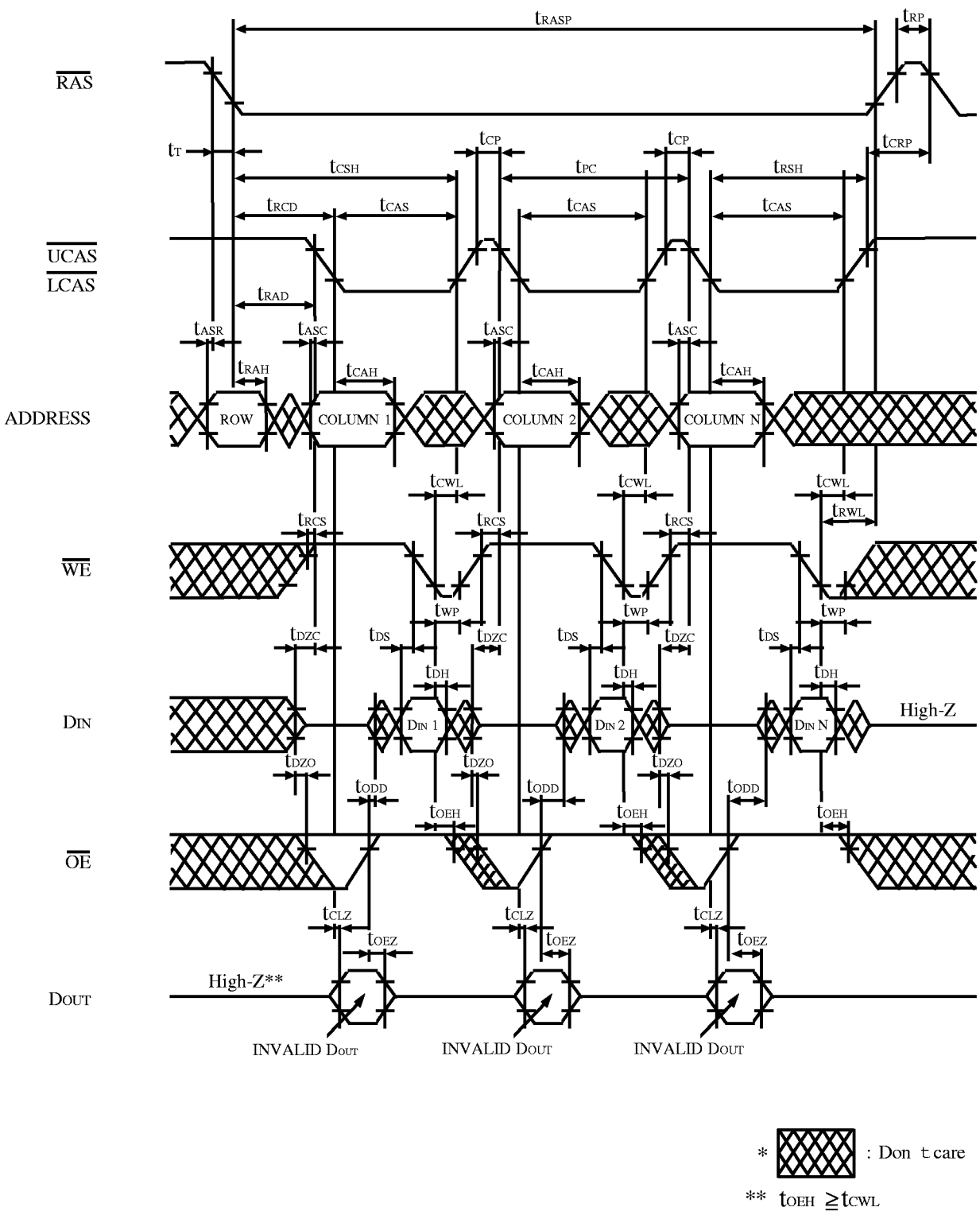


FIGURE 10. FAST PAGE MODE DELAYED WRITE CYCLE

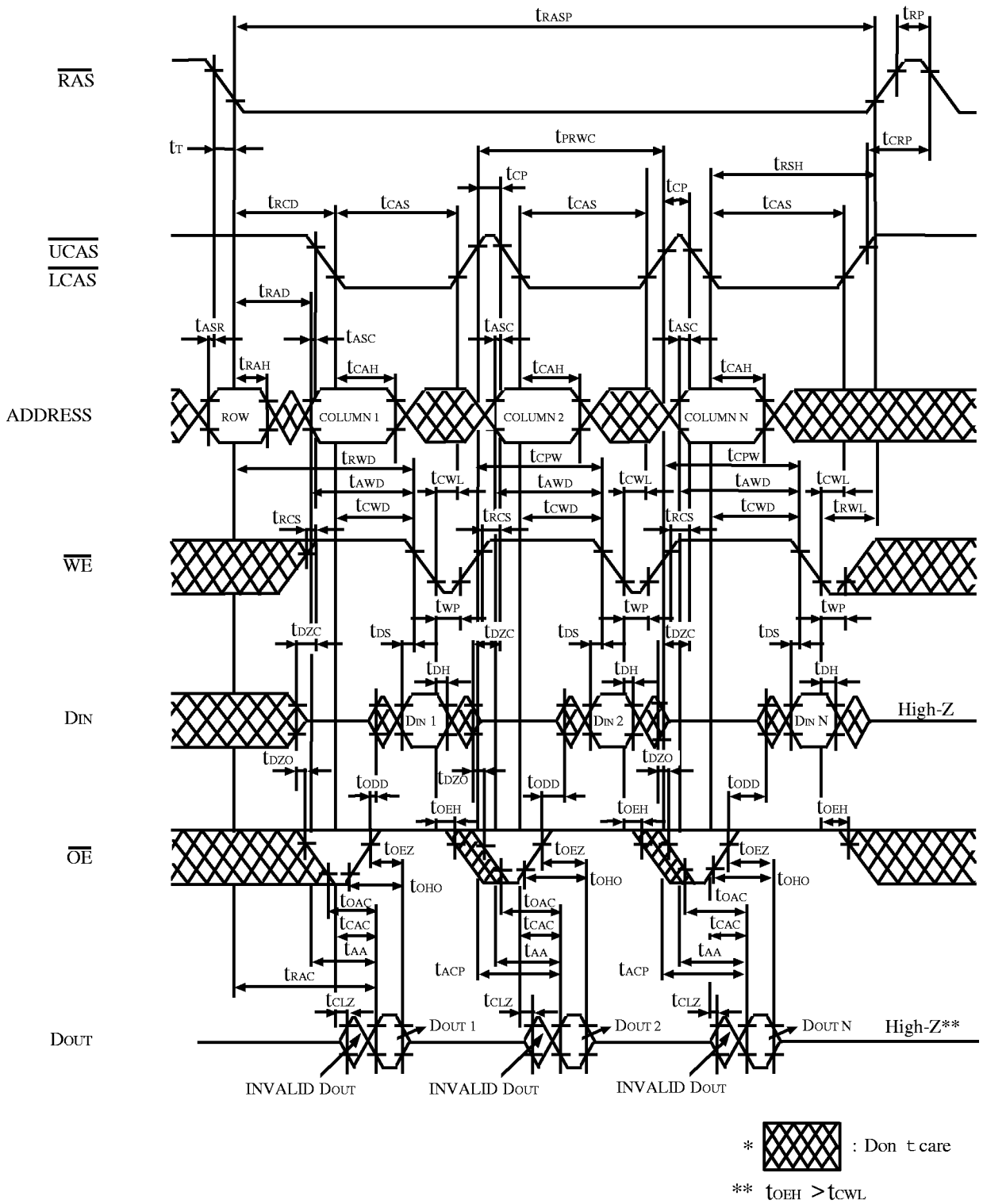
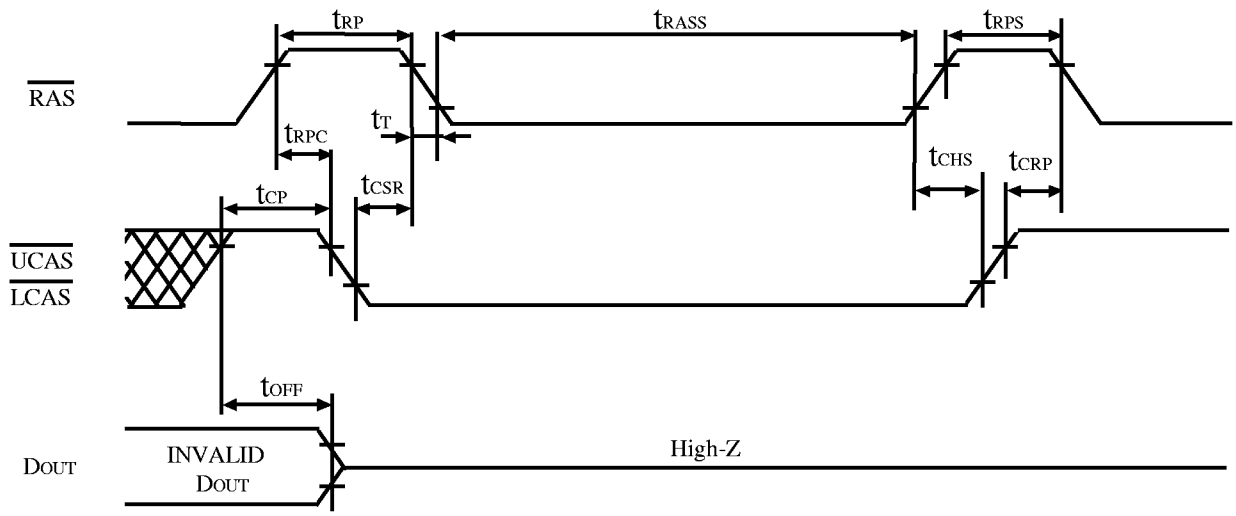


FIGURE 11. FAST PAGE MODE READ MODIFY WRITE CYCLE



* : Don t care

** Address, $\overline{OE}$, $\overline{WE}$: Don t care

The low self refresh current is achieved by introducing extremely long internal refresh cycle. Therefore some care needs to be taken on the refresh.

1. Please do not tRASS timing, 10us<=tRASS<=100us. During this period, the device is in transition state from normal operation mode to self refresh mode. If tRASS>=100us, then $\overline{RAS}$ precharge time should use tRPS instead of tRP.
2. If you use $\overline{RAS}$ only refresh or CBR burst refresh mode in normal read/write cycle, 1024 or 4096 cycles of distributed CBR refresh with 15.6us interval should be executed within 16ms or 64ms immediately after exiting from and before entering into the self refresh mode. *1 *1
3. If you use distributed CBR refresh mode with 15.6us interval in normal read/write cycle, CBR refresh should be executed within 15.6us immediately after exiting from and before entering into the self refresh mode.
4. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.

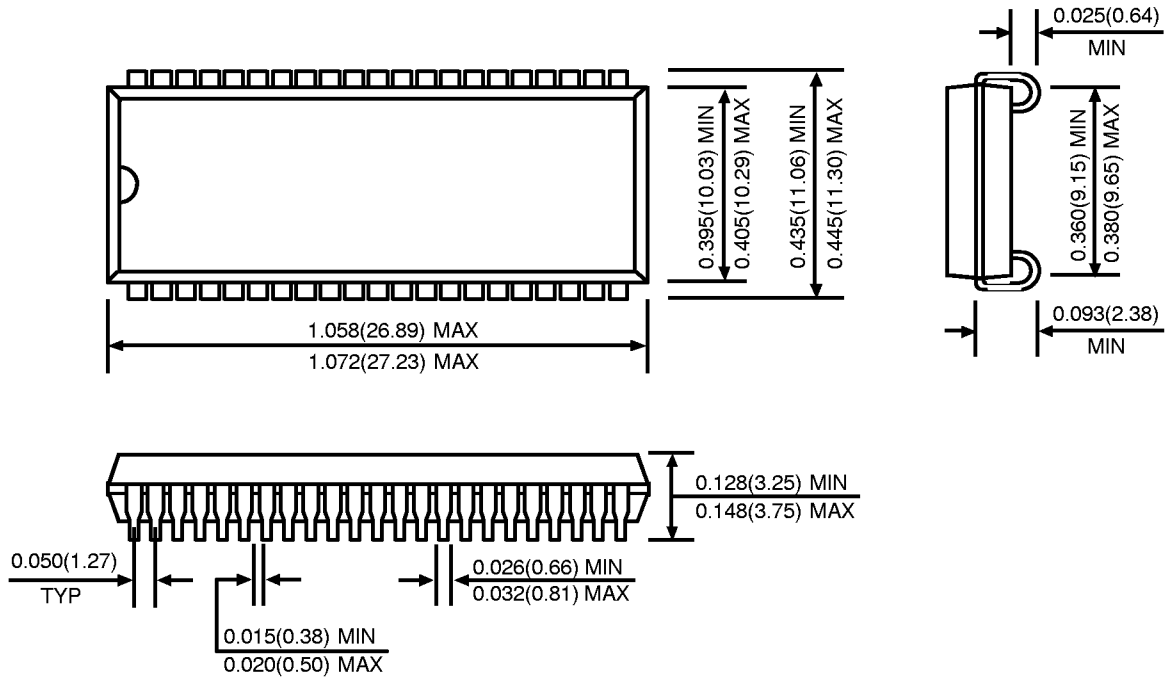
* Note 1 : GM71C(V)16160 (4096 Refresh Cycles / 64ms)
GM71C(V)18160 (1024 Refresh Cycles / 16ms)

FIGURE 12. SELF-REFRESH CYCLE

Package Dimension

Unit: Inches (mm)

42 SOJ



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