Q-TECH
CORPORATION

DUAL IN-LINE PACKAGES

CRYSTAL CLOCK OSCILLATORS

-5.2 to -4.5Vdc & 1.8 to 15Vdc - 0.01Hz to 200MHz

Description

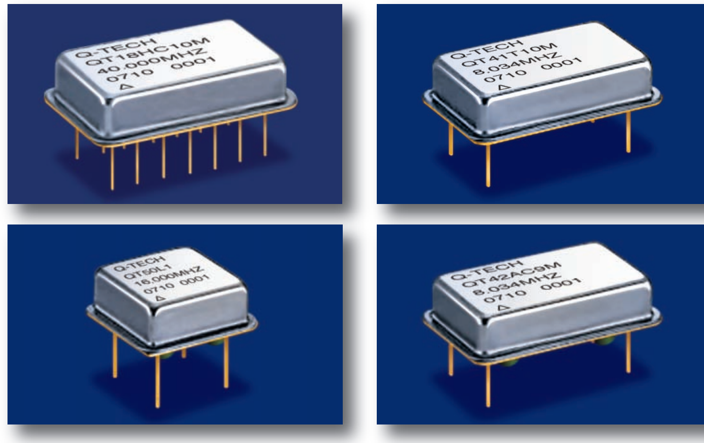
Q-Tech's Dual In-line (DIP) crystal oscillators consist of a source clock square wave generator, logic output buffers and/or logic divider stages, and a round AT high-precision quartz crystal built in a metal through-hole package in DIP-8 or DIP-14 configurations.

Features

- Made in the USA
- ECCN: EAR99
- DFARS 252-225-7014 Compliant: Electronic Component Exemption
- USML Registration # M17677
- Wide frequency range from 0.01Hz to 200MHz
- Available as QPL MIL-PRF-55310/8, /11, /14, /15, /16, /17, /18, /25, and /26
- Wide operating temperature range
- Choice of output logic options
- Supply voltages from 1.8Vdc to 15Vdc
- Lower or higher supply voltages available
- All metal hermetically sealed package
- Tight or custom symmetry available
- Fast rise and fall times
- Fast start-up time
- Capacitive load drive capability (Z output)
- Multiple outputs available
- Fundamental and third overtone designs
- High operating temperature up to +225ºC
- Custom design available tailors to meet customer's needs
- Q-Tech does not use pure lead or pure tin in its products
- RoHS compliant

Applications

- Designed to meet today's requirements for all voltage applications
- Wide military clock applications
- Smart munitions
- Navigation
- Industrial controls
- Microcontroller driver
- Down-hole applications up to +225ºC



Ordering Information

QTXX — XX— D — XX — M — 20.000MHz

Model #

C	=	CMOS +5V to +15V *
AC	=	ACMOS +5V
HC	=	HCMOS +5V
T	=	TTL +5V
L	=	LVHCMOS +3.3V
N	=	LVHCMOS +2.5V
R	=	LVHCMOS +1.8V
E	=	10K ECL -5.2V
EH	=	10KH ECL -5.2V
EF	=	100K/300K ECL -4.5V
PE	=	PECL +5V
LP	=	PECL +3.3V
Z	=	Z output

Tristate Option D
(Left blank if no Tristate)

1	=	± 100ppm	at	0ºC	to	+70ºC
3**	=	± 5ppm	at	0ºC	to	+50ºC
4	=	± 50ppm	at	0ºC	to	+70ºC
5	=	± 25ppm	at	-20ºC	to	+70ºC
6	=	± 50ppm	at	-55ºC	to	+105ºC
9	=	± 50ppm	at	-55ºC	to	+125ºC
10	=	± 100ppm	at	-55ºC	to	+125ºC
11	=	± 50ppm	at	-40ºC	to	+85ºC
12	=	± 100ppm	at	-40ºC	to	+85ºC

Screened to MIL-PRF-55310,level B
(Left blank if no screening)

Output frequency

(*) Please specify supply voltage when ordering CMOS
(**) Require an external capacitor

Frequency stability vs. temperature codes may not be available in all frequencies. Q-Tech will assign a custom part number for custom specifications and all high temperature applications with typical frequency stability at ± 250ppm up to +200ºC.

For Non-Standard requirements, contact Q-Tech Corporation at Sales@Q-Tech.com

Package Information

- Package material (header and leads): Kovar
- Lead finish: Gold Plated – 50µ ~ 80µ inches
  Nickel Underplate – 100µ ~ 250µ inches
- Cover (DIP-14): Pure Nickel Grade A (DIP-8): Stainless Steel
- Package to lid attachment: Resistance weld

Packaging Options

- Standard packaging in black foam
- Optional anti-static plastic tube

Other Options Available For An Additional Charge

- Lead forming available on all packages. Please contact for details.
- Solder Dip Sn/Pb 60/40%
- P. I. N. D. test
- Lead trimming

All DIP packages are available in surface mount form.
Specifications subject to change without prior notice.

Electrical Characteristics

Parameters		C	AC	HC	T	L (*)	ECL / PECL (**)
Output freq. range (Fo)	DIP 14	**0.01Hz — 15MHz**	**0.01Hz — 160MHz**	**0.01Hz — 160MHz**	**0.01Hz — 160MHz**	**0.01Hz — 160MHz**	**1MHz — 200MHz**
	DIP 8	**245Hz — 15MHz**	**0.01Hz — 85MHz**	**0.01Hz — 85MHz**	**10Hz — 85MHz**	**0.01Hz — 100MHz**	**1MHz — 110MHz**
Supply voltage (Vdd)		5V ~ 15Vdc ± 10%	5.0Vdc ± 10%			3.3Vdc ± 10%	-5.2Vdc ± 5% (10K / 10KHECL) 5Vdc ± 5% (PECL) 3.3Vdc ± 5% (LVPECL)
Freq. stability (ΔF/ΔT)		See Option codes					
Operating temp. (Topr)		See Option codes					
Storage temp. (Tsto)		-62ºC to + 125ºC					
Operating supply current (Idd) (No Load)		F and Vdd dependent 3 mA max. at 5V up to 5MHz 25 mA max. at 15V up to 15MHz	20 mA max. - 0.01Hz ~ < 16MHz 25 mA max. - 16MHz ~ < 40MHz 35 mA max. - 40MHz ~ < 60MHz 45 mA max. - 60MHz ~ < 85MHz 55 mA max. - 85MHz ~ < 110MHz 65 mA max. - 110MHz ~ < 125MHz 75 mA max. - 125MHz ~ 160MHz			3 mA max. - 0.01Hz ~ < 500kHz 6 mA max. - 500kHz ~ < 16MHz 10 mA max. - 16MHz ~ < 32MHz 20 mA max. - 32MHz ~ < 60MHz 30 mA max. - 60MHz ~ < 100MHz 40 mA max. - 100MHz ~ < 130MHz 50 mA max. - 130MHz ~ 160MHz	45 mA max. - 1MHz ~ < 125MHz 75 mA max. - 125MHz ~ 200MHz
Symmetry (50% of ouput waveform or 1.4Vdc for TTL)		45/55% max. Fo < 4MHz 40/60% max. Fo ≥ 4MHz	45/55% max. Fo < 12MHz 40/60% max. Fo ≥ 12MHz				45/55% max. Fo < 12MHz 40/60% max. Fo ≥ 12MHz
Rise and Fall times (Tr/Tf) (with typical load)		30ns max. (Measured from 10% to 90%)	15ns max. Fo < 15kHz 6ns max. Fo 15kHz ~ 39.999MHz 3ns max. Fo 40MHz ~ 160MHz (Measured from 10% to 90% CMOS or from 0.8V to 2.0V TTL)				3.5ns max. Fo < 125MHz 3ns max. Fo 125MHz ~ 200MHz (Measured from 20% to 80%)
Output Load		**15pF // 10kΩ**			**10TTL Fo < 20MHz** 6TTL Fo ≥ 20MHz	**15pF // 10kΩ**	50Ω to -2V (10K / 10KH) 50Ω to Vcc -2V (P & LP)
Start-up time (Tstup)		10ms max.					
Output voltage (Voh/Vol)		0.9 x Vdd min.; 0.1 x Vdd max.			2.4V min.; 0.4V max.	0.9 x Vdd min.; 0.1 x Vdd max.	-1.15V min; -1.54V max. (E) 4V min.; 3.37V max. (PE) 2.27V min.; 1.68V max. (LP)
Output Current (Ioh/Iol)		± 1mA typ. at 5V ± 6.8mA typ. at 15V	± 24mA	±8 mA	-1.6mA / TTL +40µA / TTL	± 4mA .	-50mA
Enable/Disable Tristate function Pin 1		Call for details	VIH ≥ 2.2V Oscillation; VIL ≤ 0.8V High Impedance			VIH ≥ 0.7 x Vdd Oscillation; VIL ≤ 0.3 x Vdd High Impedance	Call for details
Jitter RMS 1σ (at 25ºC)		8ps typ. - < 40MHz 5ps typ. - ≥ 40MHz				15ps typ. - < 40MHz 8ps typ. - ≥ 40MHz	Integrated phase jitter 12kHz - 20MHz 1ps typ.
Aging (at 70ºC)		± 5ppm max. first year / ± 2ppm typ. per year thereafter					

DIP 14: QT6, QT18, QT41, QT42, QT47
DIP 8: QT50, QT51, QT55

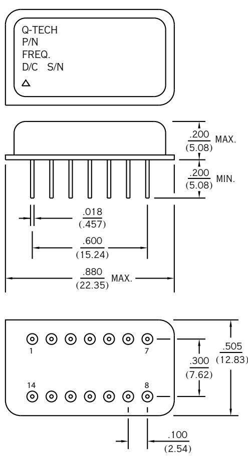
(*) Available in 2.5Vdc (N) or 1.8Vdc (R)
(**) Please contact Q-Tech for details on 100KECL logic (EF)
Z Output logic can drive up to 200 pF load with typical 6ns rise & fall times (tr, tf)

Package Configuration Versus Pin Connections

DIP 14

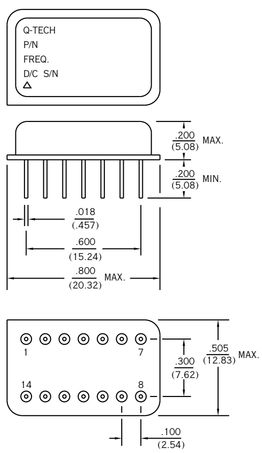
A

QT6



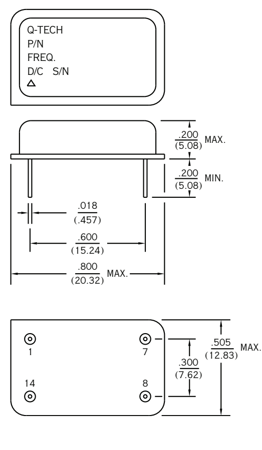
B

QT18



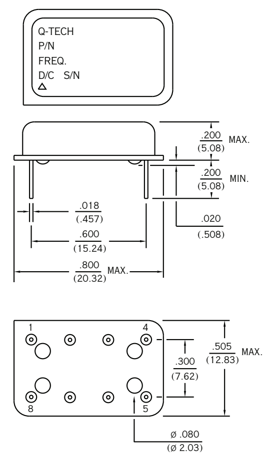
C

QT41



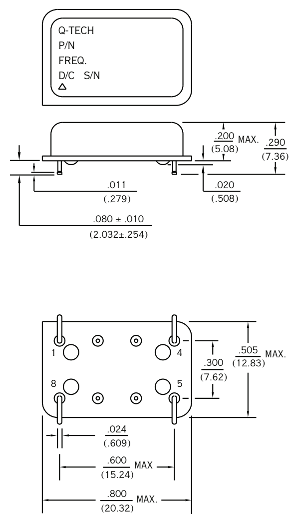
D

QT42



E

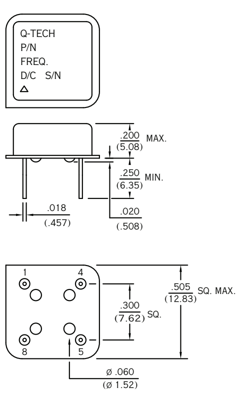
QT47



DIP 8

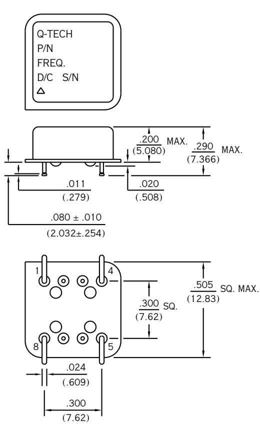
F

QT50



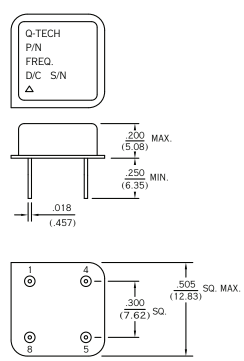
G

QT51



H

QT55



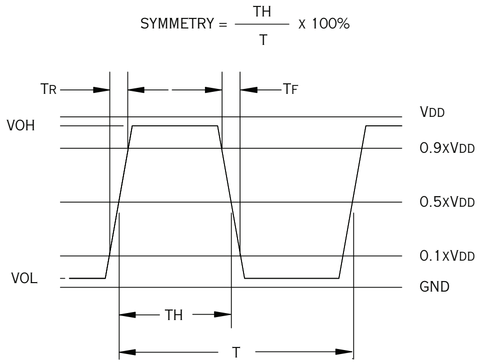
Dimensions are in inches (mm)

QT #	Conf	Vcc	GND	Case	Output (*)	E/D	Ext. Cap	Equivalent MIL-PRF-55310 Configuration
QT4	A	4	7	7	5	1	10 & 11	/14 = QT4T
QT6	A	14	7	7	8	1	10 & 11	/16 = QT6T /17 = QT6T** /18 = QT6C /26A = QT6HC
QT10	A	14	8	2	1	N/A	10 & 11	/08 = QT10T /11 = QT10C /15 = QT10C
QT12	A	14	7	7	4	1	10 & 11	N/A
QT18	B	14	7	7	8	1	10 & 11	N/A
QT41	C	14	7	7	8	1	N/A	/26B = QT41HC
QT42	D	14	7	7	8	1	N/A	N/A
QT47	E	14	7	7	8	1	N/A	N/A
QT50	F	8	4	4	5	1	N/A	N/A
QT51	G	8	4	4	5	1	N/A	N/A
QT55	H	8	4	4	5	1	N/A	N/A

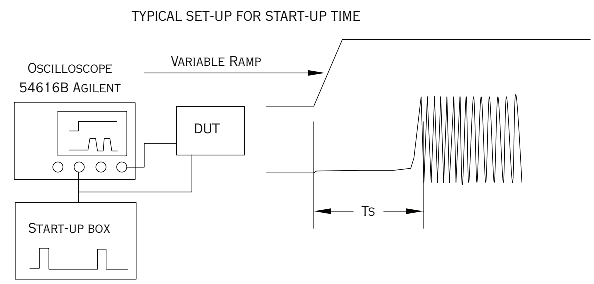
(*) ECL / PECL complimentary output available on pin 9 (For QT6 and QT18 only) with a Q-Tech custom part number

(**) Gated Output, gate control pin 9.

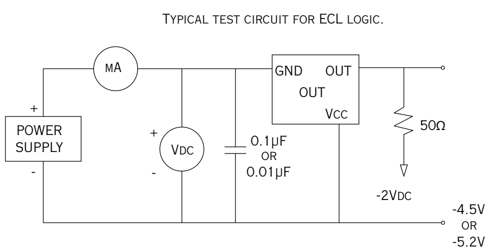
Output Waveform (Typical)

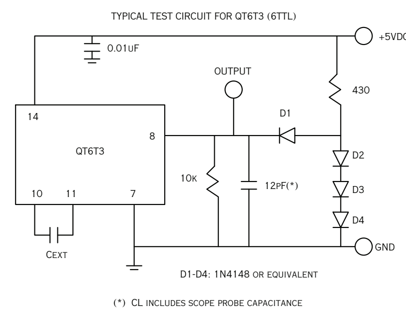


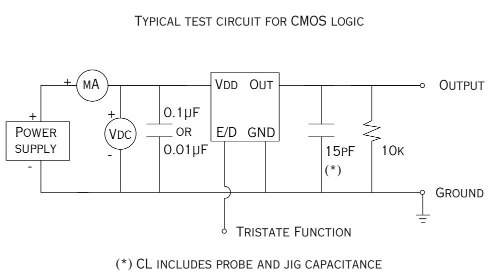
Startup Time



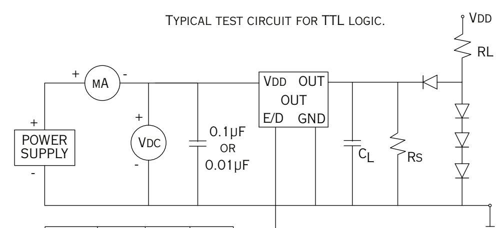
Test Circuit







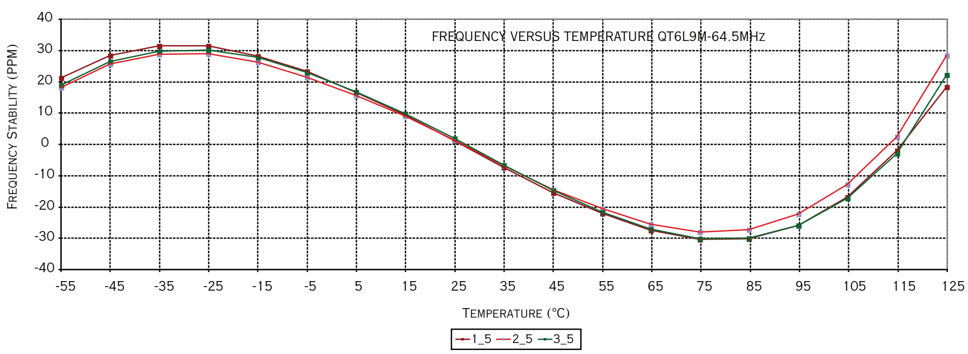
The Tristate function on pin 1 has a built-in pull-up resistor typical 50kΩ, so it can be left floating or tied to Vdd without deteriorating the electrical performance.



LOAD	CL(*)	RL	RS
6 TTL	12PF	430Ω	10KΩ
10 TTL	20PF	270Ω	6KΩ

(*) CL INCLUDES THE LOADING EFFECT OF THE OSCILLOSCOPE PROBE.

Frequency vs. Temperature Curve



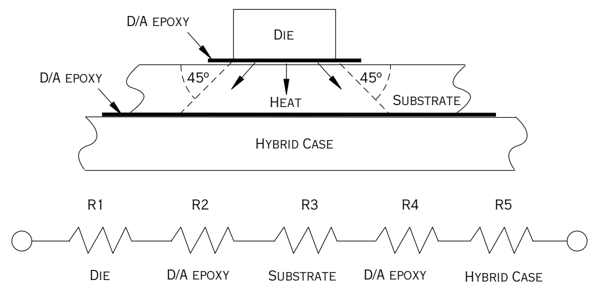
Thermal Characteristics

The heat transfer model in a hybrid package is described in figure 1 (Based on single ASIC design) .

Heat spreading occurs when heat flows into a material layer of increased cross-sectional area. It is adequate to assume that spreading occurs at a 45° angle.

The total thermal resistance is calculated by summing the thermal resistances of each material in the thermal path between the device and hybrid case.

$$RT = R1 + R2 + R3 + R4 + R5$$



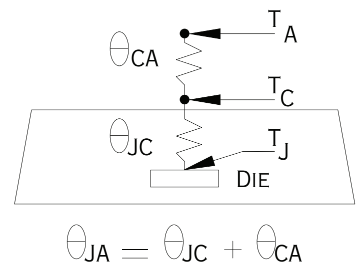
(Figure 1)

The total thermal resistance RT (see figure 2) between the heat source (die) to the hybrid case is the Theta Junction to Case (Theta JC) in°C/W.

- Theta junction to case (Theta JC) for this product is 24°C/W.
- Theta case to ambient (Theta CA) for this part is 105°C/W.
- Theta Junction to ambient (Theta JA) is 130°C/W.

Maximum power dissipation PD for this package at 25°C is:

- PD(max) = (TJ (max) – TA)/Theta JA
- With TJ = 175°C (Maximum junction temperature of die)
- PD(max) = (175 – 25)/130 = 1.15W



(Figure 2)

Environmental Specifications

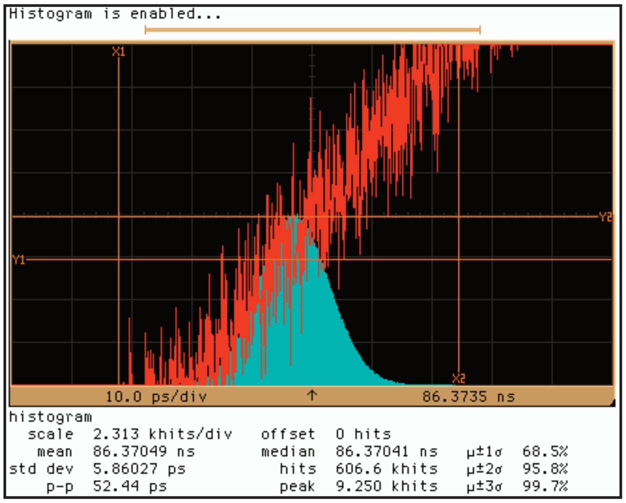
Q-Tech Standard Screening/QCI (MIL-PRF55310) is available for all of our DIP packages. Q-Tech can also customize screening and test procedures to meet your specific requirements. The DIP packages are designed and processed to exceed the following test conditions:

Environmental Test	Test Conditions
Temperature cycling	MIL-STD-883, Method 1010, Cond. B
Constant acceleration	MIL-STD-883, Method 2001, Cond. A, Y1
Seal Fine Leak	MIL-STD-883, Method 1014, Cond. A
Burn-in	160 hours, 125°C with load
Aging	30 days, 70°C, ± 0.7ppm max
Vibration sinusoidal	MIL-STD-202, Method 204, Cond. D
Shock, non operating	MIL-STD-202, Method 213, Cond. I
Thermal shock, non operating	MIL-STD-202, Method 107, Cond. B
Ambient pressure, non operating	MIL-STD-202, 105, Cond. C, 5 minutes dwell time minimum
Resistance to solder heat	MIL-STD-202, Method 210, Cond. C
Moisture resistance	MIL-STD-202, Method 106
Terminal strength	MIL-STD-202, Method 211, Cond. C
Resistance to solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-202, Method 208

Please contact Q-Tech for higher shock requirements

Period Jitter

As data rates increase, effects of jitter become critical with its budgets tighter. Jitter is the deviation of a timing event of a signal from its ideal position. Jitter is complex and is composed of both random and deterministic jitter components. Random jitter (RJ) is theoretically unbounded and Gaussian in distribution. Deterministic jitter (DJ) is bounded and does not follow any predictable distribution. DJ is also referred to as systematic jitter. A technique to measure period jitter (RMS) one standard deviation (1σ) and peak-to-peak jitter in time domain is to use a high sampling rate (>8G samples/s) digitizing oscilloscope. Figure shows an example of peak-to-peak jitter and RMS jitter (1σ) of a QT6AC8-24MHz, at 5.0Vdc.



RMS jitter (1σ): 5.86ps Peak-to-peak jitter: 52.4ps

Phase Noise and Phase Jitter Integration

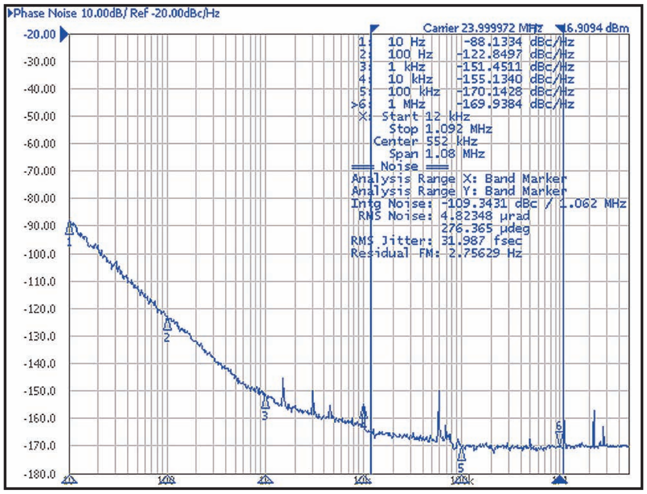
Phase noise is measured in the frequency domain, and is expressed as a ratio of signal power to noise power measured in a 1Hz bandwidth at an offset frequency from the carrier, e.g. 10Hz, 100Hz, 1kHz, 10kHz, 100kHz, etc. Phase noise measurement is made with an Agilent E5052A Signal Source Analyzer (SSA) with built-in outstanding low-noise DC power supply source. The DC source is floated from the ground and isolated from external noise to ensure accuracy and repeatability.

In order to determine the total noise power over a certain frequency range (bandwidth), the time domain must be analyzed in the frequency domain, and then reconstructed in the time domain into an rms value with the unwanted frequencies excluded. This may be done by converting L(f) back to Sφ(f) over the bandwidth of interest, integrating and performing some calculations.

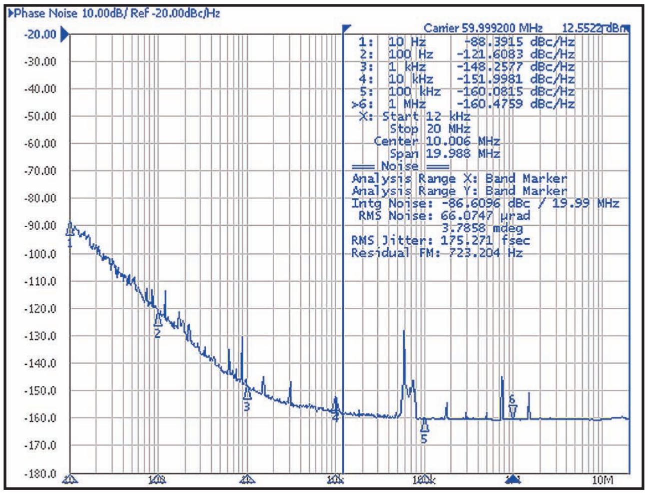
Symbol	Definition
$\int\mathcal{L}(f)$	Integrated single side band phase noise (dBc)
$S\varphi(f)=(180/\Pi)\times\sqrt{2\int\mathcal{L}(f)df}$	Spectral density of phase modulation, also known as RMS phase error (in degrees)
RMS jitter = Sφ (f)/(fosc.360°)	Jitter(in seconds) due to phase noise. Note Sφ (f) in degrees.

The value of RMS jitter over the bandwidth of interest, e.g. 10kHz to 20MHz, 10Hz to 20MHz, represents 1 standard deviation of phase jitter contributed by the noise in that defined bandwidth.

Figure below shows a typical Phase Noise/Phase jitter of a QT6AC8, 5.0Vdc, 24MHz and a QT50T, 5.0Vdc, 60 MHz clock at offset frequencies 10Hz to 5MHz, and phase jitter integrated over the bandwidth of 12kHz to 1MHz.



QT6AC8, 5.0Vdc, 24MHz



QT50T, 5.0Vdc, 60 MHz