

74LS259 Latch

8-Bit Addressable Latch
Product Specification

Logic Products

FEATURES

- Combines demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common Clear input
- Useful as a 1-of-8 active HIGH decoder

DESCRIPTION

The '259 addressable latch has four distinct modes of operation that are selectable by controlling the Clear and Enable inputs (see Function Table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS259	19ns	22mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS259N
Plastic SO-16	N74LS259D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
All	Inputs	1LSul
All	Outputs	10LSul

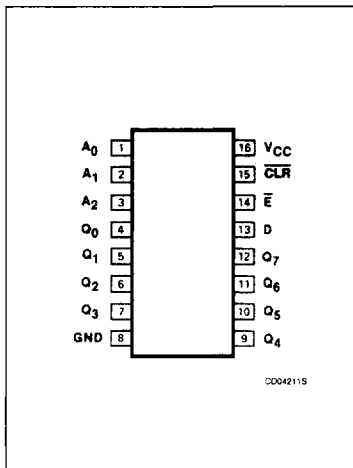
NOTE:

A 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

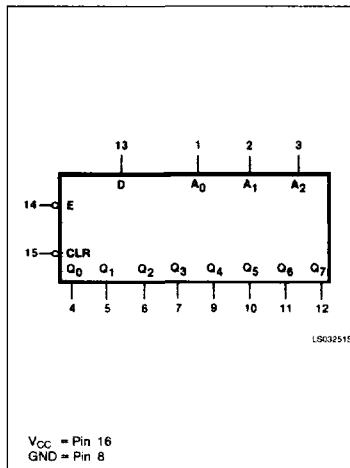
latches, the enable should be held HIGH (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode ($\overline{CLR} = \overline{E} = \text{LOW}$), addressed outputs will follow the level of

the D inputs, with all other outputs LOW. In the clear mode, all outputs are LOW and unaffected by the Address and Data inputs.

PIN CONFIGURATION

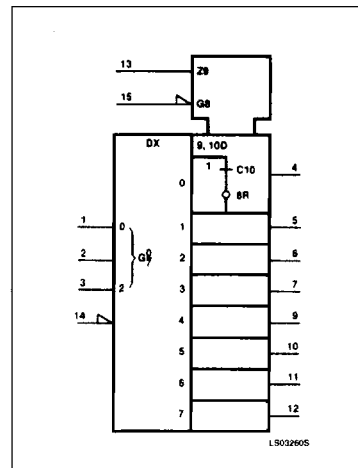


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

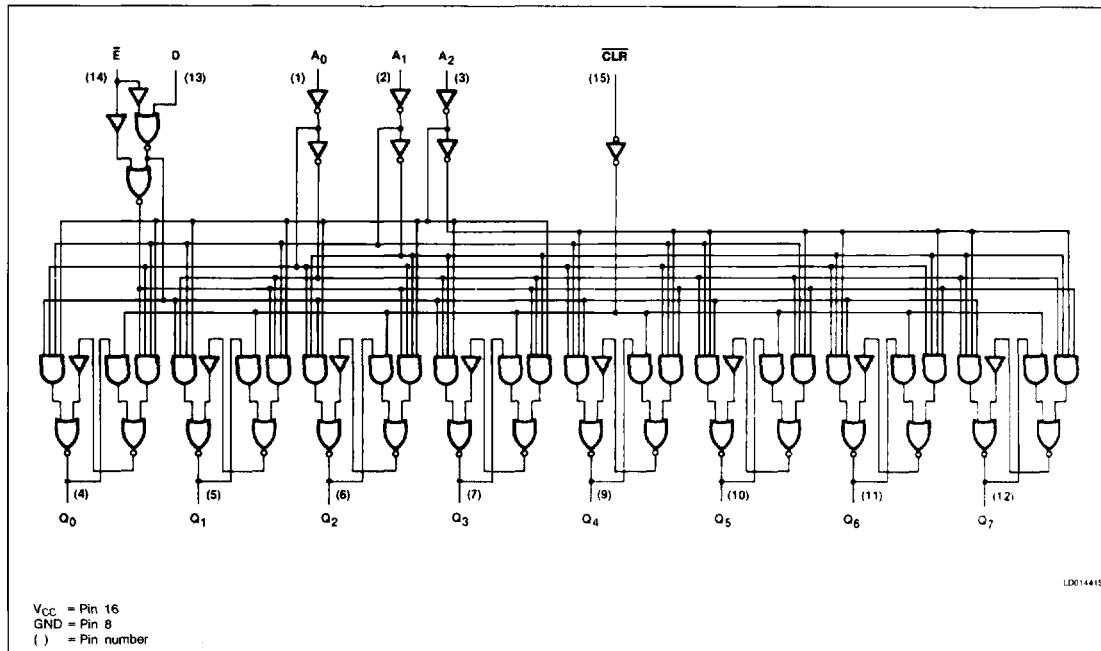
LOGIC SYMBOL (IEEE/IEC)



Latch

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LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS							
	CLR	E	D	A ₀	A ₁	A ₂	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇
Clear	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplex (active HIGH decoder when D = H)	L	L	d	L	L	L	Q = d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q = d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q = d	L	L	L	L	L
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q = d
Store (do nothing)	H	H	X	X	X	X	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
Addressable latch	H	L	d	L	L	L	Q = d	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	H	L	L	q ₀	Q = d	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	L	H	L	q ₀	q ₁	Q = d	q ₃	q ₄	q ₅	q ₆	q ₇
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	H	L	d	H	H	H	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	Q = d

H = HIGH voltage level steady state.

L = LOW voltage level steady state.

X = Don't care.

d = HIGH or LOW data one set-up time prior to the LOW-to-HIGH Enable transition.

q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

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ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			UNIT	
	Min	Nom	Max		
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IH}	Input clamp current			-18	mA
I_{OH}	HIGH-level output current			-400	μA
I_{OL}	LOW-level output current			8	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS259			UNIT	
		Min	Typ ²	Max		
V_{OH}	HIGH-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}$	2.7	3.4		V
V_{OL}	LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$		0.35	0.5	V
			$I_{OL} = \text{MAX}$		0.25	0.4
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_i = I_{IK}$			-1.5	V
I_i	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_i = 7.0V$			0.1	mA
I_{IH}	HIGH-level input current	$V_{CC} = \text{MAX}, V_i = 2.7V$			20	μA
I_{IL}	LOW-level input current	$V_{CC} = \text{MAX}, V_i = 0.4V$			-0.4	mA
I_{OS}	Short-circuit output current ³	$V_{CC} = \text{MAX}$	-20		-100	mA
I_{CC}	Supply current ⁴ (total)	$V_{CC} = \text{MAX}$		22	36	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5V, T_A = 25^\circ\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5V$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5V$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with the inputs grounded and the outputs open.

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AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		UNIT
		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
		Min	Max	
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1	35 24	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 2	32 21	ns
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 3	38 29	ns
t_{PHL}	Propagation delay, clear to output	Waveform 4	27	ns

AC SET-UP REQUIREMENTS

PARAMETER	TEST CONDITIONS	74LS		UNIT
		Min	Max	
t_W	Enable pulse width	Waveform 1	15	ns
t_W	Clear pulse width	Waveform 4	15	ns
$t_s(H)$	Set-up time HIGH, data to enable	Waveform 5	15	ns
$t_h(H)$	Hold time HIGH, data to enable	Waveform 5	5	ns
$t_s(L)$	Set-up time LOW, data to enable	Waveform 5	15	ns
$t_h(L)$	Hold time LOW, data to enable	Waveform 5	5	ns
t_s	Set-up time, address to enable ^(a)	Waveform 6	15	ns
t_h	Hold time, address to enable ^(b)	Waveform 6	15	ns

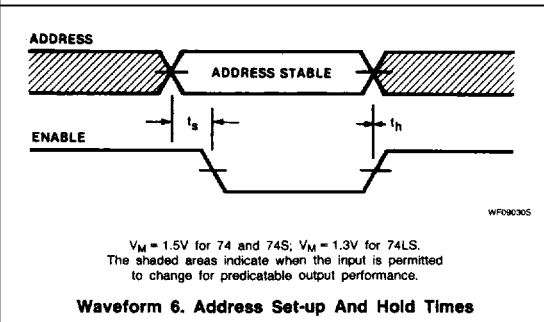
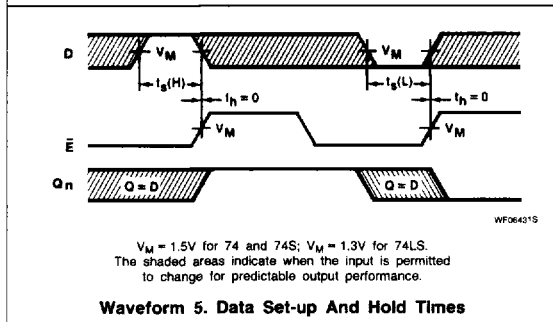
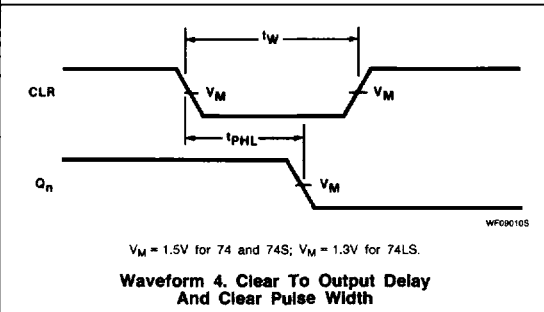
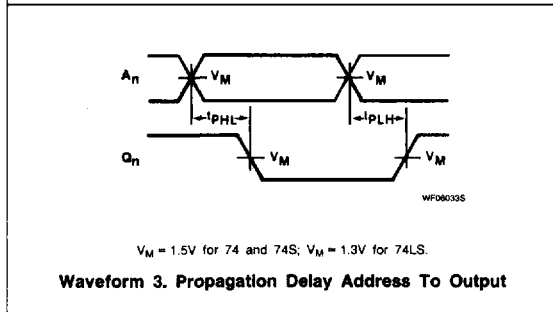
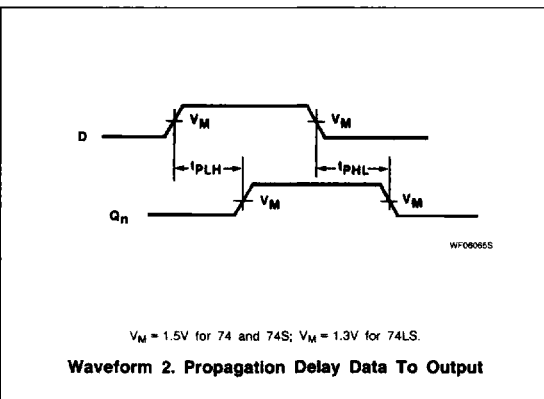
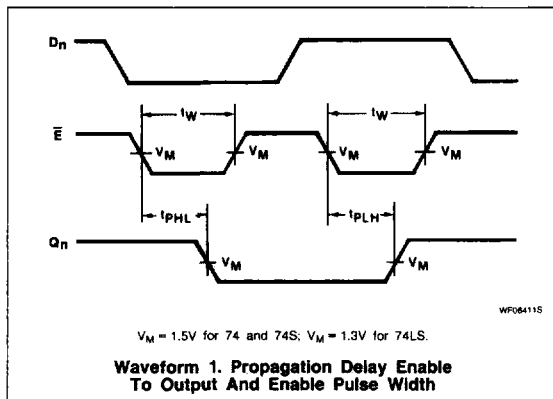
NOTES:

- The Address to Enable set-up time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
- The Address to Enable hold time is the time after the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

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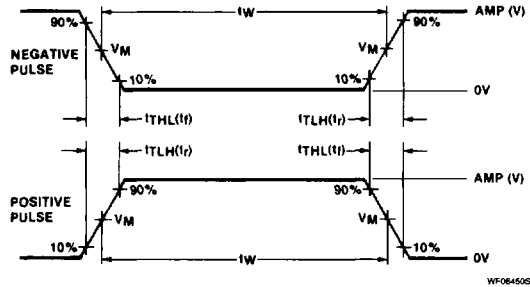
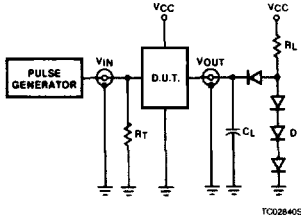
AC WAVEFORMS



Latch

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TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

