T-79-15

TELEDYNE COMPONENTS

1438

OPERATIONAL AMPLIFIER — WIDEBAND, FAST-SETTLING

FEATURES

- Gain-Bandwidth Product .....350 MHz
- Unity Gain Bandwidth .....40 MHz
- Settling Time to 0.1% (10V step).....85 ns
- Output .....±12V, ±60 mA
- Small, TO-8 Package
- Single External Compensation Capacitor
- FET Input

APPLICATIONS

- Current-to-Voltage DACs
- Pulse Amplifiers
- Radar and Sonar Signal Processing
- Graphics CRT Displays
- Video ADCs, DACs, and S/Hs

GENERAL DESCRIPTION

The 1438 hybrid operational amplifier offers versatility in wideband steady-state and fast-transient applications. The 1438 stands out for speed and predictability, as exemplified by its fast, smooth settling. The absence of large transients and oscillations in the settling waveform make it a dependable system element that can resolve settling problems associated with ADCs, DACs, and sampling circuits.

The 1438 has excellent DC characteristics: ±200 pA input bias current, 93 dB open-loop gain, and ±0.5 mV input offset voltage. The choice of a single external compensation capacitor is all that is needed to ensure a 40 MHz bandwidth at a variety of gains. True differential inputs ensure superior performance in all circuit configurations, whether inverting, noninverting, or differential. With an attractive price/performance ratio, the 1438 is an industry standard for high-speed, high-accuracy signal processing and data acquisition.

The 1438 is packaged in a 12-pin TO-8 can and is specified for 0°C to +70°C operation. The High Reliability (-HR) version is specified for –55°C to +125°C operation.

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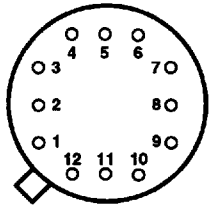
PIN CONFIGURATION

PIN NO.	DESIGNATION	PIN NO.	DESIGNATION
1	NC	12	NC
2	OFFSET TRIM	11	COMPENSATION
3	INVERTING INPUT	10	$+V_{CC}$
4	NONINVERTING INPUT	9	OUTPUT
5	$-V_{CC}$	8	OFFSET TRIM
6	NC	7	NC

NC = NO INTERNAL CONNECTION



BOTTOM VIEW

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WIDEBAND, FAST-SETTLING OPERATIONAL AMPLIFIER

1438

ABSOLUTE MAXIMUM RATINGS

V_{CC} Supply Voltage ..... ±20V
V_{ID} Differential Input Voltage ..... ±25V
V_{ICM} Common-Mode Input Voltage ..... $\pm V_{CC}$
T_C Operating Temperature Range (Case)
1438 ..... 0°C to +70°C
1438-HR ..... –55°C to +125°C
T_{STG} Storage Temperature Range ..... –65°C to +150°C
θ_{JC} Overall Junction-to-Case Thermal Resistance (Note 1) ..... 19°C/W
θ_{JC} Output Transistor Junction-to-Case Thermal Resistance (Note 2) ..... 35°C/W

NOTES: 1. Overall thermal resistance during normal operating conditions. Multiply this value by the power dissipation of the entire 1438 to determine maximum temperature rise case to junction in the hybrid.
2. Individual thermal resistance of the output stage. The 1438 is a Class AB amplifier. To calculate the output transistor temperature rise case to junction, multiply this figure by the power dissipation of the output transistor. At AC frequencies above 100 Hz, the effective thermal resistance of the output stage will drop 32.5°C/W for the 1438.

DC CHARACTERISTICS: (Note 1) V_{CC} = ±15V, R_L = 200Ω, T_C = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	1438 Min	1438 Typ	1438 Max	1438-HR Min	1438-HR Typ	1438-HR Max	Unit
V_{OS}	Input Offset Voltage		—	±0.5	±2	—	±0.5	±2	mV
V_{OS} TC	Input Offset Voltage Drift vs Temperature	Average, T_{MIN} to T_{MAX}	—	±15	—	—	±15	±50	µV/°C
I_B	Input Bias Current		—	±200	—	—	±200	—	pA
I_B TC	Input Bias Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	Doubles every 11°C			Doubles every 11°C			—
I_{OS}	Input Offset Current		—	±20	—	—	±20	—	pA
I_{OS} TC	Input Offset Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	Doubles every 11°C			Doubles every 11°C			—
A_{VOL}	Open-Loop Voltage Gain		86	93	—	86	93	—	dB
PSRR	Power Supply Rejection Ratio		—	76	—	—	76	—	dB
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±8V	60	78	—	60	78	—	dB
CMR	Common-Mode Range (DC Linear Operation)	CMRR ≥ 54 dB	±10	±12	—	±10	±12	—	V
Z_{ID}	Differential Input Impedance		—	10^{11}||3	—	—	10^{11}||3	—	Ω||pF
Z_{ICM}	Common-Mode Input Impedance		—	10^{11}||3	—	—	10^{11}||3	—	Ω||pF
V_O	Output Voltage Swing		±10	±12	—	±10	±12	—	V
I_O	Output Current		±50	±60	—	±50	±60	—	mA
I_{SC}	Output Short-Circuit Current		—	±125	—	—	±125	—	mA
R_O	Output Resistance (DC Open-Loop)		—	90	—	—	90	—	Ω
V_{CC}	Supply Voltage Range (Operating)		±12	±15	±20	±12	±15	±20	V
I_{CC}	Quiescent Supply Current		—	±12	±15	—	±12	±15	mA

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

AC CHARACTERISTICS: (Note 1) V_{CC} = ±15V, R_L = 200Ω, C_C = 0 pF, T_C = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	1438 Min	1438 Typ	1438 Max	1438-HR Min	1438-HR Typ	1438-HR Max	Unit
S_R	Slew Rate		—	400	—	—	400	—	V/µs
		C_C =15 pF	—	225	—	—	225	—	V/µs
GBWP	Gain-Bandwidth Product	f = 10 MHz	—	350	—	—	350	—	MHz
UGBW	Unity-Gain Bandwidth	C_C = 27 pF	—	40	—	—	40	—	MHz
t_s	Settling Time (A_{CL} = -1, C_C = 15 pF)	10V step/1%	—	65	—	—	65	—	ns
		10V step/0.1%	—	85	120	—	85	120	ns
		10V step/0.025%	—	150	—	—	150	—	ns
		10V step/0.01%	—	180	—	—	180	—	ns
e_n	Input Voltage Noise Density	f = 1 kHz	—	10	—	—	10	—	nV/√Hz

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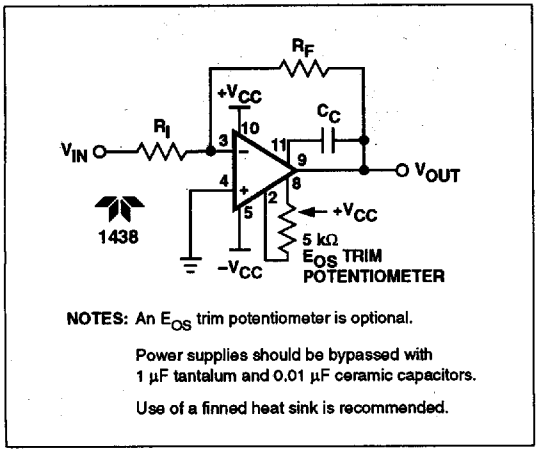
APPLICATIONS

Basic connections for the 1438 in the normal inverting mode are shown in Figure 1.



NOTES: An E_{OS} trim potentiometer is optional.

Power supplies should be bypassed with 1 µF tantalum and 0.01 µF ceramic capacitors.

Use of a finned heat sink is recommended.

Figure 1. Normal Inverting Operation

Data Conversion

Fast settling time, low bias and offset currents, and modest power consumption make the 1438 an excellent choice for use in data conversion applications. Figure 2 illustrates the 1438 as a fast-settling input buffer to a 12-bit A/D converter.

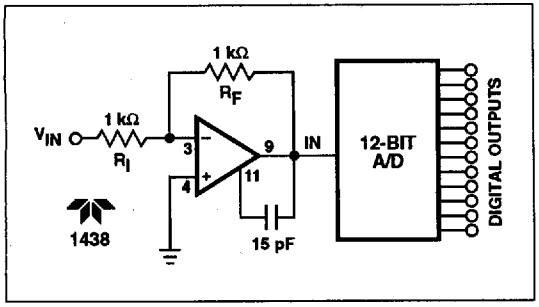


Figure 2. Fast-Settling Buffer

Figure 3 demonstrates the 1438 used as a current-to-voltage converter for a 12-bit DAC.

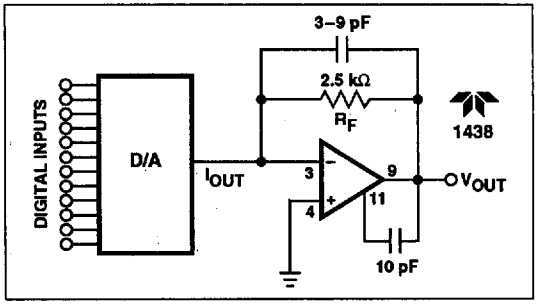


Figure 3. Current-to-Voltage Converter

Stability and Compensation

For wide bandwidth applications, the 1438 can achieve 30 MHz bandwidth at 20 dB gain with a 2 pF compensation capacitor, as shown in Figure 4. The 1438 can operate as a unity-gain buffer out to 40 MHz bandwidth with 27 pF compensation (Figure 5). The 1438 is stable without a compensation capacitor in applications with gains greater than 30 dB, such as a video amplifier (Figure 6), where the gain is 70 dB and a compensation capacitor is not needed. Refer to Figure 8 to determine the required compensation for other gain selections.

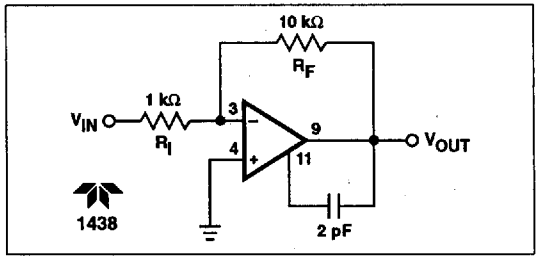


Figure 4. Inverting Gain of 10

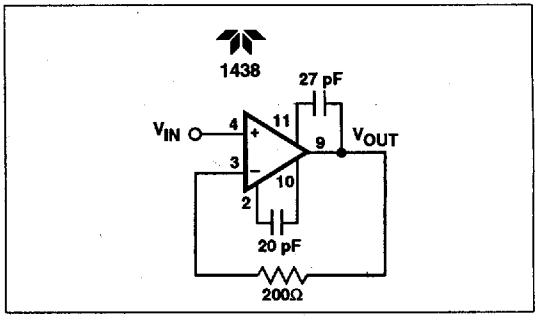


Figure 5. 40 MHz Unity-Gain Buffer

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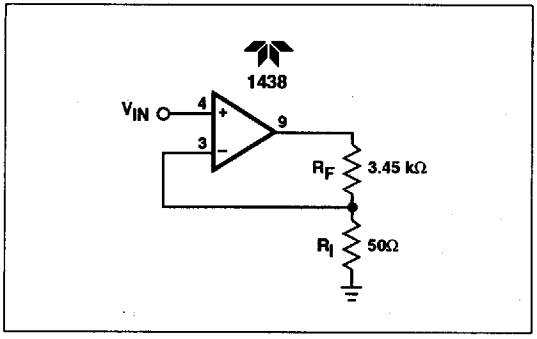


Figure 6. Video Amplifier

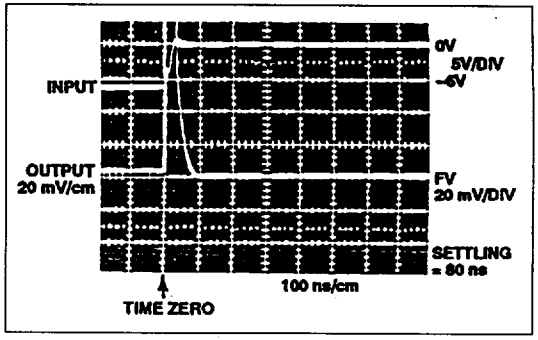
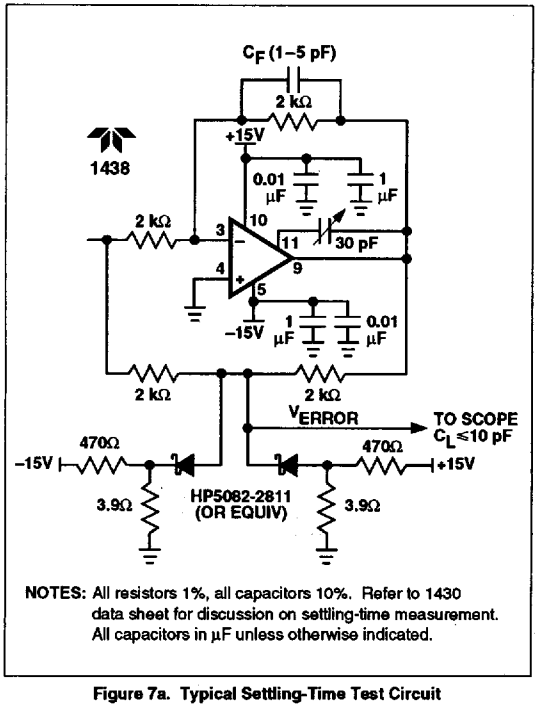


Figure 7b. Settling-Time Graph

Settling-Time Measurements

A typical settling-time measurement circuit for the 1438 is shown in Figure 7a; a photograph of a typical measurement is shown in Figure 7b. Figure 11 presents a graph of settling time to either 100 mV or 10 mV versus the output step size.



NOTES: All resistors 1%, all capacitors 10%. Refer to 1430 data sheet for discussion on settling-time measurement. All capacitors in µF unless otherwise indicated.

Figure 7a. Typical Settling-Time Test Circuit

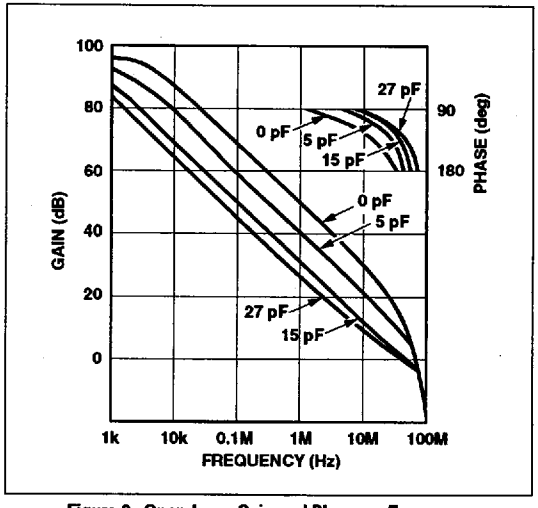


Figure 8. Open-Loop Gain and Phase vs Frequency

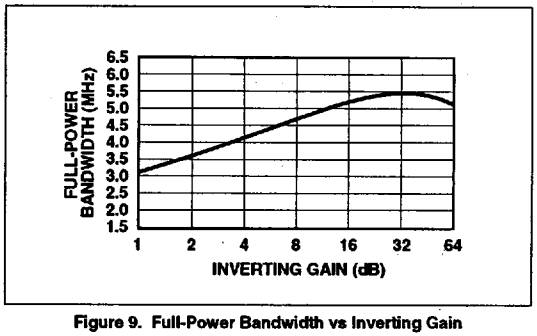


Figure 9. Full-Power Bandwidth vs Inverting Gain

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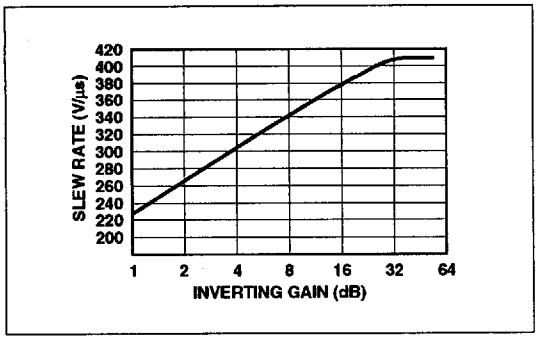

Figure 10. Slew Rate vs Inverting Gain

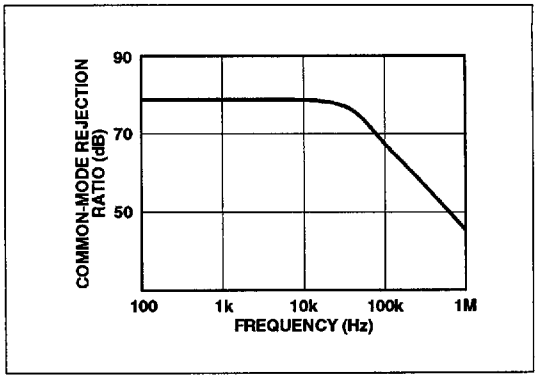

Figure 13. CMRR vs Frequency

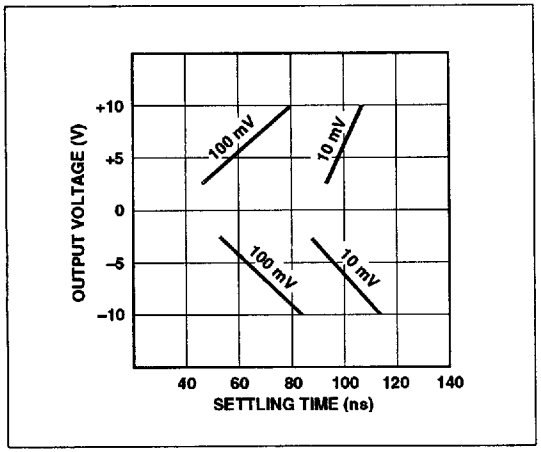

Figure 11. Settling Time vs Output Voltage Change

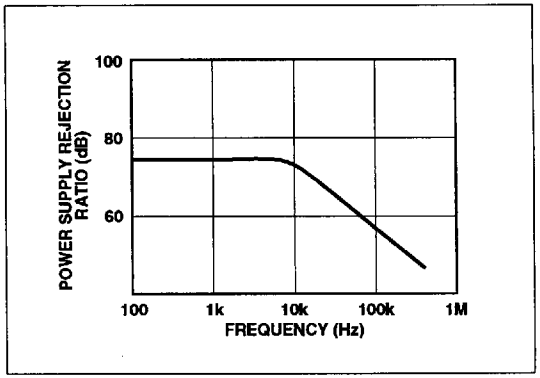

Figure 14. PSRR vs Frequency

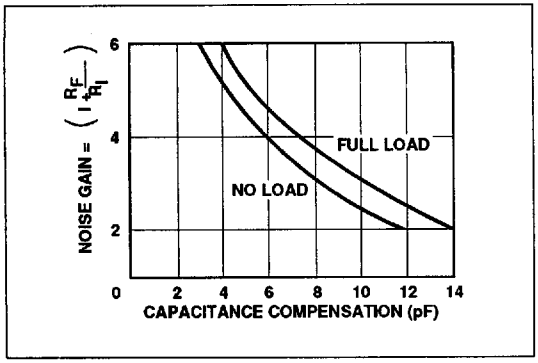

Figure 12. Noise Gain vs C_C for 16% Overshoot

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