MITEL
Technical Data

ISO-CMOS
Octal Decoders/Demultiplexers

MD54SC137, MD54SC138, MD54SC139
MD54SC237, MD54SC238, MD54SC239
MD74SC137, MD74SC138, MD74SC139
MD74SC237, MD74SC238, MD74SC239

OCT '82

Features

- Equivalent to 54/74LS' series
- Low power ISO-CMOS technology
- Short propagation delay
- Improved noise margins
- High current, sink/source capability

Ordering Information

MD54SCXXXAC	16 Pin, Cerdip
MD74SCXXXAC	16 Pin, Cerdip
MD74SCXXXAE	16 Pin, Plastic DIP

Description

This family of ISO-CMOS, MSI circuits is designed for use in high speed memory and peripheral, address decoding systems. MD54/74SC138 and MD54/74SC238, decode 3 binary inputs (A_0, A_1, A_2) to select one of eight mutually exclusive outputs (0_0 - 0_7). Three enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3), reduce the need for external gates in an expanded system. MD54/74SC137 and MD54/74SC237 feature additional latches on A_0, A_1 and A_2 for use in glitch free applications. When Latch Enable (LE) is LOW the device acts as MD54/74SC138. When LE is HIGH the address present at A_0 to A_2 is stored. A 1 to 32 decoder requires only four of these devices and one inverter. MD54/74SC139 and MD54/74SC239 feature two individual, two line (A_0-A_1) to four line (0_0-0_3) decoders.

Device Selection

Product	Format	Output
MD54/74SC137	1 of 8, latched address	inverted
MD54/74SC138	1 of 8	inverted
MD54/74SC139	Dual 1 of 4	inverted
MD54/74SC237	1 of 8, latched address	non-inverted
MD54/74SC238	1 of 8	non-inverted
MD54/74SC239	Dual 1 of 4	non-inverted

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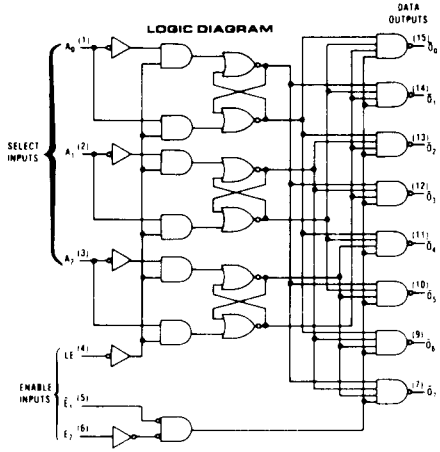
Functional Block Diagrams and Logic

Fig. 1 MD54/74SC137

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
LE	E_2	$\bar{E}_1$	A_2	A_1	A_0	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$	$\bar{O}_4$	$\bar{O}_5$	$\bar{O}_6$	$\bar{O}_7$
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address. L all others H							

H = high level, L = low level, X = irrelevent

CONNECTION DIAGRAM
DIP (TOP VIEW)

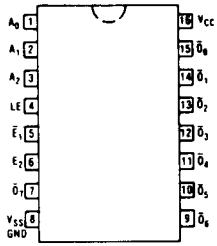
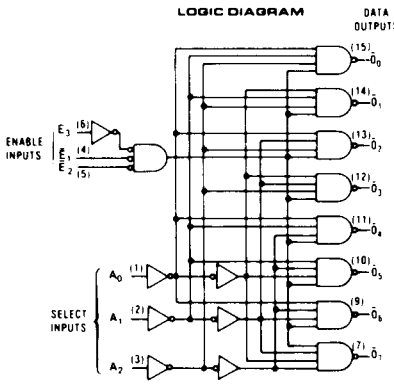


Fig. 2 MD54/74SC138

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS							
ENABLE		SELECT									
E_3	$\bar{E}_1 + \bar{E}_2$	A_2	A_1	A_0	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$	$\bar{O}_4$	$\bar{O}_5$	$\bar{O}_6$	$\bar{O}_7$
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

H = high level, L = low level, X = irrelevent

CONNECTION DIAGRAM
DIP (TOP VIEW)

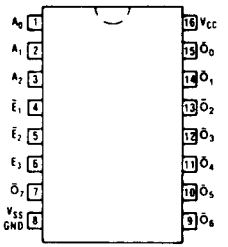
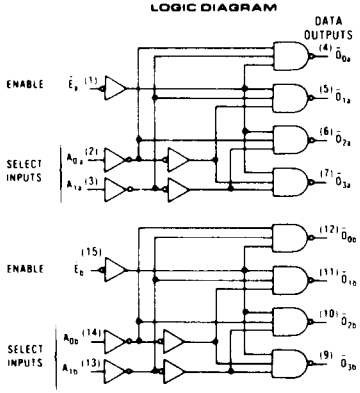


Fig. 3 MD54/74SC139

LOGIC DIAGRAM

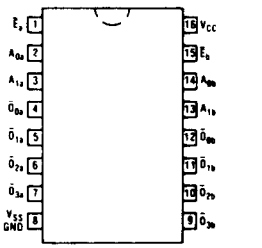


(EACH DECODER/DEMULTIPLEXER)
FUNCTION TABLE

INPUTS		OUTPUTS				
ENABLE	SELECT					
$\bar{E}$	A_1	A_0	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = irrelevent

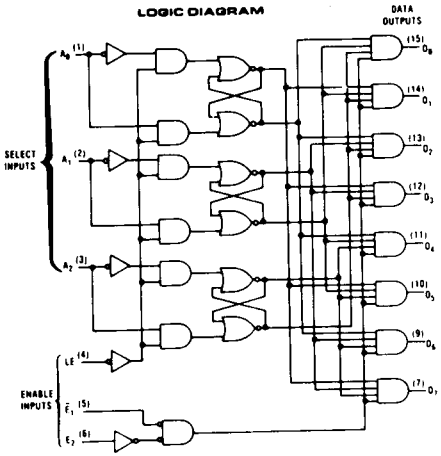
CONNECTION DIAGRAM
DIP (TOP VIEW)



Functional Block Diagrams and Logic

Fig. 4 MD54/74SC237

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS
ENABLE		SELECT		
LE	$\bar{E}_2$	$\bar{E}_1$	A_2 A_1 A_0	O_0 O_1 O_2 O_3 O_4 O_5 O_6 O_7
X	X	H	X X X	L L L L L L L L
X	L	X	X X X	L L L L L L L L
L	H	L	L L L	H L L L L L L L
L	H	L	L L H	L H L L L L L L
L	H	L	L H L	L L H L L L L L
L	H	L	L H H	L L L H L L L L
L	H	L	H L L	L L L L H L L L
L	H	L	H L H	L L L L L H L L
L	H	L	H H L	L L L L L L H L
L	H	L	H H H	L L L L L L L H
H	H	L	X X X	Output corresponding to stored address H, all others L

H = high level, L = low level, X = irrelevent

CONNECTION DIAGRAM DIP (TOP VIEW)

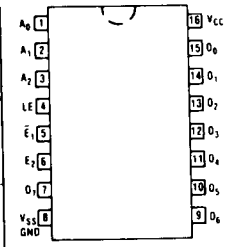
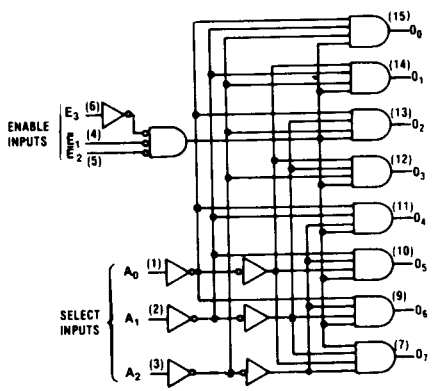


Fig. 5 MD54/74SC238

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS
ENABLE		SELECT		
E_3	$\bar{E}_{1,2}$	A_2	A_1 A_0	O_0 O_1 O_2 O_3 O_4 O_5 O_6 O_7
X	H	X	X X	L L L L L L L L
L	X	X	X X	L L L L L L L L
H	L	L	L L	H L L L L L L L
H	L	L	L H	L H L L L L L L
H	L	L	H L	L L H L L L L L
H	L	L	H H	L L L H L L L L
H	L	H	L L	L L L L H L L L
H	L	H	L H	L L L L L H L L
H	L	H	H L	L L L L L L H L
H	L	H	H H	L L L L L L L H

H = high level, L = low level, X = irrelevent

CONNECTION DIAGRAM DIP (TOP VIEW)

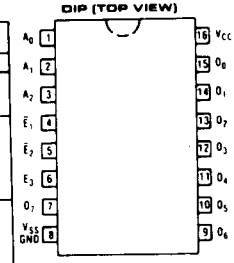
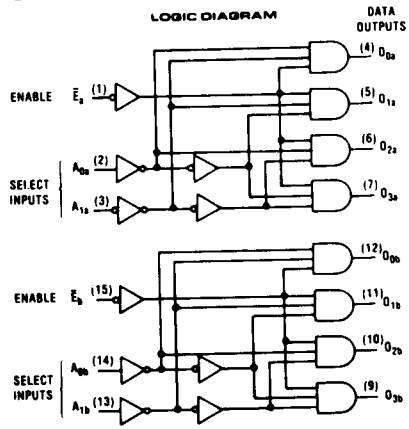


Fig. 6 MD54/74SC239

LOGIC DIAGRAM

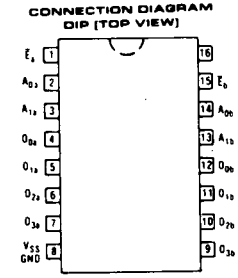


(EACH DECODER/DEMULTIPLEXER) FUNCTION TABLE

INPUTS		OUTPUTS
ENABLE	SELECT	
$\bar{E}$	A_1 A_0	O_0 O_1 O_2 O_3
H	X X	L L L L
L	L L	H L L L
L	L H	L H L L
L	H L	L L H L
L	H H	L L L H

H = high level, L = low level, X = irrelevent

CONNECTION DIAGRAM DIP (TOP VIEW)



Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	
		MD74'	MD54'
Supply voltage	V_{CC}	−0.5V to 7.0V	−0.5V to 7.0V
Input voltage	V_I	−0.3V to Vcc + 0.3V	−0.3V to V_{CC} + 0.3V
Output current, per output	I_O	± 75mA	± 75 mA
Operating temperature	T_A	−40°C to +85°C	−55°C to + 125°C
Storage temperature	T_S	−65°C to + 150°C	−65°C to + 150°C
Package Power dissipation	P	450mW	450 mW

Note: 1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Supply voltage		V_{CC}	2	5	6.5	V
Input voltage		V_I	0		V_{CC}	V
Operating free-air temperature	MD74'	T_A	0		70	°C
	MD54'	T_A	−55		125	°C

1 Voltage values are with respect to V_{SS}/GND

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range

PARAMETER	SYMBOL		MIN	TYP	MAX	UNIT	TEST CONDITIONS
High level input voltage	V_{IH}	MD54'	2			V	V_{CC} = 5.5V
		MD74'	2			V	V_{CC} = 5.25V
Low level input voltage	V_{IL}	MD54'			0.8	V	V_{CC} = 4.5V
		MD74'			0.8	V	V_{CC} = 4.75V
High level output voltage	V_{OH}	MD54'	2.4 3.5			V	V_{CC} = 4.5V, I_{OH} = −5mA, I_{OH} = −3mA
		MD74'	2.4 4.0			V	V_{CC} = 4.75V, I_{OH} = −14mA I_{OH} = −3mA
Low level output voltage	V_{OL}	MD54'			0.4	V	V_{CC} = 4.5V, I_{OL} = 6.5mA
		MD74'			0.4	V	V_{CC} = 4.75V, I_{OL} = 8 mA
Input current at maximum input voltage	I_I	MD54'			15	µA	V_{CC} = 5.5V, V_I = 5.85V
		MD74'			15	µA	V_{CC} = 5.25V, V_I = 5.55V
High level input current	I_{IH}	MD54'			10	µA	V_{CC} = 5.5V, V_I = 2.7V
		MD74'			10	µA	V_{CC} = 5.25V, V_I = 2.7V
Low level input current	I_{IL}	MD54'			−10	µA	V_{CC} = 5.5V, V_I = 0.4V
		MD74'			−10	µA	V_{CC} = 5.25V, V_I = 0.4V
Short circuit output current	I_{OS}	MD54'		−40		mA	NOTE 2, V_{CC} = 5.5V
		MD74'		−40		mA	NOTE 2, V_{CC} = 5.25V
Quiescent supply current	I_{CC}	MD54'			0.5	mA	V_{CC} = 5.5V, outputs disabled
		MD74'			0.1	mA	V_{CC} = 5.25V, outputs disabled

2 Max. dissipation of 1 ms duration should not be exceeded
3 All TYP values at T_A = 25°C V_{CC} = 5V

Switching Characteristics, V_{CC} = 5V, T_A = 25° C

PARAMETER	SYMBOL	DEVICE	MIN	TYP	MAX	UNIT	TEST CONDITION (Figure 7)
Propagation delay time Address to output	t_{PLH}	MD54/74SC137		25	38	ns	C_L = 15pF R_L = 2K Ω
		MD54/74SC138		22	35		
		MD54/74SC139		29	48		
		MD54/74SC237		30	50		
		MD54/74SC238		24	40		
		MD54/74SC239		25	45		
Propagation delay time Address to output	t_{PHL}	MD54/74SC137		31	52	ns	C_L = 15pF R_L = 2K Ω
		MD54/74SC138		24	42		
		MD54/74SC139		30	50		
		MD54/74SC237		30	44		
		MD54/74SC238		26	42		
		MD54/74SC239		27	45		
Propagation delay time E to output	t_{PLH}	MD54/74SC137		31	44	ns	C_L = 15pF R_L = 2K Ω
		MD54/74SC138		31	44		
		MD54/74SC139		22	35		
		MD54/74SC237		33	45		
		MD54/74SC238		33	45		
		MD54/74SC239		25	45		
Propagation delay time E to output	t_{PHL}	MD54/74SC137		31	48	ns	C_L = 15pF R_L = 2K Ω
		MD54/74SC138		33	48		
		MD54/74SC139		30	53		
		MD54/74SC237		34	52		
		MD54/74SC238		34	52		
		MD54/74SC239		26	35		
Set up time, address to Latch Enable Hold	t_{su}	MD54/74SC137	15			ns	C_L = 15pF R_L = 2K Ω
		MD54/74SC237	15				
Hold time output, from latch Disable	t_h	MD54/74SC137	10			ns	C_L = 15pF R_L = 2K Ω
		MD54/74SC237	10				
Input Capacitance	C_I	MD54/74SC137		3	8	pF	
		MD54/74SC138		3	8		
		MD54/74SC139		3	8		
		MD54/74SC237		3	8		
		MD54/74SC238		3	8		
		MD54/74SC239		3	8		

Voltage Waveforms - Propagation Delay Times

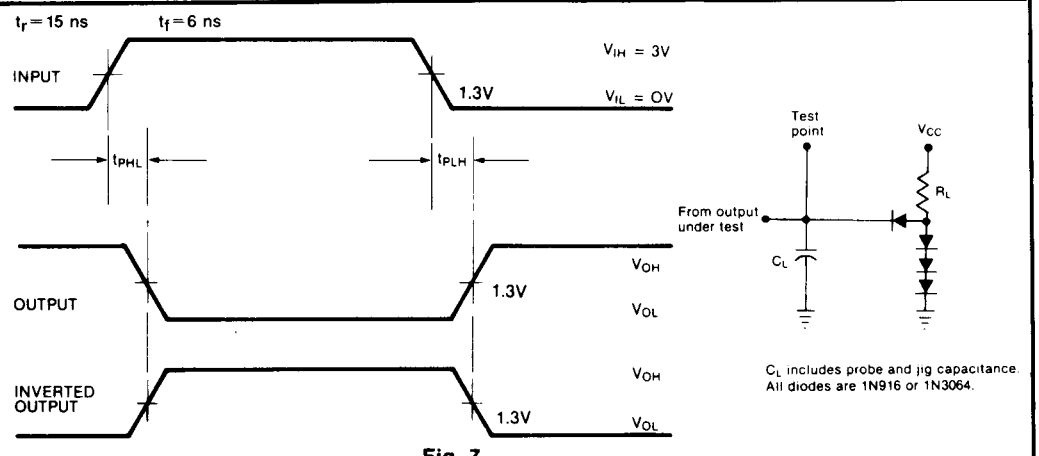


Fig. 7

Pin Function

PIN	DESCRIPTION
A_0, A_1, A_2 or A_{0a}, A_{0b} A_{1a}, A_{1b}	Address Inputs, to be decoded
$\overline{E}_1$, $\overline{E}_2$, E_3 or $\overline{E}_a$, $\overline{E}_b$ or $\overline{E}_1$, E_2	Chip Enable Inputs

PIN	DESCRIPTION
LE	Latch Enable Input
O_0 - O_7 or $\overline{O}_0$ - $\overline{O}_7$	Outputs, to peripherals Inverted Outputs, to peripherals
V_{CC}	Positive Supply Voltage
V_{SS}/GND	System Ground