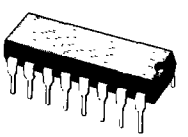
DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

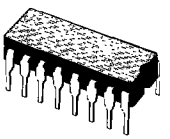
- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- NON INVERTING 3-STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

DESCRIPTION

The LSTTL/MSI T74LS253 is a very high speed Dual 4-Input Multiplexer with 3-state outputs. It can select two bits data from four sources using commun select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable (E_0) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all TTL families.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

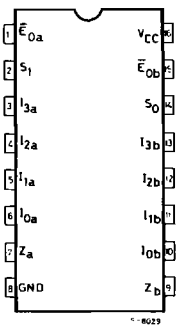
C1
(Plastic Chip Carrier)

ORDER CODES :

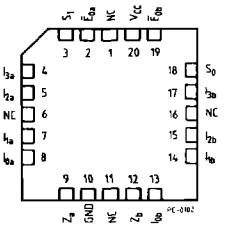
T74LS253 D1
T74LS253 B1
T74LS253 C1
T74LS253 M1

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER

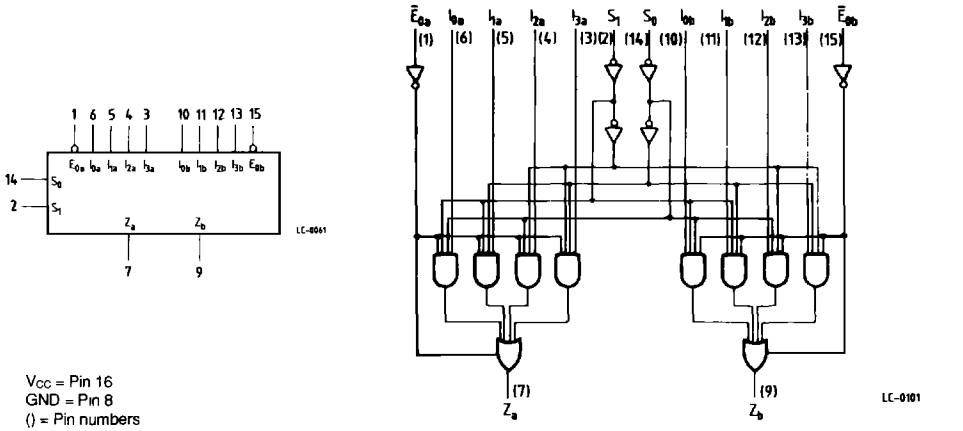


NC = No Internal Connection

PIN NAMES

S_0-S_1	COMMON SELECT INPUT
Multiplexer A	
E_{0a}	OUTPUT ENABLE (active LOW) INPUT
I_{0a}-I_{3a}	MULTIPLEXER INPUTS
Z_a	MULTIPLEXER OUTPUT
Multiplexer B	
E_{0b}	OUTPUT ENABLE (active LOW) INPUT
I_{0b}-I_{3b}	MULTIPLEXER INPUTS
Z_b	MULTIPLEXER OUTPUT

LOGIC SYMBOL AND LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
() = Pin numbers

TRUTH TABLE

Select Inputs		Data Inputs				Output Enable	Output
S_0	S_1	I_0	I_1	I_2	I_3	$\bar{E}_0$	Z
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(Z) = High Impedance (off)
Address inputs S_0 and S_1 are common to both sections.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.6 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS253XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

FUNCTIONAL DESCRIPTION

The LS253 contains two identical 4-Input Multiplexers with 3-state outputs. They select two bits from four sources selected by common select inputs (S0, S1). The 4-input multiplexers have individual Output Enable (E_{0a}, E_{0b}) inputs which when HIGH, forces the outputs to a high impedance (high Z) state.

The LS253 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select Inputs. The logic equations for the outputs are shown below.

$$Z_a = \overline{E}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1$$

$$Z_b = \overline{E}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Outputs Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.4	3.1		V_{CC} = MIN, I_{OH} = - 2.6 mA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{OZH}	Output Off Current HIGH			20	V_{CC} = MAX, V_{OUT} = 2.7 V V_E = 2.0 V		µA
I_{OZL}	Output Off Current LOW			- 20	V_{CC} = MAX, V_{IN} = 0.4 V V_E = 2.0 V		µA
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 30		- 130	V_{CC} = MAX		mA
I_{CC}	Power Supply Current Outputs LOW		7.0	12	V_{CC} = MAX, V_{IN} = 0 V, V_E = 2.0 V		mA
	Outputs Off		8.5	14	V_{CC} = MAX, V_{IN} = 4.5 V, V_E = 2.0 V		

Notes : 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2 Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		17 13	25 20	Fig. 1	C_L = 15 pF	ns
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		30 21	45 32	Fig. 1		ns
t_{PZH}	Output Enable Time to HIGH Level		15	28	Figs. 4, 5	C_L = 15 pF R_L = 2 kΩ	ns
t_{PZL}	Output Enable Time to LOW Level		15	23	Figs. 3, 5		ns
t_{PLZ}	Output Disable Time from LOW Level		18	27	Figs. 3, 5	C_L = 5 pF R_L = 2 kΩ	ns
t_{PHZ}	Output Disable Time from HIGH Level		27	41	Figs. 4, 5		ns

STATE AC WAVEFORMS AND LOAD CIRCUIT

Figure 1.

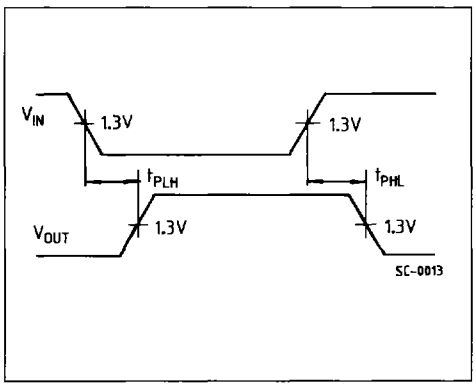


Figure 2.

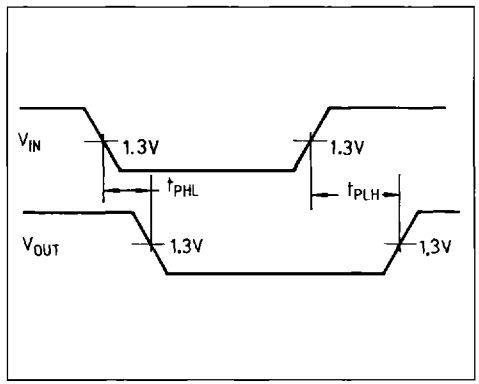


Figure 3.

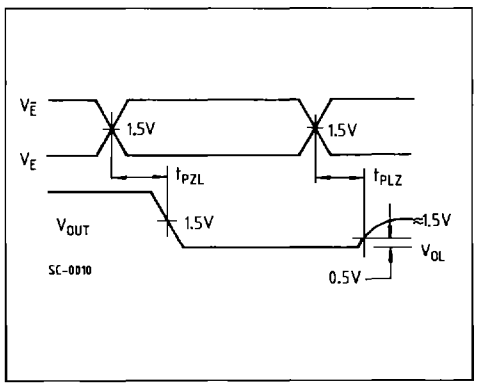


Figure 4.

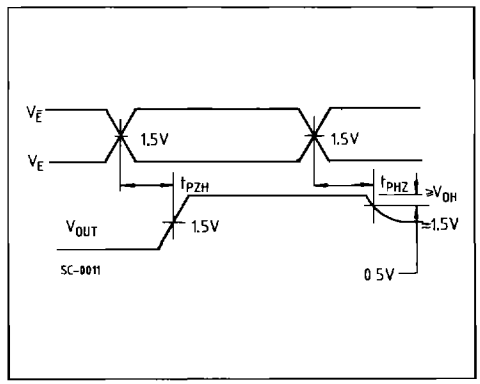
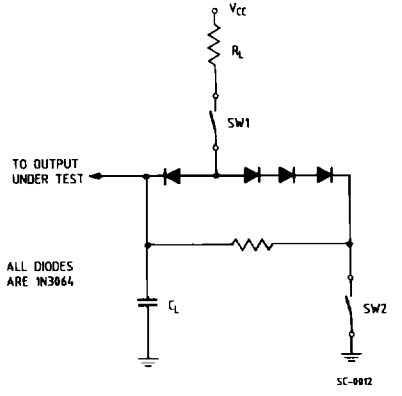


Figure 5.



SWITCHING POSITIONS

Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed