18-bit LVTTL-to-GTL and transceivers | 74GTL16622

FEATURES

- Translates between GTL/GTL + signal levels and LVTTL.
- Supports GTL/GTL + signal operation on B port.
- D-type flip-flops with qualified storage enable.
- Bus-hold data inputs eliminate the need for external pullup or pulldown resistors on A port.
- Flow-through architecture facilitates printed-circuit-board layout
- Low quiescent supply current

DESCRIPTION

These 18-bit registered bus transceivers contain two sets of D-type flip-flops for temporary storage of data flowing in either direction.

The B port operates at GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) and GTL+ (V_{TT} = 1.5 V and V_{REF} = 1 V) levels, while the A port and control inputs are compatible with LVTTL logic levels.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$) and clock(CLKAB and CLKBA) inputs. The clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs are designed to control each 9-bit transceiver independently, which makes the device more versatile.

For A-to-B data flow, the devices operate on the Low-to-High transition of CLKAB if $\overline{CEAB}$ is low. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that for A to B, but uses $\overline{OEBA}$, CLKBA and $\overline{CEBA}$.

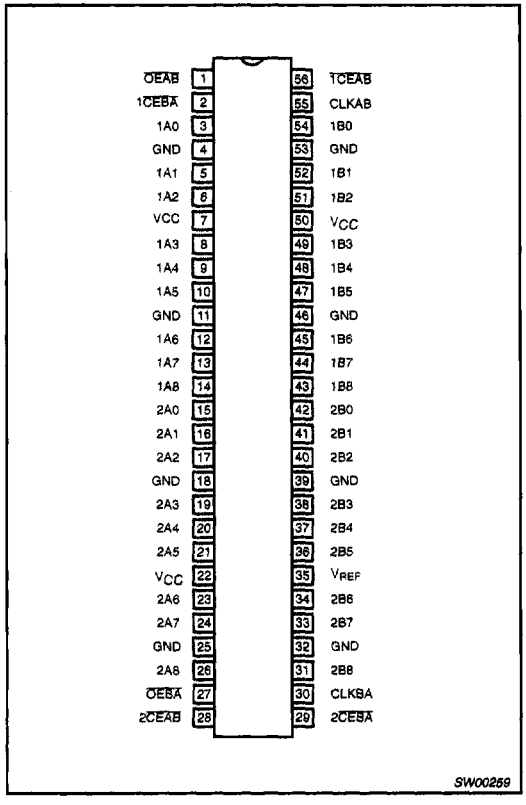
Active bus hold circuitry is provided to hold unused or floating TTL inputs at a valid logic state.

To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by current-sinking capability of the driver.

ORDERING INFORMATION

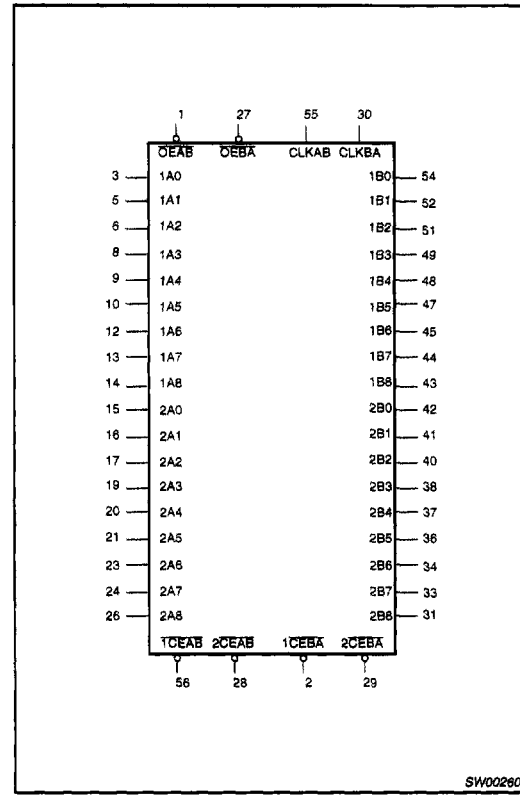
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74GTL16622	GTL16622 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74GTL16622	GTL16622 DGG	SOT364-1

PIN CONFIGURATION



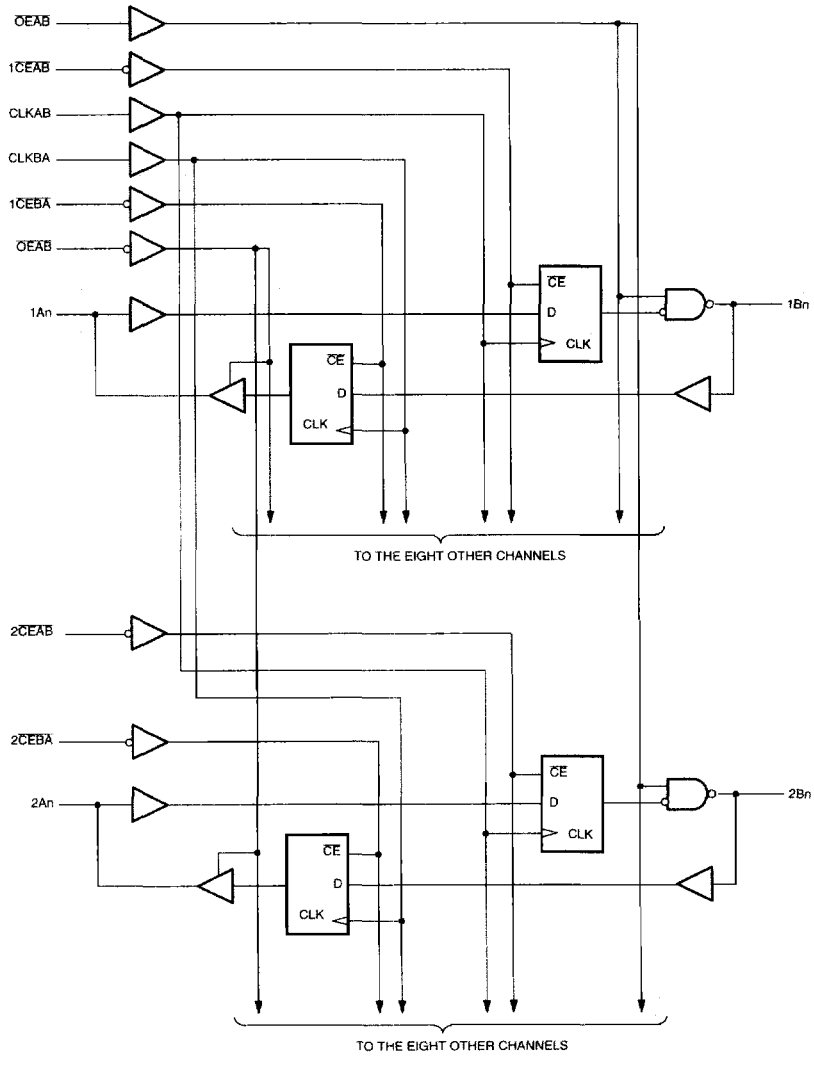
SW00259

LOGIC SYMBOL



SW00260

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUT	MODE
$\overline{CEAB}$	$\overline{OEAB}$	CLKAB	A	B	
X	H	X	X	Z	
H X	L L	X H or L	X X	B_O[2] B_O[2]	Latched storage of A data
L L	L L	↑ ↑	L H	L H	Clocked storage of A data

NOTES:
1. A-to-B data flow is shown: B-to-A data flow is similar but uses $\overline{OEBA}$, CLKBA and $\overline{CEBA}$.
2. Output level before the indicated steady-state input conditions are established.

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low to High

ABSOLUTE MAXIMUM RATINGS [1]

In accordance with the Absolute Maximum Rating System (IEC 134). See Note 1; voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +4.6	V
V_I	Input voltage range, A port[3]		−0.5 to +V_{CC} + 0.5	V
V_I	Input voltage range, B port[3]		−0.5 to +5.5	V
V_O	Voltage range applied to any output in the high or power-off state, A port/B port[3]		−0.5 to +V_{CC} + 0.5	V
I_{OH}	Current into any output in the high state	A port	−50	mA
I_{OL}	Current into any output in the low state	A port	50	mA
		B port	100	
I_{IK}	Input clamp current	V_I < 0	−50	mA
I_{OK}	Output clamp current	V_O < 0	−50	mA
P_{tot}	Power dissipation per package plastic medium-shrink (SSOP) plastic thin-medium-shrink (TSSOP)	for temperature range: −40 to +125 °C above +55 °C derate linearly with 11.3 mW/K above +55 °C derate linearly with 8 mW/K	 850 600	mW
T_{stg}	Storage temperature range		−60 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS[1]

SYMBOL	PARAMETER		MIN	MAX	MAX	UNIT
V_{CC}	DC supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	
V_{REF}	Supply voltage	GTL	0.74	0.8	0.87	V
		GTL+	0.87	1.0	1.10	
V_I	Input voltage	B port	0		V_{TT}	V
		Except B port	0		5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+50mV			V
		Except B port	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–50mV	V
		Except B port			0.8	
I_{OH}	High-level output current	A port			–50	mA
I_{OL}	Low-level output current	A and B port			50	mA
T_{amb}	*Operating free-air temperature*		–40		+85	°C

NOTES:
1. Unused control inputs must be held high or low to prevent them from floating.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 3.15V; I_{OH} = –100µA	A port	V_{CC}–0.2	–	–	V
		V_{CC} = 3.15V; I_{OH} = –12mA		V_{CC}–0.5	–	–	
		V_{CC} = 3.15V; I_{OH} = –24mA		V_{CC}–0.8	–	–	
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA	A port	–	–	0.2	V
		V_{CC} = 3.0V; I_{OL} = 12mA		–	–	0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		–	–	0.5	
V_{OL}	Low–level output voltage	V_{CC} = 3.15V; I_{OL} = 10mA	B port	–	–	0.2	V
		V_{CC} = 3.15V; I_{OL} = 40mA		–	–	0.4	
		V_{CC} = 3.15V; I_{OL} = 50mA		–	–	0.55	
I_I	Input leakage current	V_{CC} = 3.45V; V_I = V_{CC} or GND	Control pins	–	–	±5	µA
		V_{CC} = 3.45V; V_I = V_{TT} or GND	B port	–	–	±5	
$I_{I(HOLD)}$	Bus Hold current, A outputs	V_{CC} = 3.15V; V_I = 0.8V	A port	75	–	–	µA
		V_{CC} = 3.15V; V_I = 2.0V		–75	–	–	
		V_{CC} = 3.45V[2]; V_I =0.8 to 2.0V		–	–	±500	
I_{OZH}		V_{CC} = 3.45V; V_O = 1.5V	B port	–	–	10	µA
I_{OZ}[4]		V_{CC} = 3.45V; V_O = V_{CC} or GND	A port	–	–	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.45V; V_I = V_{CC} or GND; I_O = 0	A or B port	–	–	20	mA
ΔI_{CC}[4]	Additional supply current per input pin	V_{CC} = 3.45V; V_I = V_{CC} – 0.6	A port or control inputs	–	–	500	µA
C_I		V_I = 3.15V or 0	Control inputs	–	3		pF
C_{IO}		V_O = 3.15V or 0	A port	–	10		pF
		Per IEEE 1194.1	B port	–	8.5		

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the bus hold maximum dynamic current required to switch the input from one state to another.
3. For I/O ports, the parameter I_{OZ} includes the input leakage current.
4. This is the increase in supply current for each input that is at the specified TLL voltage level rather than V_{CC} or GND.

AC CHARACTERISTICS FOR GTL

Over recommended ranges of supply voltage[1]

SYMBOL	PARAMETER		MIN	MAX	UNIT
f_{clock}	Clock frequency		0	200	MHz
t_W	Pulse duration, CLK high or low		2.5		ns
t_{SU}	Setup time	Data before CLK ↑	2.0		ns
		$\overline{CE}$ before CLK ↑	1.0		
t_h	Hold time	Data after CLK ↑	0		ns
		$\overline{CE}$ after CLK ↑	0		

SYMBOL	FROM (INPUT)	TO (OUTPUT)	MIN	TYP[2]	MAX	UNIT
f_{MAX}			200			MHz
t_{PLH}	CLKAB	B		1.7	2.7	ns
t_{PHL}				1.7	2.7	
t_{PLH}	$\overline{OEAB}$	B		1.5	2.4	ns
t_{PHL}				1.5	2.4	
Slew rate	Both transitions			0.7		V/ns
t_r	Transition time, B outputs (0.6 V to 1 V)		0.7	0.8	1.2	ns
t_f	Transition time, B outputs (1 V to 0.6 V)		0.4	0.5	0.6	ns
t_{PLH}	CLKAB	A		2.7	3.8	ns
t_{PHL}				2.7	3.8	
t_{enable}	$\overline{OEAB}$	A		2.5	4.0	ns
$t_{disable}$				2.5	4.0	

NOTES:

1. These parameters are warranted but not production tested.
2. All typical values are measured at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS FOR GTL+

Over recommended ranges of supply voltage[1]

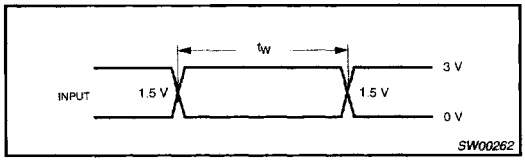
SYMBOL	PARAMETER		MIN	MAX	UNIT
f_{clock}	Clock frequency		0	200	MHz
t_W	Pulse duration, CLK high or low		2.5		ns
t_{SU}	Setup time	Data before CLK ↑	2.0		ns
		$\overline{CE}$ before CLK ↑	1.0		
t_h	Hold time	Data after CLK ↑	0		ns
		$\overline{CE}$ after CLK ↑	0		

SYMBOL	FROM (INPUT)	TO (OUTPUT)	MIN	TYP[2]	MAX	UNIT
f_{MAX}			200			MHz
t_{PLH}	CLKAB	B		1.8	2.8	ns
t_{PHL}				1.8	2.8	
t_{PLH}	$\overline{OEAB}$	B		1.5	2.5	ns
t_{PHL}				1.5	2.5	
Slew rate	Both transitions			0.8		V/ns
t_r	Transition time, B outputs (0.6 V to 1.3V)		0.8	1.2	2.2	ns
t_f	Transition time, B outputs (1 V to 0.6 V)		0.5	0.7	1.0	ns
t_{PLH}	CLKAB	A		2.7	3.8	ns
t_{PHL}				2.7	3.8	
t_{enable}	$\overline{OEAB}$	A		2.5	4.0	ns
$t_{disable}$				2.5	4.0	

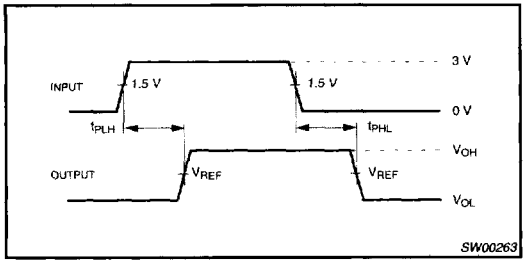
NOTES:

1. These parameters are warranted but not production tested.
2. All typical values are measured at V_{CC} = 3.3V and T_{amb} = 25°C.

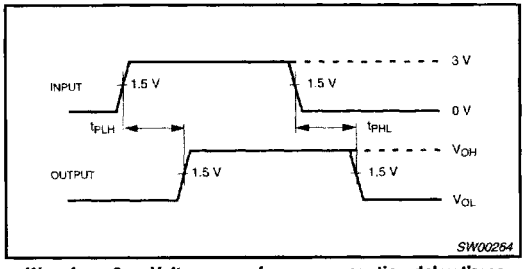
AC WAVEFORMS



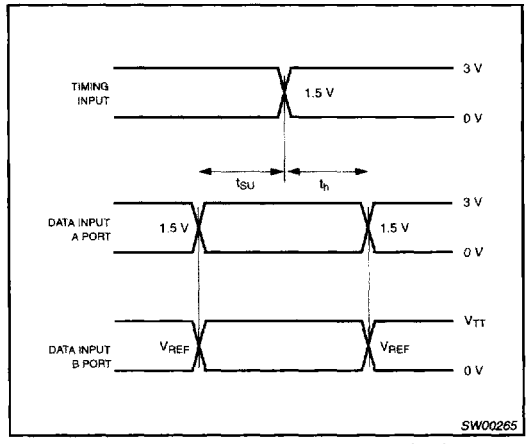
Waveform 1. Voltage waveforms pulse duration



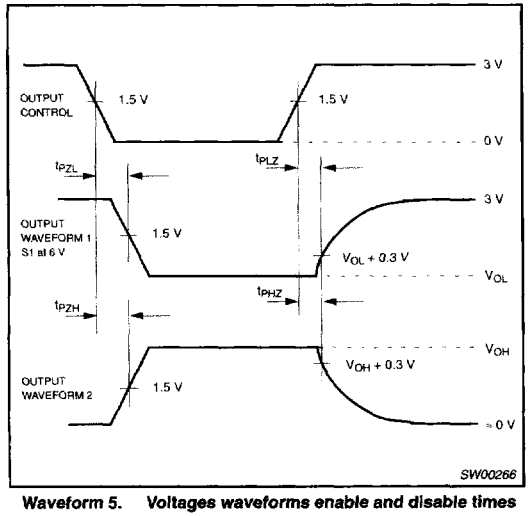
Waveform 2. Voltatage waveforms propagation times. (CLKAB to B port)



Waveform 3. Voltage waveforms propagation delay times (CLKBA to A port)

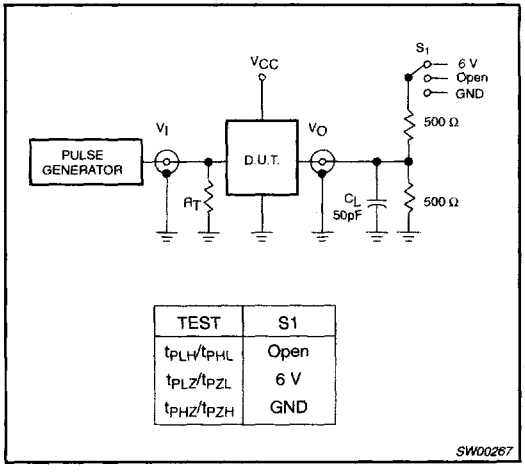


Waveform 4. Voltage waveforms setup and hold times



Waveform 5. Voltages waveforms enable and disable times (A port)

LOAD CIRCUIT FOR A OUTPUTS



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT FOR B OUTPUTS