

High Performance Average Current Mode PWM

**ADVANCED
INFORMATION**

FEATURES

- Combined Accurate Voltage Reference and PWM Functions
- 1% DAC/Reference
- Low Offset Voltage Amplifier
- High Bandwidth Current and Voltage Amplifiers
- Low Offset x10, x20 Current Sense Amplifier
- 100kHz, 200kHz, 400kHz Oscillator Frequency Options
- Foldback Current Limiting
- Undervoltage Lockout
- 1.5A Peak Totem Pole Output
- Chip Disable Function

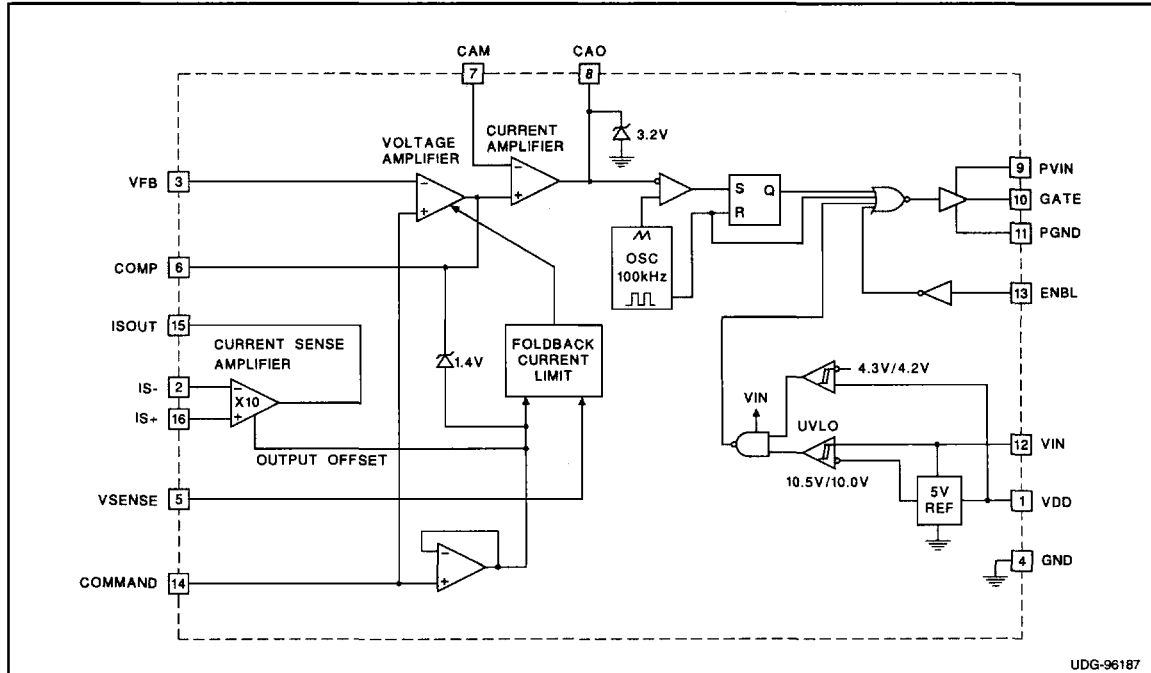
DESCRIPTION

The UCC3881-1,-2,-3,-4,-5,-6 combines high precision reference circuitry with average current mode PWM controller circuitry to power Intel Pentium® Pro and other high end microprocessors with a minimum of external components. The chip includes a precision 5V reference which is accurate to $\pm 1\%$ and is capable of sourcing current to external circuitry. Undervoltage lockout circuitry assures correct logic states at the output during power up and power down. Grounding the ENBL pin forces the GATE output low.

The voltage and current amplifiers have a 5.5MHz gain-bandwidth product to satisfy high performance system requirements. An internal current sense amplifier permits the use of a low value current sense resistor, minimizing power loss. Oscillator frequency is fixed internally at 100kHz, 200kHz, or 400kHz depending upon the option selected. Foldback circuitry reduces the converter current limit to 50% of its nominal value when the converter is short circuited. The gate driver is a totem pole output stage capable of driving an external MOSFET with 1.5A peak current.

This device is available in 16-pin dual in-line and surface-mount packages. The UCC1881-x is specified for operation from -55°C to $+125^{\circ}\text{C}$, the UCC2881-x is specified for operation from -25°C to $+85^{\circ}\text{C}$, and the UCC3881-x is specified for operation from 0°C to 70°C .

BLOCK DIAGRAM

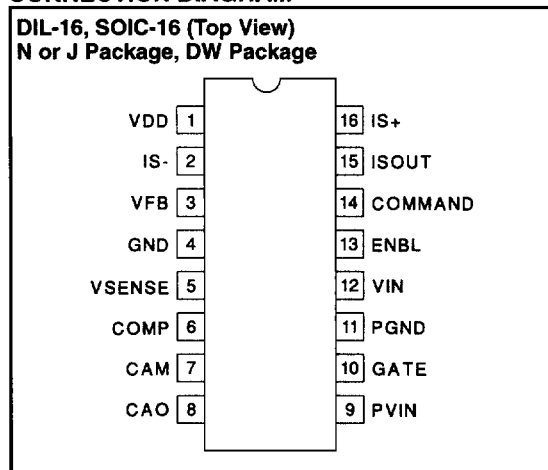


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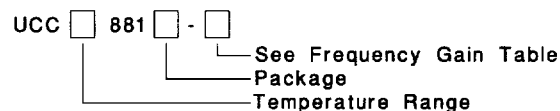
GENERAL POWER SUPPLY

UCC1881-1,-2,-3,-4,-5,-6
 UCC2881-1,-2,-3,-4,-5,-6
 UCC3881-1,-2,-3,-4,-5,-6

CONNECTION DIAGRAM



ORDERING INFORMATION



Frequency Gain Table

	Frequency			CS Amplifier Gain	
	100kHz	200kHz	400kHz	10	20
UCC3881-1	X			X	
UCC3881-2		X		X	
UCC3881-3			X	X	
UCC3881-4	X				X
UCC3881-5		X			X
UCC3881-6			X		X

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VIN = 12V, VSENSE = 3.5V, VENBL = 5V, VPVIN = 12V, VVFB = 3.5, 0°C < TA < 70°C, TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout					
VIN UVLO Turn-on Threshold			10.5	10.8	V
VIN UVLO Turn-off Threshold		9.5	10		V
UVLO Threshold Hysteresis			500		mV
Supply Current					
IIN			2		mA
Reference					
VDD Output Voltage	IvDD = 1mA, 0°C < TA < 70°C	4.95	5	5.05	V
	IvDD = 1mA, -25°C < TA < 85°C		5		
	IvDD = 1mA, -55°C < TA < 125°C		5		
VDD Load Regulation	IvDD = 0mA to 5mA	-10	0		mV
VDD Sourcing Current	VDD = 0V		10		mA
ENBL Pin					
Pullup Current	VENBL = 2.5V		-50	-20	µA
Voltage Error Amplifier					
Input Bias Current	VCM = 3V	-2		0	µA
Input Offset Current	VCM = 3V			0.01	µA
Open Loop Gain	1V < VCOMP < 4V		90		dB

UCC1881-1,-2,-3,-4,-5,-6
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UCC3881-1,-2,-3,-4,-5,-6

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, VIN = 12V, VSENSE = 3.5V, VENBL = 5V, V_{PVIN} = 12V, V_{VFB} = 3.5, 0°C < TA < 70°C, TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Error Amplifier (cont.)					
Common Mode Rejection Ratio	1V < V _{CM} < 3.5V		80		dB
Power Supply Rejection Ratio	10.8V < V _{IN} < 15V		85		dB
Output Sourcing Current	V _{VFB} = 2V, V _{COMMAND} = V _{COMP} = 2.5V		-0.9		mA
Output Sinking Current	V _{VFB} = 3V, V _{COMMAND} = V _{COMP} = 2.5V		7.2		mA
Gain Bandwidth Product	F = 100kHz	3			MHz
Current Sense Amplifier					
Gain (UCCx881-1,-2,-3)			10		V/V
Gain (UCCx881-4,-5,-6)			20		V/V
Input Resistance			5		kΩ
Common Mode Rejection Ratio	0V < V _{CM} < 4.5V		60		dB
Power Supply Rejection Ratio	10.8V < V _{IN} < 15V		80		dB
Output Sourcing Current	V _{IS-} = 2V, V _{ISOUT} = V _{IS+} = 2.5V		-0.9		mA
Output Sinking Current	V _{IS-} = 3V, V _{ISOUT} = V _{IS+} = 2.5V		7.2		mA
-3dB Frequency (UCCx881-1,-2,-3)	At Gain = 10	3.5			MHz
-3dB Frequency (UCCx881-4,-5,-6)	At Gain = 20	1.75			MHz
Current Amplifier					
Input Offset Voltage	V _{CM} = 3V			10	mV
Input Bias Current	V _{CM} = 3V		0.1		μA
Open Loop Gain	1V < V _{CAO} < 3V		90		dB
Output Voltage High			3.2		V
Common Mode Rejection Ratio	1V < V _{CM} < 4.9V		80		dB
Power Supply Rejection Ratio	10.8V < V _{IN} < 15V		80		dB
Output Sourcing Current	V _{CAO} = 2V, V _{CAO} = V _{COMP} = 2.5V		-0.9		mA
Output Sinking Current	V _{CAO} = 3V, V _{CAO} = V _{COMP} = 2.5V		7.2		mA
Gain Bandwidth Product	F = 100kHz	3.5			MHz
Oscillator					
Frequency (UCCx881-1,-4)	TA = 25°C	85	100	115	kHz
Frequency (UCCx881-2,-5)	TA = 25°C		200		kHz
Frequency (UCCx881-3,-6)	TA = 25°C		400		kHz
Frequency Change with Voltage	10.8V < V _{IN} < 15V		1		%
Output Section					
Maximum Duty Cycle		90	95	99	%
Output Low Voltage	I _{GATE} = -100mA		0.2		V
Output High Voltage	I _{GATE} = 100mA		11.8		V
Rise Time	C _{GATE} = 3.3nF		20	80	ns
Fall Time	C _{GATE} = 3.3nF		15	80	ns
Foldback Current Limit					
Clamp Level	Measured at Volt EA Output; V _F B = V _{COMMAND} = 3V		4.4		V
	V _{COMMAND} = 3V, V _{VFB} = 0, V _F B = V _{COMMAND} = 3V		3.7		V
Output Impedance	I _{GATE} = 100mA		2		Ω
	I _{GATE} = -100mA		2		Ω



GENERAL POWER SUPPLY

PIN DESCRIPTIONS

CAM (current amplifier inverting input): The average load current feedback from ISOOUT is applied through a resistor to this pin. The current loop compensation network is also connected to this pin (see CAO below).

CAO (current amplifier output): The current loop compensation network is connected between this pin and CAM. The voltage on this pin is the input to the PWM comparator and regulates the output voltage of the system. The GATE output is disabled (held low) unless the voltage on this pin exceeds 1V, allowing the PWM to force zero duty cycle when necessary. The PWM forces 100% duty cycle when the voltage on CAO exceeds the oscillator peak voltage (3V). To provide superior transient response, a 3.2V clamp circuit prevents the CAO voltage from rising excessively past the oscillator peak voltage.

COMMAND (digital-to-analog converter output voltage): This pin is the noninverting input of the voltage amplifier. The voltage on this pin sets the switching regulator output voltage. A high accuracy voltage may be generated by connecting this pin to the tap point of a resistor divider connected between VDD and GND. Bypass COMMAND with a 0.01 μ F, low ESR, low ESL capacitor for best circuit noise immunity.

COMP (voltage amplifier output): The system voltage compensation network is applied between COMP and VFB.

GATE (PWM output, MOSFET driver): This output provides a 1.5A totem pole driver. Use a series resistor of at least 5 Ω between this pin and the gate of the external MOSFET to prevent excessive overshoot. GATE has a typical output impedance of 2 Ω .

GND (signal ground): All voltages are measured with respect to GND. Bypass capacitors on VIN and VDD should be connected directly to the ground plane near GND.

ENBL (chip enable pin): This input is used to disable the GATE output. Grounding this pin causes the GATE output to be held low; floating the pin or pulling it up to 5V ensures normal operation. ENBL is pulled up to 5V internally.

IS- (current sense amplifier inverting input): This pin is the inverting input to the current sense amplifier and is connected to the low side of the average current sense resistor.

IS+ (current sense amplifier noninverting input): This pin is the noninverting input to the current sense amplifier and is connected to the high side of the average current sense resistor.

ISOOUT (current sense amplifier output): This pin is the output of the current sense amplifier. The voltage on this pin is $(COMMAND + GCSA \cdot I_{AVG} \cdot R_{SENSE})$, where COMMAND is the voltage on COMMAND, I_{AVG} is the average load current of the system, and R_{SENSE} is the value of the average current sensing resistor. GCSA is the fixed gain of the current sense amplifier (10 for UCCx881-1,-2,-3, and 20 for UCCx881-4,-5,-6).

PGND (power ground): This pin provides a dedicated ground for the output gate driver. GND and PGND should be connected externally using a short PC board trace. Decouple PVIN to PGND with a low ESR capacitor $\geq 0.1\mu$ F.

PVIN (positive power supply voltage): This pin provides a dedicated power supply connection for the output gate driver. This pin should be bypassed directly to PGND. VIN and PVIN may be tied together directly, or VIN may be filtered from PVIN.

VFB (voltage amplifier inverting input): This input is connected to COMP through a feedback network and to the power supply output through a resistor or a divider network.

VDD (voltage reference output): This pin provides an accurate 5V reference and is internally short circuit current limited. VDD also provides a threshold voltage for the UVLO comparator. For best reference stability, bypass VDD directly to GND with a low ESR, low ESL capacitor of at least 0.01 μ F.

VIN (positive signal supply voltage): This pin supplies power to the chip. Connect VIN to a stable voltage source that is at least 10.8V above GND and capable of sourcing at least 15mA. The GATE output will be held low until VDD exceeds the upper undervoltage lockout threshold. This pin should be bypassed directly to GND.

VSENSE (output voltage sensing input): This pin is connected directly to the system output voltage and is used by the foldback current limiting circuitry.