

# SN54F541, SN74F541 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SDFS021A – D3126, JANUARY 1989 – REVISED OCTOBER 1993

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Data Flow-Through Pinout (All Inputs on Opposite Side From Outputs)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs

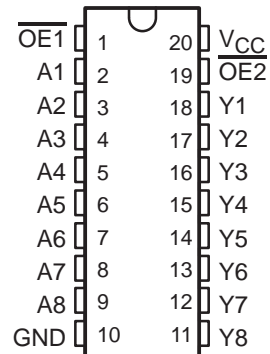
## description

The 'F541 octal buffer/line driver is ideal for driving bus lines or buffering memory address registers. The device features inputs and outputs on opposite sides of the package to facilitate printed-circuit-board layout.

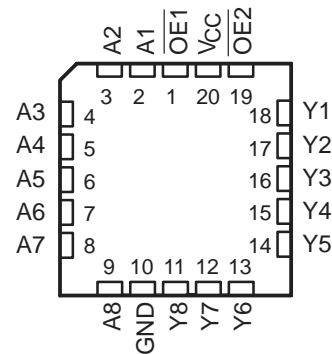
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all eight outputs are in the high-impedance state.

The SN54F541 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74F251 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54F541 . . . J PACKAGE  
SN74F541 . . . DW OR N PACKAGE  
(TOP VIEW)



SN54F541 . . . FK PACKAGE  
(TOP VIEW)



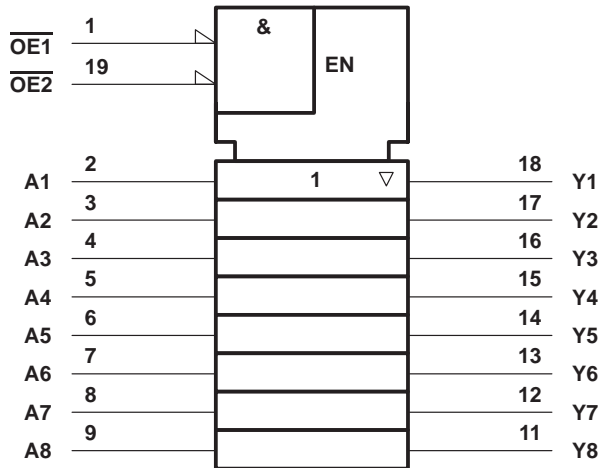
FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

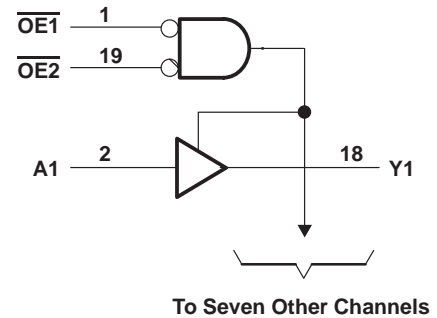
# SN54F541, SN74F541 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SDFS021A – D3126, JANUARY 1989 – REVISED OCTOBER 1993

## logic symbol†



## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-1.2 V to 7 V
Input current range .....	-30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state .....	-0.5 V to 5.5 V
Voltage range applied to any output in the high state .....	-0.5 V to $V_{CC}$
Current into any output in the low state: SN54F541 .....	96 mA
SN74F541 .....	128 mA
Operating free-air temperature range: SN54F541 .....	-55°C to 125°C
SN74F541 .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

		SN54F541			SN74F541			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{IK}$	Input clamp current			-18			-18	mA
$I_{OH}$	High-level output current			-12			-15	mA
$I_{OL}$	Low-level output current			48			64	mA
$T_A$	Operating free-air temperature	-55		125	0		70	°C

# SN54F541, SN74F541 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		SN54F541			SN74F541			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2			-1.2	V
$V_{OH}$	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -3\text{ mA}$	2.4	3.3		2.4	3.3		V
		$I_{OH} = -12\text{ mA}$	2	3.2					
		$I_{OH} = -15\text{ mA}$				2	3.1		
	$V_{CC} = 4.75\text{ V}$ ,	$I_{OH} = -3\text{ mA}$				2.7			
$V_{OL}$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 48\text{ mA}$		0.38	0.55				V
		$I_{OL} = 64\text{ mA}$					0.42	0.55	
$I_{OZH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.7\text{ V}$			50			50	$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0.5\text{ V}$			-50			-50	$\mu\text{A}$
$I_I$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 7\text{ V}$			0.1			0.1	mA
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$			20			20	$\mu\text{A}$
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.5\text{ V}$			-0.6			-0.6	mA
$I_{OS}^\ddagger$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0$	-100		-225	-100		-225	mA
$I_{CC}$	$V_{CC} = 5.5\text{ V}$	Outputs high		28	35		28	35	mA
		Outputs low		62	75		62	75	
		Outputs disabled		40	55		40	55	

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$ , $C_L = 50\text{ pF}$ , $R_L = 500\ \Omega$ , $T_A = 25^\circ\text{C}$			$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $C_L = 50\text{ pF}$ , $R_L = 500\ \Omega$ , $T_A = \text{MIN to MAX}^\S$				UNIT
			'F541			SN54F541		SN74F541		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	Any A	Y	1.5	3.3	5.5	1	6.5	1.5	6	ns
$t_{PHL}$			1.5	2.7	5.5	1	6.5	1.5	6	
$t_{PZH}$	$\overline{OE}$	Y	3	5.8	8	1.7	10	2.5	9.5	ns
$t_{PZL}$			3.5	6.1	8.5	2.2	10	3	9.5	
$t_{PHZ}$	$\overline{OE}$	Y	1.5	3.4	6	1	7	1.5	6.5	ns
$t_{PLZ}$			1.5	2.9	5.5	1	7.5	1.5	6	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and waveforms are shown in Section 1.





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PRODUCT SUPPORT: [TRAINING](#)

## SN74F541, Octal Buffers/Drivers With 3-State Outputs

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54F541	SN74F541
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.5 to 5.5
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive (mA)		-15/64
tpd max (ns)		6
Static Current		55

### FEATURES

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- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
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- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs

### DESCRIPTION

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The 74F541 octal buffer/line driver is ideal for driving bus lines or buffering memory address registers. The device features inputs and outputs on opposite sides of the package to facilitate printed-circuit-board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all eight outputs are in the high-impedance state.

The SN54F541 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74F251 is characterized for operation from 0°C to 70°C.

### TECHNICAL DOCUMENTS

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### DATASHEET

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Full datasheet in Acrobat PDF: [sn74f541.pdf](#) (70 KB, Rev.A) (Updated: 10/01/1993)

### APPLICATION NOTES

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View Application Notes for [Digital Logic](#)

- [Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs \(Rev. A\)](#) (SCBA012A - Updated: 08/01/1997)
- [Designing With Logic \(Rev. C\)](#) (SDYA009C - Updated: 06/01/1997)
- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
- [Timing Differences of 10-pF Versus 50pF Loading](#) (SCEA004 - Updated: 11/01/1996)

#### RELATED DOCUMENTS

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View Related Documentation for [Digital Logic](#)

- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [Logic Selection Guide Second Half 2002 \(Rev. R\)](#) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- [Military Semiconductors Selection Guide 2002 \(Rev. B\)](#) (SGYC003B, 1648 KB - Updated: 04/22/2002)

#### PRICING/AVAILABILITY/PKG

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#### DEVICE INFORMATION

ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY   SUS	STD PACK QTY
SN74F541DW	ACTIVE	<a href="#">SOP (DW)</a>   20	0 TO 70	<a href="#">View Contents</a>	1KU   0.56	25
SN74F541DWR	ACTIVE	<a href="#">SOP (DW)</a>   20	0 TO 70	<a href="#">View Contents</a>	1KU   0.56	2000
SN74F541N	ACTIVE	<a href="#">PDIP (N)</a>   20	0 TO 70	<a href="#">View Contents</a>	1KU   0.56	20
SN74F541NSR	ACTIVE	<a href="#">SOP (NS)</a>   20		<a href="#">View Contents</a>	1KU   2.10	2000

#### TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002

IN STOCK	IN PROGRESS QTY DATE	LEAD TIME
N/A*	1   04 Oct	5 WKS
	> 10k   11 Oct	
2000	2000   19 Sep	5 WKS
	167   25 Sep	
	> 10k   11 Oct	
N/A*	1   07 Oct	5 WKS
	> 10k   14 Oct	
	> 10k   21 Oct	
N/A*	> 10k   14 Oct	5 WKS

#### REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002

DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
<a href="#">Avnet</a>   AMERICA	> 1k	<a href="#">BUY NOW</a>
<a href="#">Avnet</a>   AMERICA	> 1k	<a href="#">BUY NOW</a>
<a href="#">Avnet</a>   AMERICA	398	<a href="#">BUY NOW</a>

#### MODELS

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- [IBIS Model of SN74F541](#) (SDFM011, 65 KB - Updated: 08/18/2000)
- [IBIS Model of SN74F541](#) (SDFM011, 10 KB, ZIP - Updated: 08/18/2000)

Table Data Updated on: 9/26/2002

