PRELIMINARY

DESCRIPTION

The HY62UF8200 / HY62QF8200 / HY62EF8200 / HY62SF8200 is a high speed, super low power and 2M bit full CMOS SRAM organized as 262,144 words by 8bits. The HY62UF8200 / HY62QF8200 / HY62EF8200 / HY62SF8200 uses high performance full CMOS process technology and is designed for high speed and low power circuit technology. It is particularly well-suited for the high density low power system application. This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 1.5V.

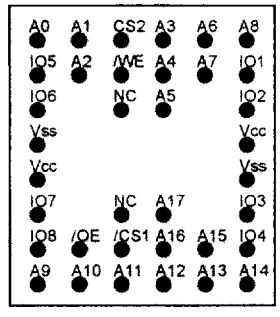
FEATURES

- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Battery backup(LL/SL-part)
  - 1.5V(min) data retention
- Standard pin configuration
  - 48ball uBGA

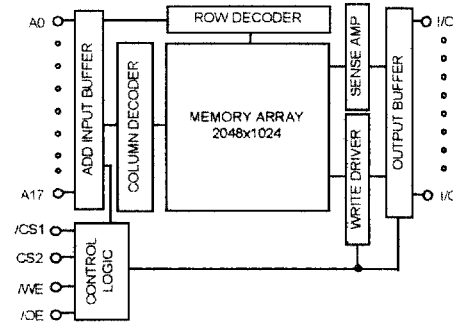
Product No.	Voltage (V)	Speed (ns)	Operation Current(mA)	Standby Current(uA)		Temperature (℃)
				LL	SL	
HY62UF8200	3.0	70/85/100	10	10	2	0~70(Normal)
HY62UF8200-I	3.0	70/85/100	10	10	2	-40~85(E.T.)
HY62QF8200	2.5	85/100/120	5	10	2	0~70(Normal)
HY62QF8200-I	2.5	85/100/120	5	10	2	-40~85(E.T.)
HY62EF8200	2.0	100/120/150	5	10	2	0~70(Normal)
HY62EF8200-I	2.0	100/120/150	5	10	2	-40~85(E.T.)
HY62SF8200	1.8	120/150/200	5	10	2	0~70(Normal)
HY62SF8200-I	1.8	120/150/200	5	10	2	-40~85(E.T.)

Note 1. E.T. : Extended Temperature, Normal : Normal Temperature
2. Current value is max.

PIN CONNECTION



BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Function	Pin Name	Pin Function
/CS1	Chip Select 1	A0 ~ A17	Address Input
CS2	Chip Select 2	I/O1 ~ I/O8	Data Input/Output
/WE	Write Enable	Vcc	Power(3.0V, 2.5V, 2.0V or 1.8V)
/OE	Output Enable	Vss	Ground

ORDERING INFORMATION

Part No.	Speed	Power	Temp.	Package
HY62UF8200LLM	70/85/100	LL-part		uBGA
HY62UF8200SLM	70/85/100	SL-part		uBGA
HY62UF8200LLM-I	70/85/100	LL-part	E.T.	uBGA
HY62UF8200SLM-I	70/85/100	SL-part	E.T.	uBGA
HY62QF8200LLM	85/100/120	LL-part		uBGA
HY62QF8200SLM	85/100/120	SL-part		uBGA
HY62QF8200LLM-I	85/100/120	LL-part	E.T.	uBGA
HY62QF8200SLM-I	85/100/120	SL-part	E.T.	uBGA
HY62EF8200LLM	100/120/150	LL-part		uBGA
HY62EF8200SLM	100/120/150	SL-part		uBGA
HY62EF8200LLM-I	100/120/150	LL-part	E.T.	uBGA
HY62EF8200SLM-I	100/120/150	SL-part	E.T.	uBGA
HY62SF8200LLM	120/150/200	LL-part		uBGA
HY62SF8200SLM	120/150/200	SL-part		uBGA
HY62SF8200LLM-I	120/150/200	LL-part	E.T.	uBGA
HY62SF8200SLM-I	120/150/200	SL-part	E.T.	uBGA

Note 1. E.T. : Extended Temperature, Blank : Normal Temperature

ABSOLUTE MAXIMUM RATING (1)

Symbol	Parameter	Rating	Unit	Remark
V_{IN}, V_{OUT}	Input/Output Voltage	-0.2 to 3.6	V	
V_{CC}	Power Supply	-0.2 to 4.0	V	
T_A	Operating Temperature	0 to 70	℃	HY62UF8200
				HY62QF8200
				HY62EF8200
				HY62SF8200
		-40 to 85	℃	HY62UF8200-I
				HY62QF8200-I
				HY62EF8200-I
				HY62SF8200-I
T_{STG}	Storage Temperature	-55 to 150	℃	
P_D	Power Dissipation	1.0	W	
T_{SOLDER}	Lead Soldering Temperature & Time	260•5	℃•sec	

Note

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITION

Symbol	Parameter	Product	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	HY62UF8200-(I)	2.7	3.0	3.3	V
		HY62QF8200-(I)	2.2	2.5	2.8	V
		HY62EF8200-(I)	1.8	2.0	2.2	V
		HY62SF8200-(I)	1.6	1.8	2.0	
Vss	Ground	HY62UF8200-(I) HY62QF8200-(I) HY62EF8200-(I) HY62SF8200-(I)	0	0	0	V
VIH	Input High Voltage	HY62UF8200-(I)	2.2	-	Vcc+0.2	V
		HY62QF8200-(I)	2.0	-	Vcc+0.2	V
		HY62EF8200-(I)	1.6	-	Vcc+0.2	V
		HY62SF8200-(I)	1.4		Vcc+0.2	V
VIL	Input Low Voltage	HY62UF8200-(I) HY62QF8200-(I) HY62EF8200-(I) HY62SF8200-(I)	-0.2(1)	-	0.4	V

Note : 1. VIL = -1.5V for pulse width less than 30ns

TRUTH TABLE

/CS1	CS2	/WE	/OE	MODE	I/O OPERATION	Supply Current
H	X	X	X	Standby	High-Z	Isb, Isb1
X	L	X	X			
L	H	H	H	Output Disabled	High-Z	Icc
L	H	H	L	Read	Data Out	Icc
L	H	L	X	Write	Data In	Icc

Note :
1. H=VIH, L=VIL, X=don't care

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.0V±10%/2.5V±10%/2.0V±10%/1.8V±10%, T_A = 0℃ to 70℃(Normal)/ -40℃ to 85℃(E.T.)

Sym	Parameter		Test Condition			Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current		$V_{SS} \le V_{IN} \le V_{CC}$			-1	-	1	uA
I_{LO}	Output Leakage Current		$V_{SS} \le V_{OUT} \le V_{CC}$, /CS1 = V_{IH} or CS2 = V_{IL} or /OE = V_{IH} or /WE = V_{IL}			-1	-	1	uA
I_{CC}	Operating Power Supply Current		/CS1 = V_{IL}, CS2 = V_{IH}, V_{IN} = V_{IH} or V_{IL}, $I_{I/O}$ = 0mA	Vcc = 3.0V		-	5	10	mA
				Vcc = 2.5V/2V/1.8V		-	3	5	mA
I_{CC1}	Average Operating Current	HY62UF8200-(I)	/CS1 = V_{IL} CS2 = V_{IH}, Min Duty Cycle = 100%, $I_{I/O}$ = 0mA			-	-	45	mA
		HY62QF8200-(I)				-	-	35	mA
		HY62EF8200-(I)				-	-	25	mA
		HY62SF8200-(I)				-	-	20	mA
I_{SB}	TTL Standby Current (TTL Input)	HY62UF8200-(I)	/CS1 = V_{IH} or CS2 = V_{IL}			-	-	0.5	mA
		HY62QF8200-(I)				-	-	0.3	mA
		HY62EF8200-(I)				-	-	0.3	mA
		HY62SF8200-(I)				-	-	0.3	mA
I_{SB1}	Standby Current (CMOS Input)		/CS1 ≥ Vcc - 0.2V CS2 ≥ 0.2V or CS2 ≥ Vcc - 0.2V		SL	-	0.05	2	uA
					LL	-	-	10	uA
V_{OL}	Output Low Voltage		Vcc = 3.0V	I_{OL} = 2.1mA		-	-	0.4	V
			Vcc = 2.5V	I_{OL} = 0.5mA					
			Vcc = 2.0V	I_{OL} = 0.33mA					
			Vcc = 1.8V	I_{OL} = 0.26mA					
V_{OH}	Output High Voltage	HY62UF8200-(I)	Vcc = 3.0V	I_{OH} = -1.0mA		2.2	-	-	V
		HY62QF8200-(I)	Vcc = 2.5V	I_{OH} = -0.5mA		2.0	-	-	V
		HY62EF8200-(I)	Vcc = 2.0V	I_{OH} = -0.44mA		1.6	-	-	V
		HY62SF8200-(I)	Vcc = 1.8V	I_{OH} = -0.44mA		1.4	-	-	V

Note : Typical values are at Vcc = 3.0V/2.5V/2.0V/1.8V, T_A = 25℃

AC CHARACTERISTICS

Vcc = 3.0V±10%, TA = 0℃ to 70℃(Normal)/ -40℃ to 85℃(E.T.), unless otherwise specified

#	Symbol	Parameter	-70		-85		-10		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
	READ CYCLE								
1	tRC	Read Cycle Time	70	-	85	-	100	-	ns
2	tAA	Address Access Time	-	70	-	85	-	100	ns
3	tACS	Chip Select Access Time	-	70	-	85	-	100	ns
4	tOE	Output Enable to Output Valid	-	40	-	45	-	50	ns
5	tCLZ	Chip Select to Output in Low Z	10	-	10	-	20	-	ns
6	tOLZ	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
7	tCHZ	Chip Deselection to Output in High Z	0	30	0	30	0	30	ns
8	tOHZ	Out Disable to Output in High Z	0	30	0	30	0	30	ns
9	tOH	Output Hold from Address Change	10	-	10	-	15	-	ns
	WRITE CYCLE								
10	tWC	Write Cycle Time	70	-	85	-	100	-	ns
11	tCW	Chip Selection to End of Write	60	-	70	-	80	-	ns
12	tAW	Address Valid to End of Write	60	-	70	-	80	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width	50	-	55	-	75	-	ns
15	tWR	Write Recovery Time	0	-	0	-	0	-	ns
16	tWHZ	Write to Output in High Z	0	25	0	30	0	35	ns
17	tDW	Data to Write Time Overlap	30	-	35	-	45	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
19	tOW	Output Active from End of Write	5	-	5	-	10	-	ns

Vcc = 2.5V±10%, TA = 0℃ to 70℃(Normal)/ -40℃ to 85℃(E.T.), unless otherwise specified

#	Symbol	Parameter	-85		-10		-12		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
	READ CYCLE								
1	tRC	Read Cycle Time	85	-	100	-	120	-	ns
2	tAA	Address Access Time	-	85	-	100	-	120	ns
3	tACS	Chip Select Access Time	-	85	-	100	-	120	ns
4	tOE	Output Enable to Output Valid	-	45	-	50	-	60	ns
5	tCLZ	Chip Select to Output in Low Z	10	-	20	-	20	-	ns
6	tOLZ	Output Enable to Output in Low Z	5	-	5	-	10	-	ns
7	tCHZ	Chip Deselection to Output in High Z	0	30	0	30	0	40	ns
8	tOHZ	Out Disable to Output in High Z	0	30	0	30	0	40	ns
9	tOH	Output Hold from Address Change	10	-	15	-	15	-	ns
	WRITE CYCLE								
10	tWC	Write Cycle Time	85	-	100	-	120	-	ns
11	tCW	Chip Selection to End of Write	70	-	80	-	100	-	ns
12	tAW	Address Valid to End of Write	70	-	80	-	100	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width	55	-	75	-	85	-	ns
15	tWR	Write Recovery Time	0	-	0	-	0	-	ns
16	tWHZ	Write to Output in High Z	0	30	0	35	0	40	ns
17	tDW	Data to Write Time Overlap	35	-	45	-	50	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
19	tOW	Output Active from End of Write	5	-	10	-	10	-	ns

Vcc = 2.0V ± 10%, TA = 0℃ to 70℃(Normal)/ -40℃ to 85℃(E.T.), unless otherwise specified

#	Symbol	Parameter	-100		-120		-150		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
	READ CYCLE								
1	tRC	Read Cycle Time	100	-	120	-	150	-	ns
2	tAA	Address Access Time	-	100	-	120	-	150	ns
3	tACS	Chip Select Access Time	-	100	-	120	-	150	ns
4	tOE	Output Enable to Output Valid	-	50	-	60	-	75	ns
5	tCLZ	Chip Select to Output in Low Z	20	-	20	-	20	-	ns
6	tOLZ	Output Enable to Output in Low Z	5	-	10	-	10	-	ns
7	tCHZ	Chip Deselection to Output in High Z	0	30	0	40	0	50	ns
8	tOHZ	Out Disable to Output in High Z	0	30	0	40	0	50	ns
9	tOH	Output Hold from Address Change	15	-	15	-	15	-	ns
	WRITE CYCLE								
10	tWC	Write Cycle Time	100	-	120	-	150	-	ns
11	tCW	Chip Selection to End of Write	80	-	100	-	120	-	ns
12	tAW	Address Valid to End of Write	80	-	100	-	120	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width	75	-	85	-	100	-	ns
15	tWR	Write Recovery Time	0	-	0	-	0	-	ns
16	tWHZ	Write to Output in High Z	0	35	0	40	0	50	ns
17	tDW	Data to Write Time Overlap	45	-	50	-	60	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
19	tOW	Output Active from End of Write	10	-	10	-	10	-	ns

Vcc = 1.8V ± 10%, TA = 0℃ to 70℃(Normal)/ -40℃ to 85℃(E.T.), unless otherwise specified

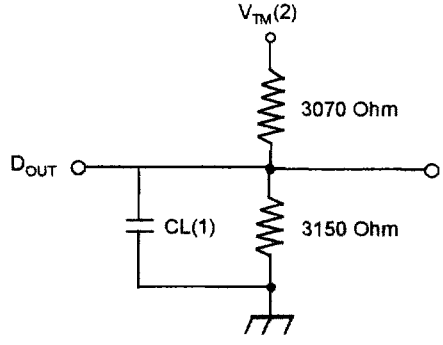
#	Symbol	Parameter	-12		-15		-20		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
	READ CYCLE								
1	tRC	Read Cycle Time	120	-	150	-	200	-	ns
2	tAA	Address Access Time	-	120	-	150	-	200	ns
3	tACS	Chip Select Access Time	-	120	-	150	-	200	ns
4	tOE	Output Enable to Output Valid	-	60	-	75	-	100	ns
5	tCLZ	Chip Select to Output in Low Z	20	-	20	-	30	-	ns
6	tOLZ	Output Enable to Output in Low Z	10	-	10	-	15	-	ns
7	tCHZ	Chip Deselection to Output in High Z	0	40	0	50	0	60	ns
8	tOHZ	Out Disable to Output in High Z	0	40	0	50	0	60	ns
9	tOH	Output Hold from Address Change	15	-	15	-	30	-	ns
	WRITE CYCLE								
10	tWC	Write Cycle Time	120	-	150	-	200	-	ns
11	tCW	Chip Selection to End of Write	100	-	120	-	170	-	ns
12	tAW	Address Valid to End of Write	100	-	120	-	170	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width	85	-	100	-	135	-	ns
15	tWR	Write Recovery Time	0	-	0	-	0	-	ns
16	tWHZ	Write to Output in High Z	0	60	0	70	0	80	ns
17	tDW	Data to Write Time Overlap	50	-	60	-	80	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
19	tOW	Output Active from End of Write	10	-	15	-	15	-	ns

AC TEST CONDITIONS

T_A = 0℃ to 70℃(Normal) / -40℃ to 85℃(E.T.), unless otherwise specified

PARAMETER		Value
Input Pulse Level	HY62UF8200-(I)	0.4V to 2.2V
	HY62QF8200-(I)	0.4V to 2.2V
	HY62EF8200-(I)	0.4V to 1.8V
	HY62SF8200-(I)	0.4V to 1.6V
Input Rise and Fall Time		5ns
Input and Output Timing Reference Level	HY62UF8200-(I)	1.5V
	HY62QF8200-(I)	1.1V
	HY62EF8200-(I)	0.9V
	HY62SF8200-(I)	0.8V
Output Load		CL = 30pF + 1TTL Load

AC TEST LOADS



Note
1. Including jig and scope capacitance
2. V_{TM} = 2.8V for Vcc = 3.0V : HY62UF8200-(I)
   V_{TM} = 2.3V for Vcc = 2.5V : HY62QF8200-(I)
   V_{TM} = 1.8V for Vcc = 2.0V : HY62EF8200-(I)
   V_{TM} = 1.6V for Vcc = 1.8V : HY62SF8200-(I)

CAPACITANCE

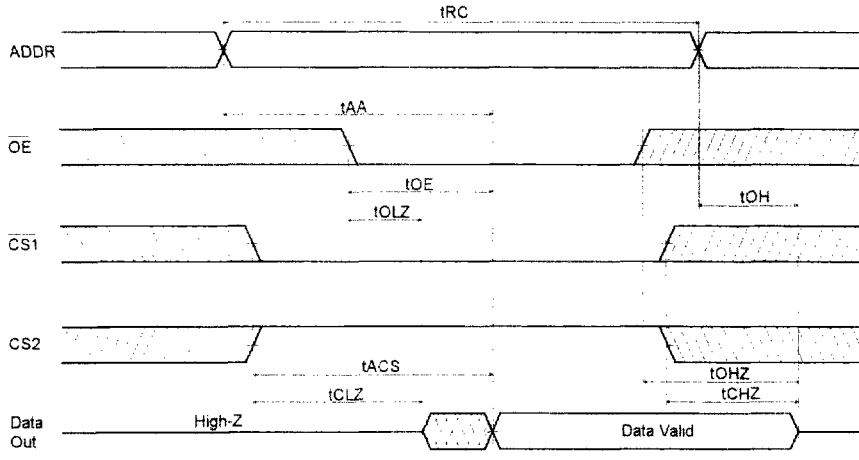
(Temp = 25℃, f= 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance(Add, /CS, /WE, /OE)	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance(I/O)	$V_{I/O}$ = 0V	10	pF

Note : These parameters are sampled and not 100% tested

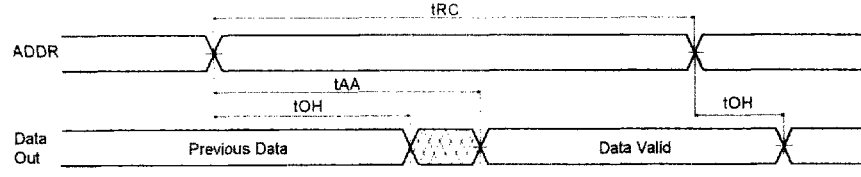
TIMING DIAGRAM

READ CYCLE 1



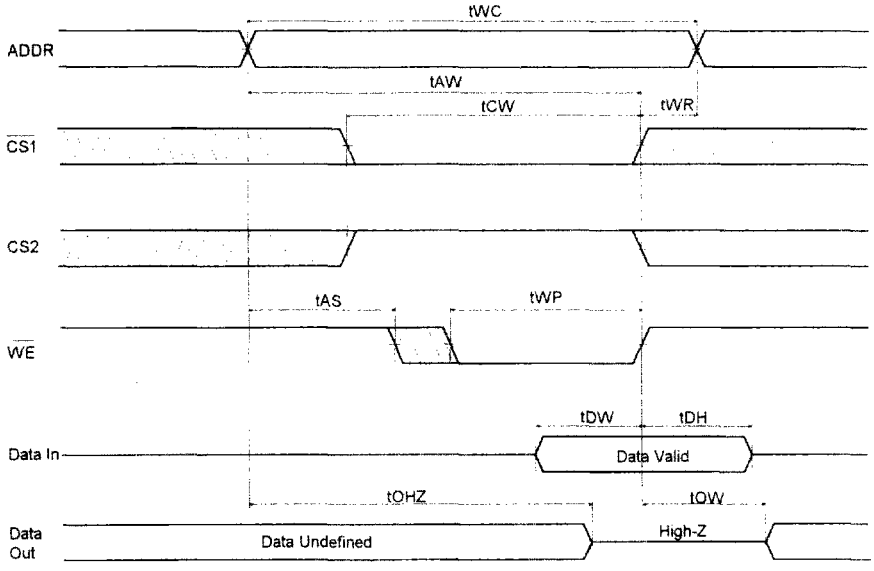
Note(READ CYCLE):
1. tCHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels
2. At any given temperature and voltage condition, tCHZ max. is less than tCLZ min. both for a given device and from device to device.
3. /WE is high for the read cycle.

READ CYCLE 2

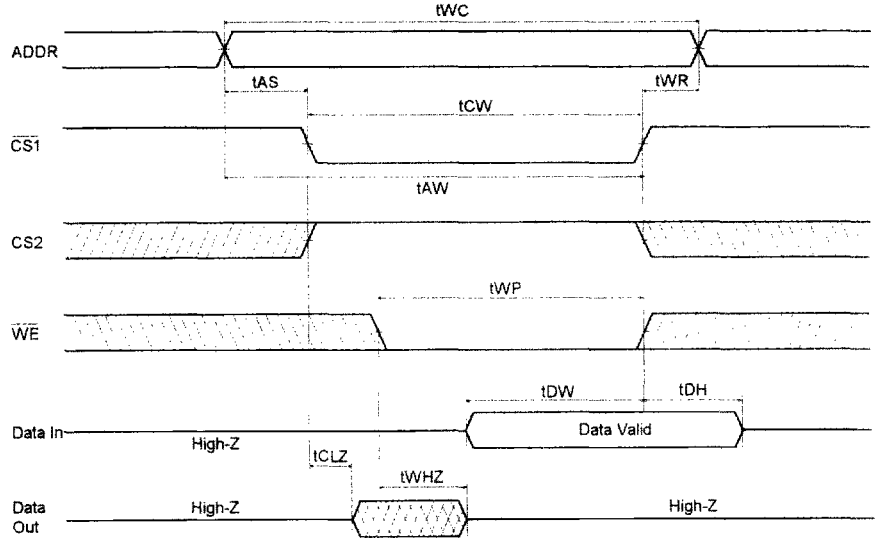


Note(READ CYCLE):
1. /WE is high for the read cycle.
2. Device is continuously selected /CS1 = V_{IL}, CS2 = V_{IH}
3. /OE =V_{IL}.

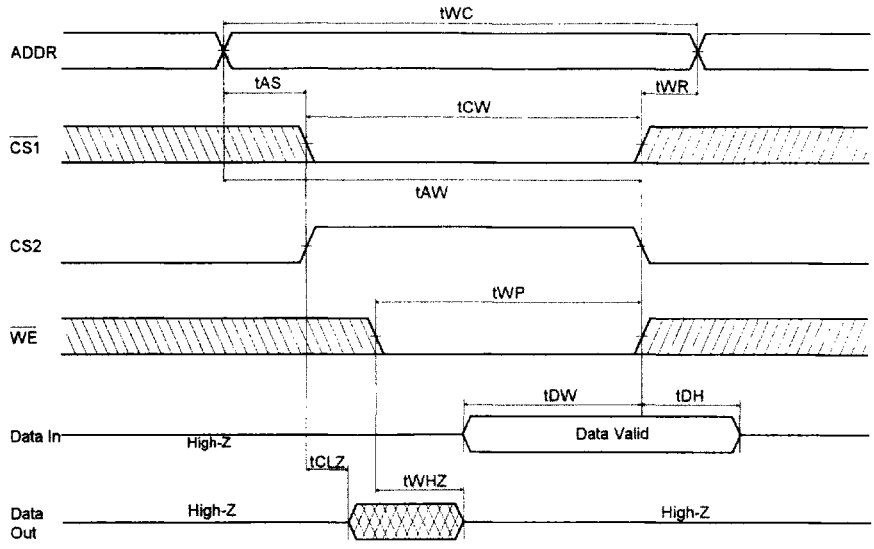
WRITE CYCLE 1(/WE Controlled)



WRITE CYCLE 2 (/CS1 Controlled)



WRITE CYCLE 3 (CS2 Controlled)



Notes(WRITE CYCLE):

1. A write occurs during the overlap of a low /CS1, CS2 and low /WE. A write begines at the latest transition among /CS1 going low, CS2 going high and /WE going low: A write ends at the earliest transition among /CS1 going high, CS2 low and /WE going high. tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS1 going low or CS2 going high to the end of write .
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR is applied in case a write ends as /CS1, or /WE going high, and tWR is applied in case a write ends at CS2 going low.
5. If /OE, CS2 and /WE are in the read mode during this period, the I/O pins are in the output low-Z state, input of opposite phase of the output must not be applied because bus contention can occur.
6. If /CS1 goes low simultaneously with /WE going low, the outputs remain in high impedance state.
7. Dout is the read data of the new address.
8. When /CS1 is low and CS2 is high, I/O pins are in the output state. The input signals in the opposite phase leading to the outputs should not be applied.

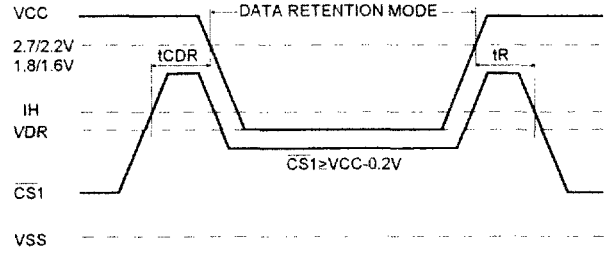
DATA RETENTION ELECTRIC CHARACTERISTIC

T_A=0℃ to 70℃(Normal)/-40℃ to 85℃(E.T.)

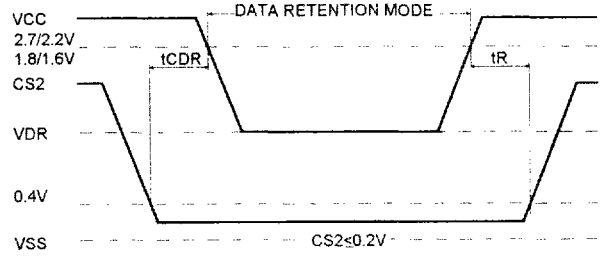
Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{DR}	Vcc for Data Retention	/CS1 ≥ Vcc-0.2V, CS2 ≤ 0.2V or ≥ Vcc-0.2V, Vss ≤ V_{IN} ≤ Vcc		1.5	-	3.3	V
I_{CCDR}	Data Retention Current	Vcc=2.0V, /CS1 ≥ Vcc - 0.2V, CS2 ≤ 0.2V or ≥ Vcc-0.2V, Vss ≤ V_{IN} ≤ Vcc	LL	-	-	10	uA
			SL	-	-	2	uA
tCDR	Chip Deselect to Data Retention Time	See Data Retention Timing Diagram		0	-	-	ns
tR	Operating Recovery Time			tRC(2)	-	-	ns

Notes:
1. Typical values are under the condition of T_A = 25℃.
2. tRC is read cycle time.

DATA RETENTION TIMING DIAGRAM 1



DATA RETENTION TIMING DIAGRAM 2



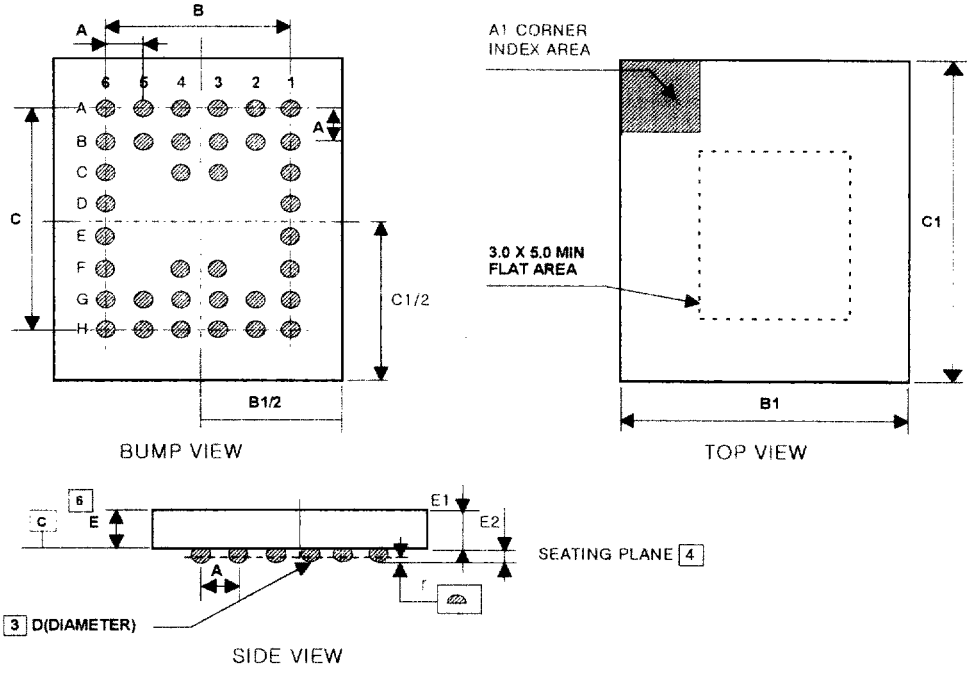
Note :
1. 2.7V : HY62UF8200 and HY62UF8200-I
   2.2V : HY62QF8200 and HY62QF8200-I
   1.8V : HY62EF8200 and HY62EF8200-I
   1.6V : HY62SF8200 and HY62SF8200-I

RELIABILITY SPEC.

TEST	MODE	TEST SPEC.
ESD	HBM	≥ 2000V
	MM	≥ 250V
LATCH - UP		≤ -100mA
		≥ 100mA

PACKAGE INFORMATION

48ball Micro Ball Grid Array Package(M)



Symbol	Min.	Typ.	Max.
A	-	0.75	-
B	-	3.75	-
B1	6.70	6.80	6.90
C	-	5.25	-
C1	9.30	9.40	9.50
D	0.25	0.30	0.35
E	0.79	0.80	0.81
E1	-	0.55	-
E2	0.20	0.25	0.30
r	-	-	0.08

Note

1. DIMENSIONING AND TOLERANCING PER ASME Y14. SM-1994.
2. ALL DIMENSIONS ARE MILLIMETERS.
3. DIMENSION " D " IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER IN A PLANE PARALLEL TO DATUM C
4. PRIMARY DATUM C(SEATING PLANE) IS DEFINED BY THE CROWN OF THE SOLDER BALLS.
5. SOLDER BALL ARRAY MAY BE DEPOPULATED BY OMISSION BALLS FROM A FULL MATRIX. NO SHIFTING OF MATRIX PATTERN IS ALLOWED.
6. THIS IS A CONTROLLING DIMENSION.