Low Power PCIe/ Thunderbolt Clock Gernerator

Features

- 3.3V ±10% supply voltage
- 25MHz XTAL or reference clock input
- Ourput
  - 5x100MHz PCIe 3.0/2.0/1.0 clock with low power push-pull output buffers (no 50-ohm to ground needed), spread spectrum capability on all 100MHz clock outputs with -0.5% down spread
  - 2x25MHz LVCMOS clock
- Industrial temperature range: -40°C to 85°C
- Packaging (Pb free and Green)
  - TSSOP 28 (L)

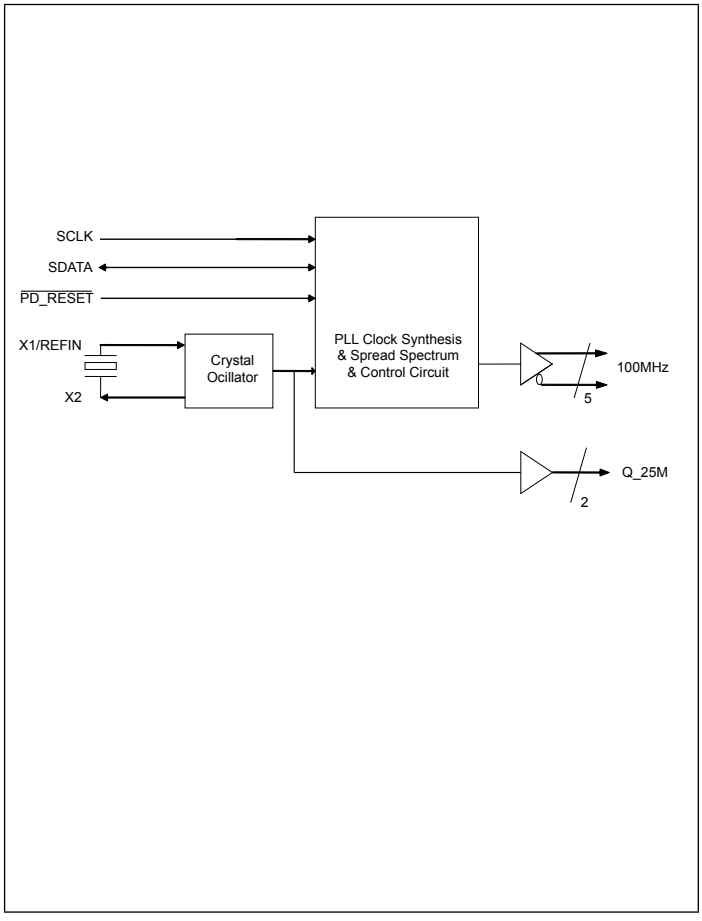
Description

The PI6C5572-05 is a high performance networking clock generator which generates PCIe 3.0/2.0/1.0 Compliant 100MHz HCSL clock signals along with two LVCMOS 25MHz clock from either 25MHz crystal or reference input. This integrated solution is ideal for Thunderbolt, Networking, Embedded systems and other systems that require PCIe 1.0, 2.0 and 3.0 HCSL signals and 25MHz clocks yet small foot print.

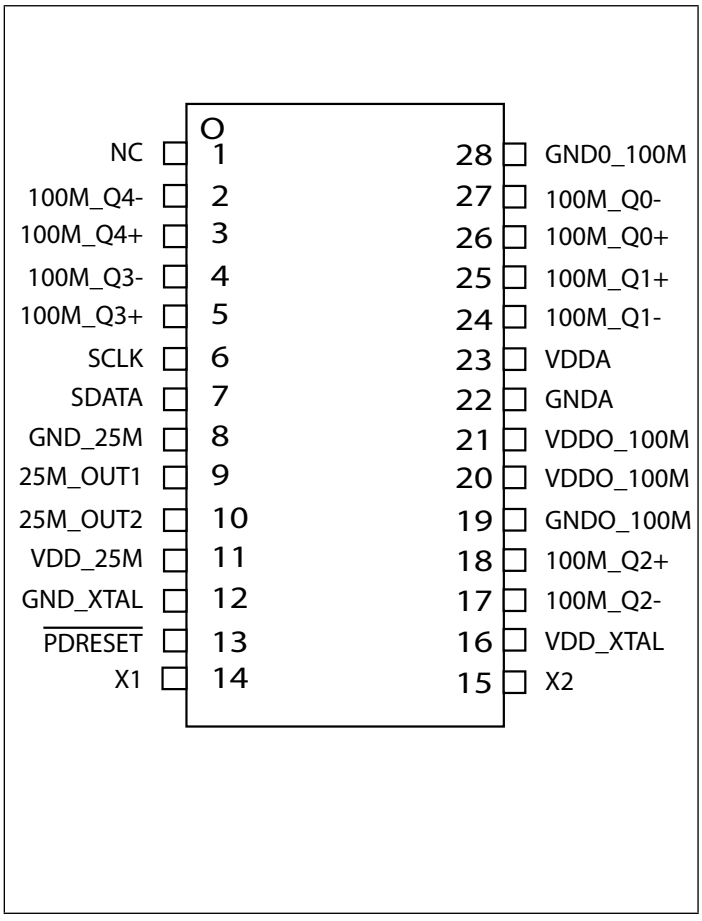
Applications

- Thunderbolt applications
- Networking systems
- Embedded systems
- Other systems

Block Diagram



Pin Configuration



Pin Description

Pin #	Pin Name	Pin Type	Pin Description
1	NC		
2	100M_Q4-	Output	100MHz HCSL output
3	100M_Q4+	Output	100MHz HCSL output
4	100M_Q3-	Output	100MHz HCSL output
5	100M_Q3+	Output	100MHz HCSL output
6	SCLK	Input	SMBus compatible input clock. Supports fast mode 400 kHz input clock
7	SDATA	I/O	SMBus compatible data line
8	GND_25M	Power	Ground for 25MHz output
9	25M_OUT1	Output	25MHz LVCMOS output. When disabled, output is trisated and has a normal 110kOhm pull-down
10	25M_OUT2	Output	25MHz LVCMOS output. When disabled, output is trisated and has a normal 110kOhm pull-down
11	VDD_25M	Power	3.3V supply for 25MHz output
12	GND_XTAL	Power	Ground for XTAL
13	$\overline{\text{PDRESET}}$	Input	Power on reset, when low all PLLs are powered down and output trisated. SMBus registers are reset to default values
14	X1	Input	Crystal input. Integrated 6pf capacitance
15	X2	Output	Crystal output. Integrated 6pf capacitance
16	VDD_XTAL	Power	3.3V supply for XTAL
17	100M_Q2-	Output	100MHz HCSL output
18	100M_Q2+	Output	100MHz HCSL output
19	GNDO_100M	Output	Ground for 100MHz output buffer
20	VDDO_100M	Power	3.3V supply for 100MHz output buffer
21	VDDO_100M	Power	3.3V supply for 100MHz output buffer
22	GNDA	Power	Ground for 100MHz related PLL
23	VDDA	Power	3.3V supply for 100MHz related PLL
24	100M_Q1-	Output	100MHz HCSL output
25	100M_Q1+	Output	100MHz HCSL output
26	100M_Q0+	Output	100MHz HCSL output
27	100M_Q0-	Output	100MHz HCSL output
28	GNDO_100M	Power	Ground for 100MHz output buffer

Serial Data Interface (SMBus)

PI6C5572-05 is a slave only SMBus device that supports indexed block read and indexed block write protocol using a single 7-bit address and read/write bit as shown below.

Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	0/1

How to Write

1 bit	8 bits	1	8 bits	1	8 bits	1	8 bits	1		8 bits	1	1 bit
Start bit	d2H	Ack	Register offset	Ack	Byte Count = N	Ack	Data Byte 0	Ack	…	Data Byte N - 1	Ack	Stop bit

Note:
1. Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

How to Read (M: abbreviation for Master or Controller; S: abbreviation for slave/clock)

1 bit	8 bits	1 bit	8 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit	…	8 bits	1 bit	1 bit
M: Start bit	M: Send "D2h"	S: sends Ack	M: send starting data-byte location: N	S: sends Ack	M: Start bit	M: Send "D3h"	S: sends Ack	S: sends # of data bytes that will be sent: X	M: sends Ack	S: sends starting data byte N	M: sends Ack	…	S: sends data byte N+X-1	M: Not Acknowledge	M: Stop bit

Byte 0: Spread Spectrum Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Spread Spectrum Selection for 100 MHz HCSL PCI-Express clocks	RW	0	All 100MHz HCSL PCI Express output	0=spread off 1 = -0.5% down spread
6	Enables hardware or software control of OE bits (see Byte 0–Bit 6 and Bit 5 Functionality table)	RW	0	$\overline{\text{PD\_RESET}}$ pin, bit 5	0 = hardware cntl 1 = software ctrl
5	Software $\overline{\text{PD\_RESET}}$ bit. Enables or disables all outputs (see Byte 0–Bit 6 and Bit 5 Functionality table)	RW	1	All outputs	0 = disabled 1 = enabled
4 to 1	Reserved	RW	Undefined	Not Applicable	
0	OE for 25M_Out2	RW	1	25M_Out2	0 = disabled 1 = enabled

Byte 0 - Bit 6 and Bit 5 Functionality

Bit 6	Bit 5	Description
0	X	$\overline{\text{PD\_RESET}}$ HW pin/signal = enabled
1	0	Disables all outputs and tri-states the outputs, $\overline{\text{PD\_RESET}}$ HW pin/signal = DO NOT CARE
1	1	Enable all outputs, $\overline{\text{PD\_RESET}}$ HW pin/signal = DON'T CARE

Byte 1: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Reserved	RW	Undefined	Not Applicable	
6	OE for 25M_Out1	RW	1	25M_Out1	0 = disabled 1 = enabled
5	Reserved	RW	Undefined	Not Applicable	
4	OE for 100M_Q4 HCSL output	RW	1	100M_Q4	0=disable 1 = enabled
3	Reserved	RW	Undefined	Not Applicable	
2	OE for 100M_Q3 HCSL output	RW	1	100M_Q3	0=disable 1 = enabled
1 to 0	Reserved	RW	Undefined	Not Applicable	

Byte 2: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7 to 5	Reserved	RW	Undefined	Not Applicable	
4 to 0	Reserved	R	Undefined	Not Applicable	

Byte 3: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	OE for 100M_Q2 HCSL Output	RW	1	100M_Q2	0 = disabled 1 = enabled
6 to 3	Reserved	RW	Undefined	Not Applicable	
2	OE for 100M_Q1 HCSL Output	RW	1	100M_Q1	0 = disabled 1 = enabled
1	OE for 100M_Q0 HCSL Output	RW	1	100M_Q0	0 = disabled 1 = enabled
0	Reserved	R	Undefined	Not Applicable	

Byte 4 & 5: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7 to 0	Reserved	R	Undefined	Not Applicable	

Byte 6: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Revision ID bit 3	R	1	Not Applicable	
6	Revision ID bit 2	R	0	Not Applicable	
5	Revision ID bit 1	R	0	Not Applicable	
4	Revision ID bit 0	R	0	Not Applicable	
3	Vendor ID bit 3	R	0	Not Applicable	
2	Vendor ID bit 2	R	0	Not Applicable	
1	Vendor ID bit 1	R	1	Not Applicable	
0	Vendor ID bit 0	R	1	Not Applicable	

Absolute Maximum Ratings[1] (Over operating free-air temperature range)

Parameters	Min.	Max.	Units
Storage Temperature	-65	150	°C
Ambient Temperature with Power Applied	-40	85	
3.3V Analog Supply Voltage	-0.5	4.6	V
ESD Protection (HBM)		2000	

Note:
1. Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

Symbol	Parameters	Test Condition	Min.	Typ.	Max.	Units
V_{DD}	Power supply		3.0	-	3.6	V
I_{DD}	Total Power Supply Current	All outputs unloaded	-	-	71	mA
$I_{DD\_Output\ Tri\text{-}stated}$	Total power supply current with tri-stated outputs	OE = "0", no load	-	-	42	mA
$I_{DD\ Power\text{-}Down}$	Total power supply current in power down mode	$\overline{PD\_RESET}$= "0", no load	-	-	3.8	mA
T_A	Operating temperature		-40	-	+85	°C

LVCMOS DC Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage		-0.3	-	0.8	
V_{OH}	Output High Voltage	I_{OH} = -8mA	V_{DD}-0.4	-	-	
V_{OL}	Output Low Voltage	I_{OL} = 8mA	-	-	0.4	
I_{IH}	Input High Current	V_{IN} = V_{DD} -0.1V	-	-	45	µA
I_{IL}	Input Low Current	V_{IN} = 0V	-45	-	-	
R_{PU}	Internal Pull-Up Resistance	$\overline{PDRESET}$	-	216	-	kOhm
R_{DN}	Internal Pull-Down Resistance	25M_OUT1, 25M_OUT2	-	110	-	

HCSL DC Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage		660	-	950	mV
V_{OL}	Output Low Voltage		-	-	150	
V_{CROSS}	Absolute Crossing Point Voltages		250	-	550	
ΔV_{CROSS}	Total variation of V_{CROSS} overall edges		-	-	140	

LVCMOS AC Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{in}	Input Frequency		-	25	-	MHz
F_{OUT}	Output Frequency	C_{LOAD} = 15pF	-	25	-	
T_r/T_f	Output Rise/Fall time	20% of V_{DD} to 80% of V_{DD}	-	-	1.35	ns
T_{DC}	Output Duty Cycle		45	-	55	%
T_j	Period Jitter	25 MHz clock output	-	-	90	ps

Electrical Characteristics - 100MHz Differential HCSL Outputs

Unless otherwise specified, V_{DD}=3.3V±5%, Ambient Temperature -40°C to +85°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Frequency					100	MHz
Cycle-to-Cycle Jitter	$T_{CC/Jitter}$				150	ps
Peak-to-Peak Phase Jitter		Using PCIe jitter measurement method			86	
PCIe 2.0 RMS Phase Jitter	$J_{RMS2.0}$	PCIe 2.0 Test Method @ 100MHz Output			3.1	ps
PCIe 3.0 RMS Jitter	$J_{RMS3.0}$	PLL L-BW @ 2M & 5M 1st H3			3	ps
		PLL H-BW @ 2M & 5M 1st H3			1	
Spread Modulation Percentage				-0.5	0	%
Spread Modulation Frequency				32		kHz
Duty Cycle	T_{DC}		45	50	55	%
Rising Edge Rate		Note 3, 4	0.6		4.0	V/ns
Falling Edge Rate		Note 3, 4	0.6		4.0	V/ns
Rise-Fall Matching		Note 3, 11			20%	
Output Skew	T_{OSKEW}	V_T = 50%(measurement threshold)			70	ps
High-Level Output Voltage	V_{OH}	Note 2, (R_S=33-Ohm)	0.65	0.71	0.85	V
Low-Level Output Voltage	V_{OL}		–0.20	0	0.05	
Absolute Crossing Point Voltage	V_{CROSS}	Note 2, 5, 6	0.25		0.55	V
Variation of VCROSS over all rising clock edges	$V_{CROSS\ Delta}$	Note 2, 5, 8			140	mV
Average Clock Period Accuracy	$T_{PERIOD\ AVG}$	Note 3, 9, 10	–300		2800	ppm
Absolute Period (including jitter and spread spectrum)	$T_{PERIOD\ ABS}$	Note 3, 7	9.847		10.203	ns

Notes:

1. Measured at the end of an 8-inch trace with a 5pF load.
2. Measurement taken from a single-ended waveform.
3. Measurement taken from a differential waveform.
4. Measured from -150 mV to +150 mV on the differential waveform. The signal is monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.
5. Measured at crossing point where the instantaneous voltage value of the rising edge of 100M+ equals the falling edge 100M–.
6. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
7. Defines as the absolute minimum or maximum instantaneous period. This includes cycle-to-cycle jitter, relative PPM tolerance, and spread spectrum modulation.
8. Defined as the total variation of all crossing voltages of rising 100M+ and falling 100M–.
9. Refer to section 4.3.2.1 of the PCI Express Base Specification, Revision 1.1 for information regarding PPM considerations.
10. PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100 MHz exactly or 100 Hz. For 300 PPM there is an error budget of 100Hz/PPM * 300 PPM = 30 kHz. The period is measured with a frequency counter with measurement window set at 100 ms or greater. With spread spectrum turned off the error is less than ±300 ppm. With spread spectrum turned on there is an additional +2500 PPM nominal shift in maximum period resulting from the -0.5% down spread.
11. Matching applies to rising edge rate for PCIe and falling edge rate for PCIeN. It is measured using a ±75 mV window centered on the median cross point where PCIe rising meets PCIeN falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rising edge rate of PCIe should be compared to the falling edge rate of PCIeN. The maximum allowed difference should not exceed 20% of the slowest edge rate.

PCI-Express Layout Guidelines

Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure	Notes
L1 length, Route as non-coupled 50 ohm trace.	0.5 max	inch	1,2	
L2 length, Route as non-coupled 50 ohm trace.	0.2 max	inch	1,2	
L3 length, Route as non-coupled 50 ohm trace.	0.2 max	inch	1,2	
R_S	33	ohm	1,2	

Down Device Differential Routing	Dimension or Value	Unit	Figure	Notes
L4 length, Route as coupled microstrip 100 ohm differential trace.	2 min to 16 max	inch	1	
L4 length, Route as coupled stripline 100 ohm differential trace.	1.8 min to 14.4 max	inch	1	

Figure 1: Down Device Routing

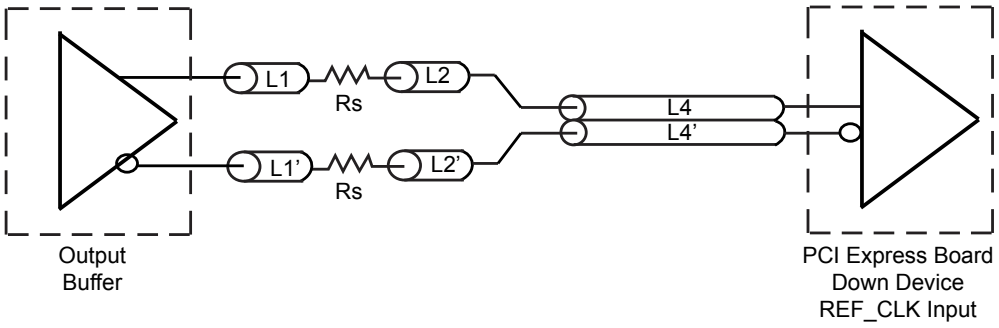
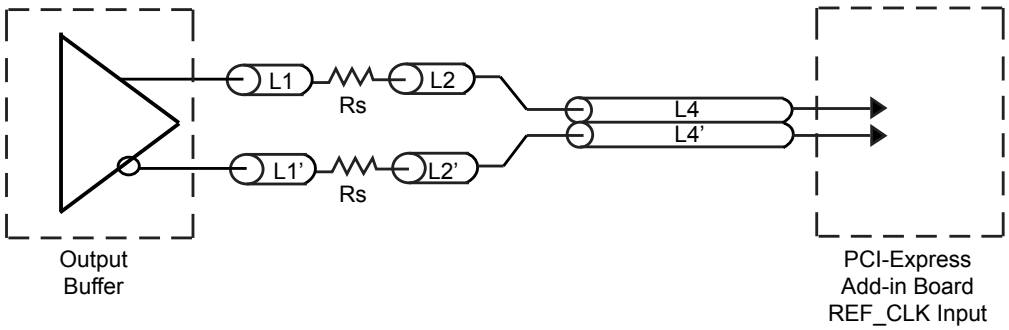


Figure 2: PCI-Express Connector Routing



Configuration test load board termination for HCSL Outputs

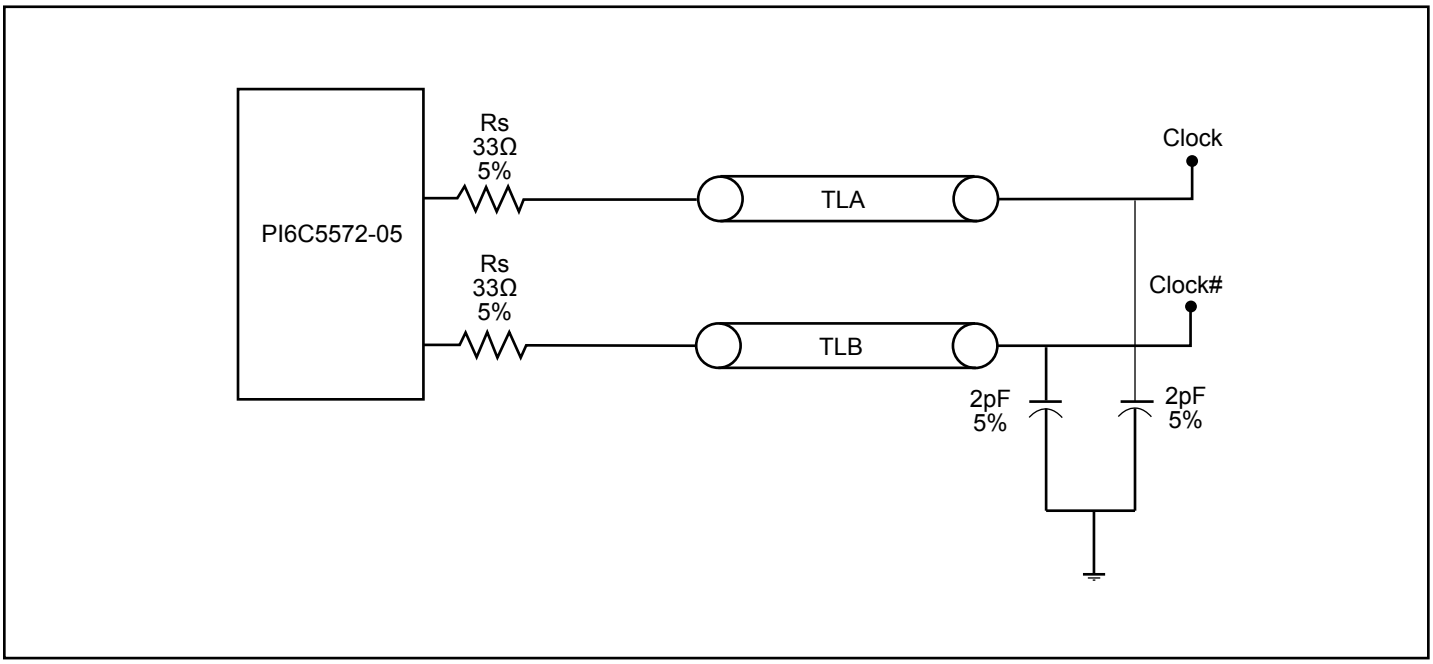
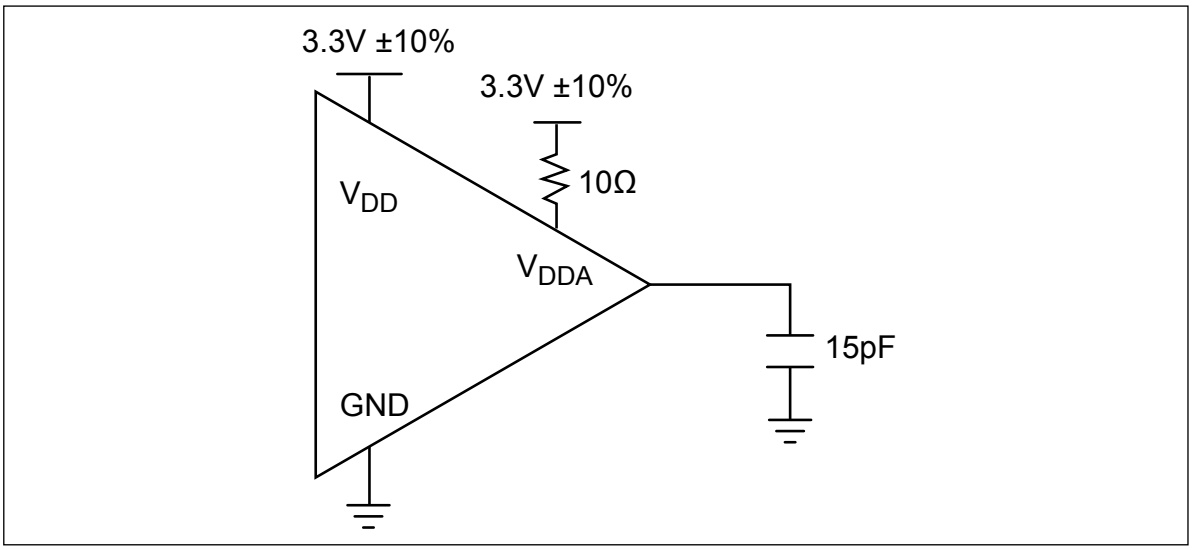


Figure 4. Configuration Test Load Board Termination

LVCMOS Test Circuit

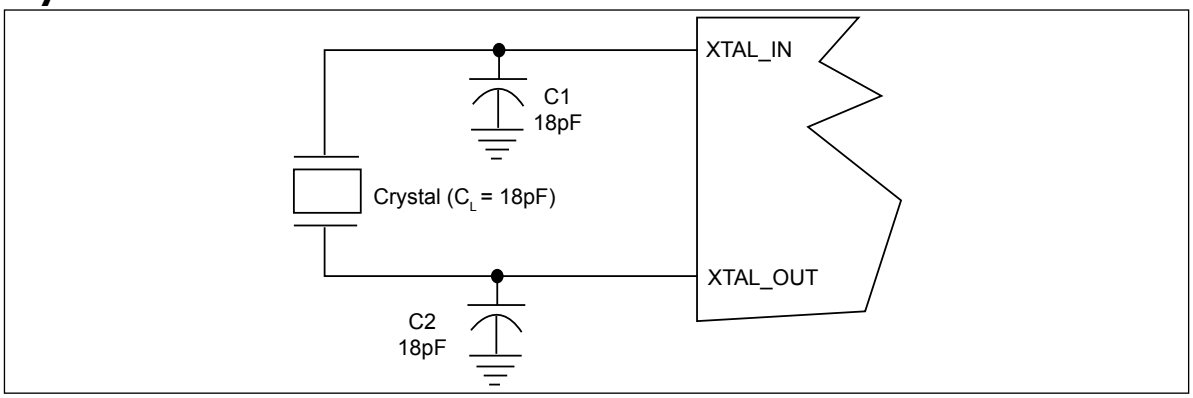


Application Notes

Crystal circuit connection

The following diagram shows PI6C5572-05 crystal circuit connection with a parallel crystal. For the CL=18pF crystal, it is suggested to use C1= 18pF, C2= 18pF. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts.

Crystal Oscillator Circuit



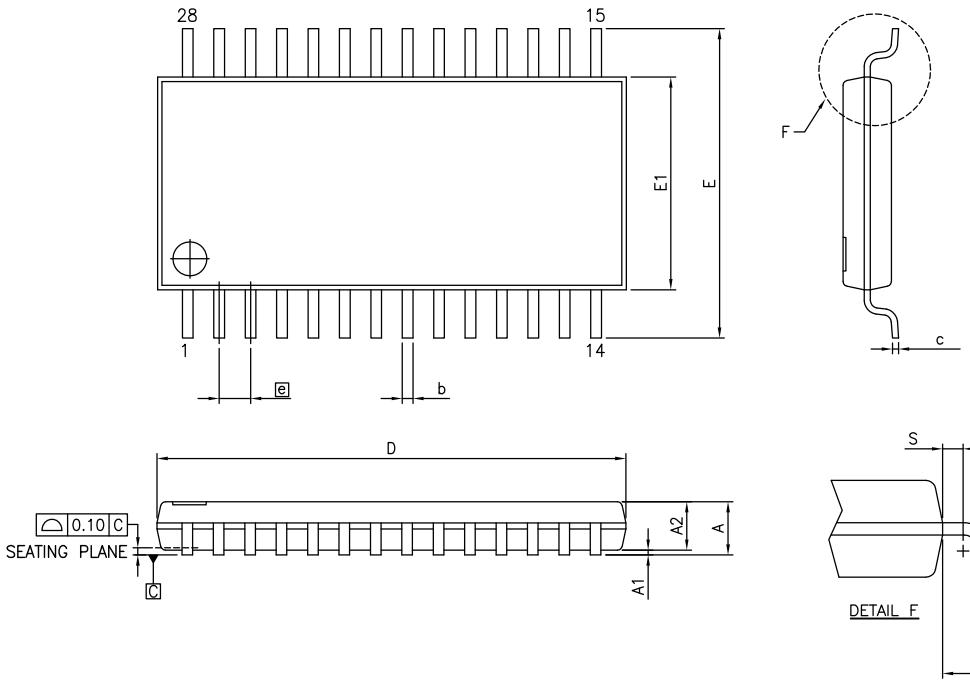
Recommended Crystal Specification

Pericom recommends:

a) GC2500003 XTAL 49S/SMD(4.0 mm), 25M, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/GC_GF.pdf

b) FY2500081, SMD 5x3.2(4P), 25M, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf

c) FL2500047, SMD 3.2x2.5(4P), 25M, CL=18pF, +/-20ppm, http://www.pericom.com/pdf/datasheets/se/FL.pdf



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	9.60	9.70	9.80
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

Notes:
1. Refer JEDEC: MO-153F/AE
2. Controlling dimensions in millimeters
3. Package outline exclusive of mold flash and metal burr

PERICOM Enabling Serial Connectivity

DATE: 05/03/12

DESCRIPTION: 28 pin, 173mil wide, TSSOP

PACKAGE CODE: L

DOCUMENT CONTROL #: PD-1313 **REVISION: E**

12-0375

Note:
- For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information(1-3)

Ordering Code	Package Code	Package Description
PI6C5572-05LIE	L	28 pin, Pb-free & Green, TSSOP (L28)

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel