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National Semiconductor

May 1991

CGS74B2525 • CGS74B2526
1-to-8 Minimum Skew Clock Driver

General Description

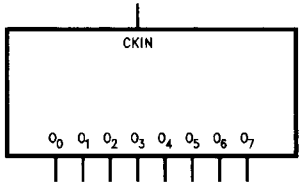
These minimum skew clock drivers are designed for Clock Generation and Support (CGS) applications operating well above 20 MHz (33 MHz, 50 MHz). The devices guarantee minimum output skew across the outputs of a given device and also from device-to-device. Skew parameters are also provided as a means to measure duty cycle requirements as those found in high speed clocking systems. The 'B2525 is a minimum skew clock driver with one input driving eight outputs specifically designed for signal generation and clock distribution applications. The 'B2526 is similar to the 'B2525 but contains a multiplexed clock input to allow for systems with dual clock speeds or systems where a separate test clock has been implemented.

Features

- Clock Generation and Support (CGS) Devices—Ideal for high frequency signal generation or clock distribution applications
- CGS74B version features National's Advanced Bipolar FAST® LSI process
- 1-to-8 low skew clock distribution
- Sub 1 ns pin-to-pin output skew
- Specifications for device-to-device variation of propagation delay
- Specification for transition skew to meet duty cycle requirements
- Multiplexed clock input ('B2526)
- 14- and 16-center pin V_{CC} and GND configuration to minimize high speed switching noise
- Current sourcing 48 mA and current sinking of 64 mA
- Low dynamic power consumption above 20 MHz
- Guaranteed 4 kV ESD protection

Logic Symbols

'B2525



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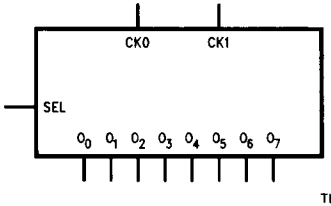
'B2526



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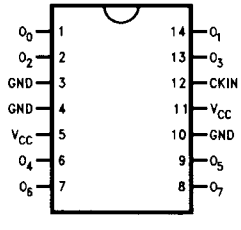
Connection Diagrams

Pin Assignment for DIP and SOIC

'B2525



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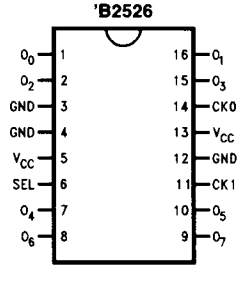
'B2526



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Functional Description

On the multiplexed clock device, the SEL pin is used to determine which CK_n input will have an active effect on the outputs of the circuit. When SEL = 1, the CK_1 input is selected and when SEL = 0, the CK_0 input is selected. The non-selected CK_n input will not have any effect on the logical output level of the circuit. The output pins act as a single entity and will follow the state of the CK_{IN} or CK_1/CK_0 pins when either the multiplexed ('B2526) or the straight ('B2525) clock distribution chip is selected.

Pin Description

Pin Names	Description
CK_{IN}	Clock Input ('B2525)
CK_0, CK_1	Clock Inputs ('B2526)
O_0–O_7	Outputs
SEL	Clock Select ('B2526)

Truth Tables

'B2525

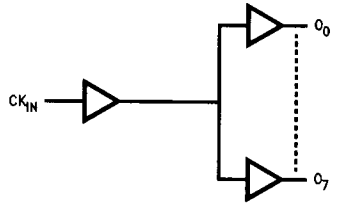
Inputs	Outputs
CK_{IN}	O_1–O_7
L	L
H	H

'B2526

Inputs			Outputs
CK_0	CK_1	SEL	O_1–O_7
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

L = Low Voltage Level
H = High Voltage Level
X = Immaterial

'B2525



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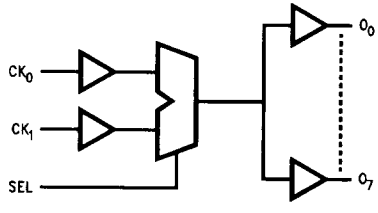
'B2526



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})			7.0V
Input Voltage (V_I)			7.0V
Operating Free Air Temperature			0°C to +70°C
Storage Temperature Range			−65°C to +150°C
Typical θ_{JA}	'B2525	'B2526	
Plastic (N) Package	104	92	°C/W
Jedec SOIC (M) Package	120	126	°C/W

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage—High (V_{IH})	2.0V
Input Voltage—Low (V_{IL})	0.8V
High Level Output Current (I_{OH})	−48 mA
Low Level Output Current (I_{OL})	+64 mA
Free Air Operating Temperature (T_A)	0°C to +70°C

Note 2: Plastic SOIC packaging meets 2000 temperature cycles from −40° to +125° C.

DC Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −3 mA, V_{CC} = 4.5V		2.4			
		I_{OH} = −48 mA, V_{CC} = 4.5V		2.0			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 64 mA			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IH} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−50		−150	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		8	15	mA
			Outputs Low		32	42	mA
C_{IN}	Input Capacitance	V_{CC} = 5V			5		pF

AC Electrical Characteristics

Symbol	Parameter	CGS74B			Units
		V_{CC} = 4.5V to 5.5V R_L = 500Ω, C_L = 50 pF			
		Min	Typ	Max	
t_{PLH}	Propagation Delay CK to O_n ('2525)	2	2.9	4.8	ns
t_{PHL}		2	3.0	4.8	
t_{PLH}, t_{PHL}	Propagation Delay CK_n to O_n ('2526)				ns

See *Figures 1–6* for frequency, loading and airflow curves.

Extended AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	CGS74B $R_L = 500\Omega$, $C_L = 50$ pF, $T_A = 0°C$ to $70°C$			Units
			Min	Typ	Max	
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	5.0		0.15	1	ns
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	5.0		0.15	1	ns
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation (Note 1)	5.0		0.7	1.5	ns
t_{PV}	Maximum Skew Part-to-Part Variation Skew (Note 2)	5.0			1.75	ns
t_{PS}	Maximum Skew Pin (Signal) Transition Variation (Note 1)	5.0		0.6	1.5	ns
t_{rise}, t_{fall}	Maximum Rise/Fall Time (from 0.5/2.4V to 2.4/0.5V at 33 MHz, $T_A = 25°C$)	5.0 5.0		1.90 1.15		ns ns

*Voltage Range 5.0 is 5.0V ±0.5V

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design. See *Figures A, B,* and *C* of Parameter Measurement Information.

Note 2: Part-to-part skew is defined as the absolute value of the difference between the propagation delay for any outputs from device to device. The parameter is specified for a given set of conditions (i.e., capacitive load, V_{CC}, temperature, # of outputs switching, etc.). Parameter guaranteed by design. See *Figure D* of Parameter Measurement Information.

See *Figures 1–6* for frequency, loading, and airflow curves.

Typical Performance Characteristics

f_{MAX} vs Capacitive Load

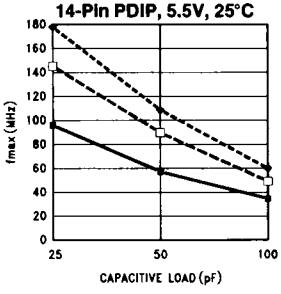

FIGURE 1

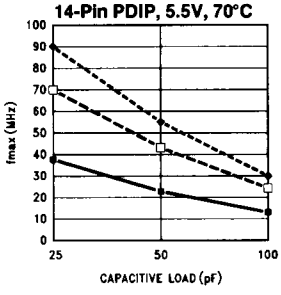

FIGURE 2

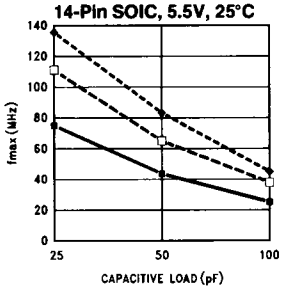

FIGURE 3

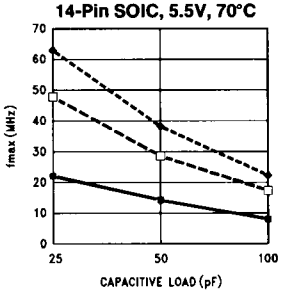

FIGURE 4

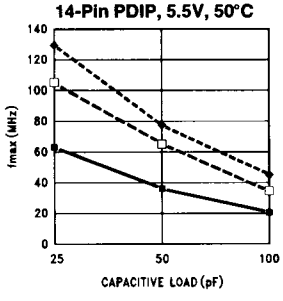

FIGURE 5

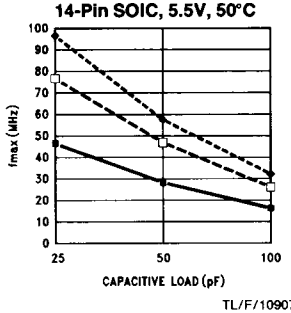

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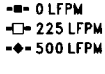
FIGURE 6



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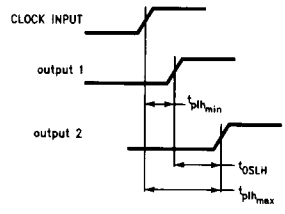
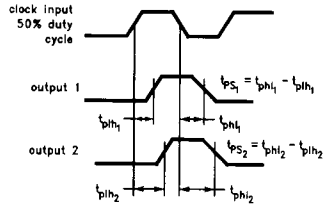
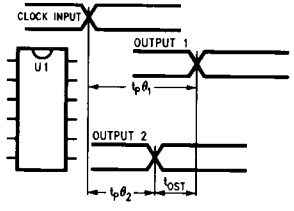
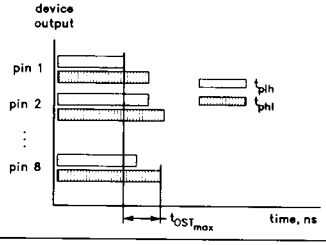
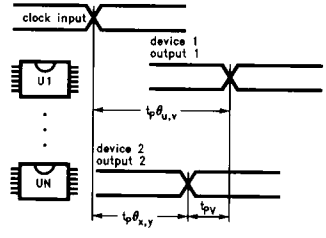
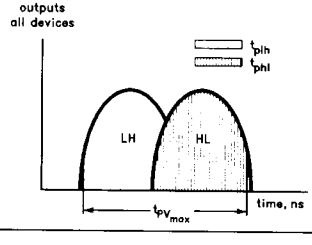
Note 1: Values of f_{max} were chosen to maintain 150°C die temperature. In all cases, the values represent worst case performance.

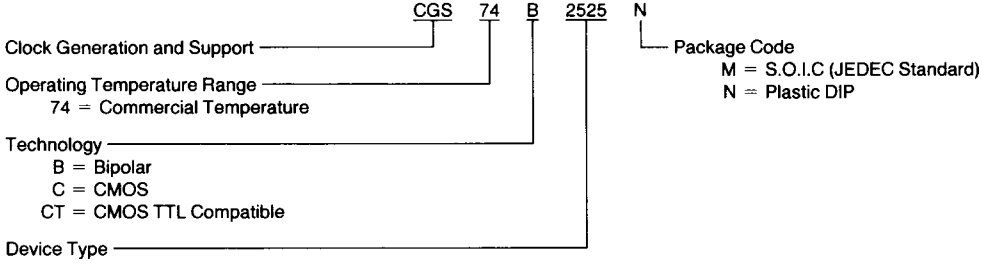
Minimum Skew Parameters

Parameter Measurement Information (Preliminary)

Definition	Example	Significance
t_{OSHL}, t_{OSLH} **Common Edge Skew:** Output Skew for HIGH-to-LOW Transitions: $t_{OSHL} = \lvert t_{PHL_{max}} - t_{PHL_{min}} \rvert$ Output Skew for LOW-to-HIGH Transitions: $t_{OSLH} = \lvert t_{PLH_{max}} - t_{PLH_{min}} \rvert$ Propagation delays are measured across the outputs of any given device.	 **FIGURE A**	• t_{OS}, Output Skew or Common Edge Skew • Skew parameter to observe propagation delay differences in applications requiring synchronous data/clock operations.
t_{PS} **Pin Skew or Transition Skew:** $t_{PS} = \lvert t_{PHL_i} - t_{PLH_i} \rvert$ Both HIGH-to-LOW and LOW-to-HIGH propagation delays are measured at each output pin across the given device. T_{PS} is the maximum difference for outputs i = 1 to 8 within a device package.	 **FIGURE B**	• t_{PS}, Pin Skew or Transition Skew • Skew parameter to observe duty cycle degradation of any output signal (pin).
t_{OST} **Opposite Edge Skew:** $t_{OST} = \lvert t_P\theta_m - t_P\theta_n \rvert$ where θ is any edge transition (HIGH-to-LOW or LOW-to-HIGH) measured between any two outputs (m or n) within any given device.	 **FIGURE C**	• t_{OST}, Any Edge Skew • Skew parameter to observe performance distribution of propagation delays across the outputs within any given device. 
t_{PV} **Part Variation Skew:** $t_{PV} = \lvert t_P\theta_{u,v} - t_P\theta_{x,y} \rvert$ where θ is any edge transition (HIGH-to-LOW or LOW-to-HIGH propagation delay) measured from the outputs (v or y) of any two devices (u or x).	 **FIGURE D**	• t_{PV}, Part Variation Skew • Skew parameter to observe performance distribution of propagation delays between the outputs of any two devices. 

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

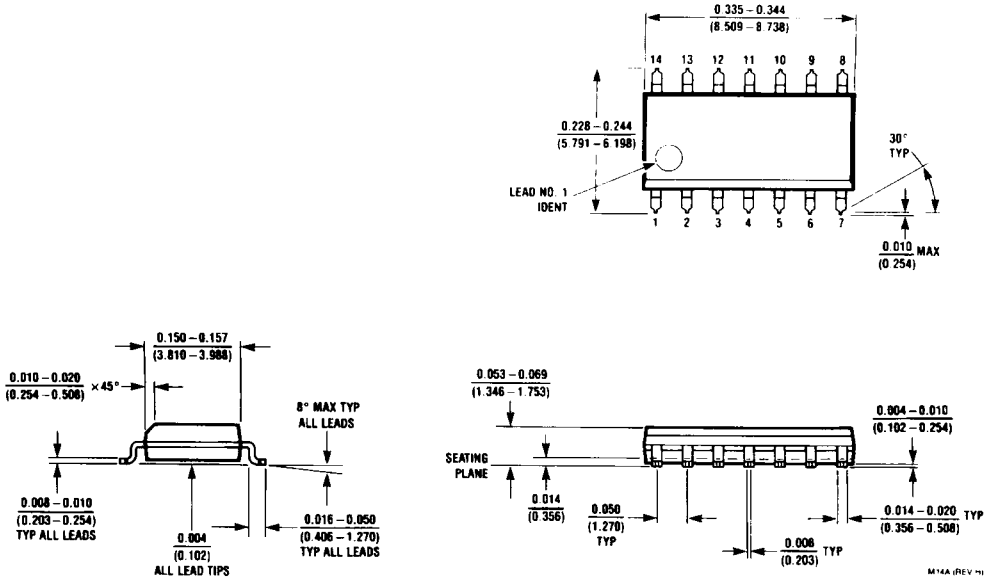


Temperature Information

	Technology	Temperature Range†		
		74-Grade	64-Grade	54-Grade
TTL/CMOS	Bipolar	0°C to 70°C	−40°C to +85°C	−55°C to +125°C
	CMOS	−40°C to +85°C	N/A	−55°C to +125°C
	CMOS/TTL Compatible	−40°C to +85°C	N/A	−55°C to +125°C
	BiCMOS	0°C to +70°C	−40°C to +85°C	−55°C to +125°C

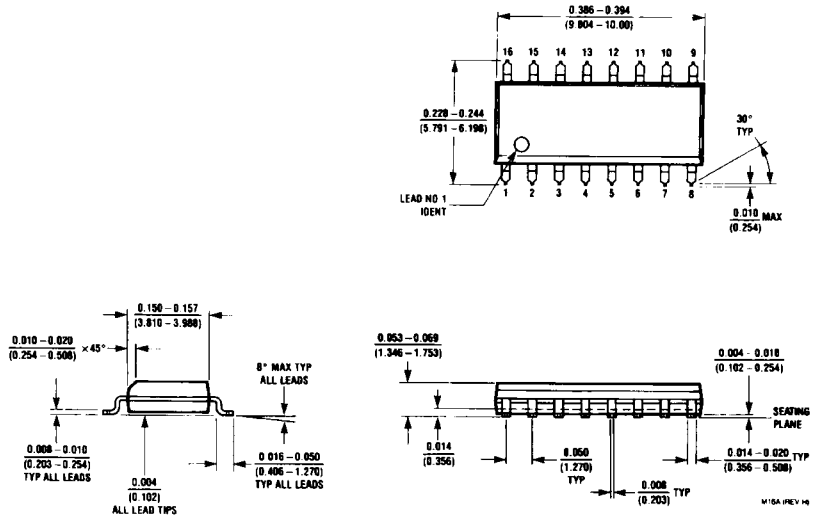
†Typically, 64- and 74-grade are commercial products; and 54-grade may or may not be a Mil/Aero product.

Physical Dimensions inches (millimeters)

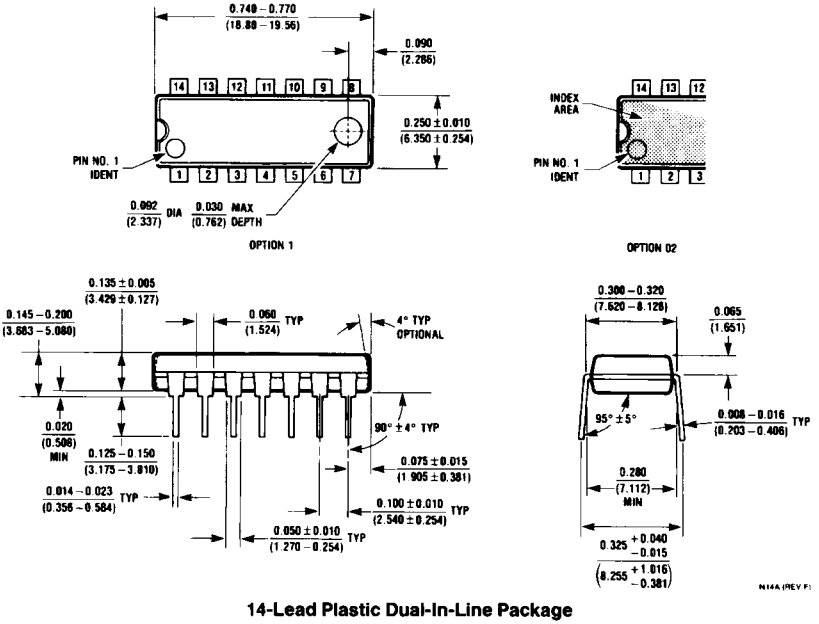


14-Lead Small Outline Integrated Circuit
NS Package Number M14A

Physical Dimensions inches (millimeters) (Continued)

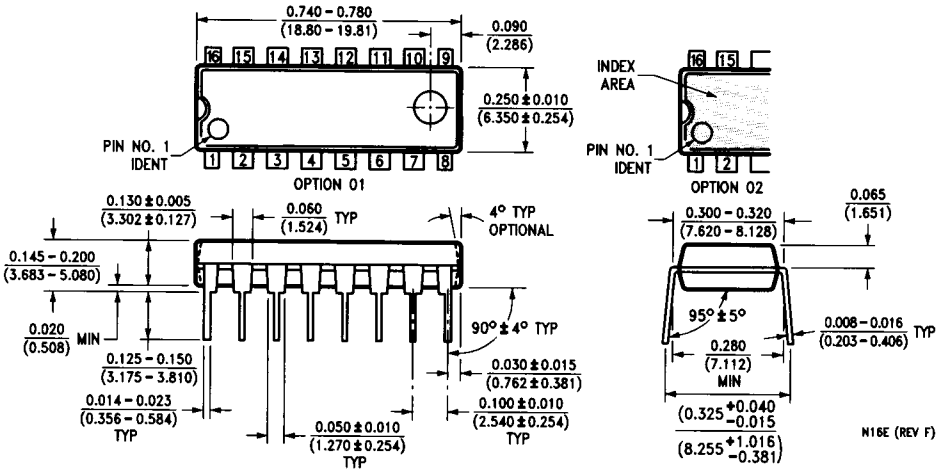


16-Lead Small Outline Integrated Circuit
NS Package Number M16A



14-Lead Plastic Dual-In-Line Package
NS Package Number N14A

Physical Dimensions inches (millimeters) (Continued)



16-Lead Plastic Dual-In-Line Package
NS Package Number N16E

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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