



High-Speed CMOS 3.3V 16-Bit Latched Transceiver with Output Resistor

QS74LVCH16543A

FEATURES/BENEFITS

- 5V tolerant inputs and outputs
- Bus Hold feature holds last active state during 3-state operation
- 10 μ A I_{CCQ} quiescent power supply current
- Hot insertable
- 2.0V–3.6V V_{CC} supply operation
- ± 24 mA balanced output drive
- Power down high impedance inputs and outputs
- Input hysteresis for noise immunity
- Meets or exceeds JEDEC Standard 36 specifications
- Multiple power and ground pins for low noise
- Operating temperature range:
–40°C to 85°C
- Latch-up performance exceeds 500mA
- ESD performance:
Human body model > 2000V
Machine model > 200V
- Packages available:
56-pin TSSOP
56-pin SSOP

DESCRIPTION

The LVCH16543A is a 16-bit latched bus transceiver with three-state outputs that is ideal for driving address and data buses. Two independent 8-bit D-type latched transceivers are used with separate input and output control to permit independent control of data flow in either direction. The QS74LVCH16543A provides Bus Hold circuitry on the data inputs to retain the last active state during 3-state operation, eliminating the need for external pull-up resistors. The 3.3V LVC family features low power, low switching noise, and fast switching speeds for low power portable applications as well as high-end advanced workstation applications. 5V tolerant inputs and outputs allow this LVC product to be used in mixed 5V and 3.3V applications. Easy board layout is facilitated by the use of flow-through pinouts and byte enable controls provide architectural flexibility for systems designers. To accommodate hot-plug or live insertion applications, this product is designed not to load an active bus when V_{CC} is removed.

Figure 1. Functional Block Diagram

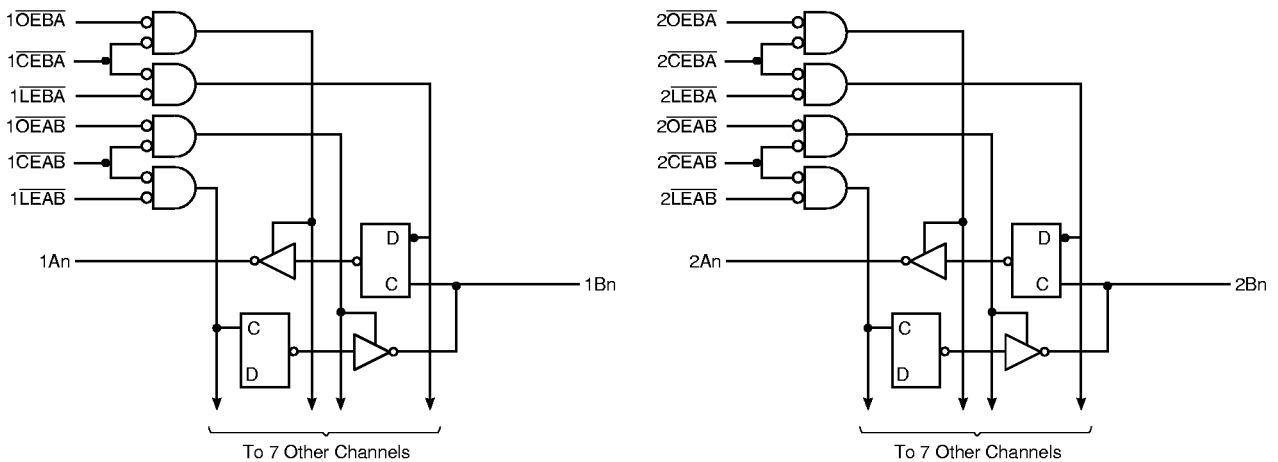


Figure 2. Pin Configuration
(All Pins Top View)

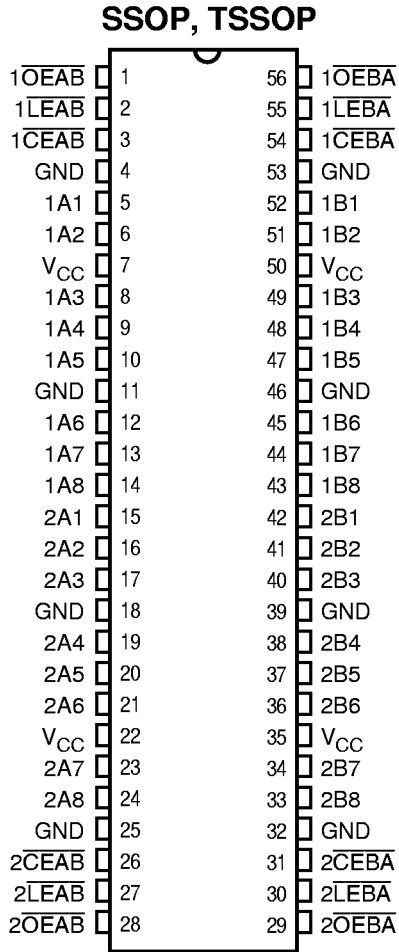


Table 1. Pin Description

Name	Description
\overline{xOEAB}	A to B Output Enable Inputs (Active LOW)
\overline{xOEBA}	B to A Output Enable Inputs (Active LOW)
\overline{xCEAB}	A to B Enable Inputs (Active LOW)
\overline{xCEBA}	B to A Enable Inputs (Active LOW)
\overline{xLEAB}	A to B Latch Enable Inputs (Active LOW)
\overline{xLEBA}	B to A Latch Enable Inputs (Active LOW)
xAx	A to B Data Inputs or B to A 3-State Outputs (Bus Hold Inputs)
xBx	B to A Data Inputs or A to B 3-State Outputs (Bus Hold Inputs)

Table 2. Function Table

Inputs		Status	Latch Buffers	Output
\overline{xCEAB}	\overline{xLEAB}	\overline{xOEAB}	xAx to xBx	xBx
H	X	X	Storing	High-Z
X	H	X	Storing	X
X	X	H	X	High-Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

Notes:

- * = Before \overline{xLEAB} LOW-to-HIGH Transition
 H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
- A-to-B data flow shown: B-to-A flow control is the same, except using \overline{xCEBA} , \overline{xLEBA} , \overline{xOEBA}

Table 3. Absolute Maximum Ratings

Supply Voltage to Ground	-0.5V to 7.0V
DC Output Voltage V_{OUT}	
Outputs HIGH-Z	-0.5V to 7.0V
Outputs Active	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage V_{IN}	-0.5V to 7.0V
DC Input Diode Current with $V_{IN} < 0$	-50mA
DC Output Diode Current	
$V_O < 0$	-50mA
$V_O > V_{CC}$	50mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	$\pm 50mA$
DC Supply Current per Supply Pin	$\pm 100mA$
DC Ground Current per Ground Pin	$\pm 100mA$
T_{STG} Storage Temperature	-65°C to 150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

Table 4. Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit	
V_{CC}	Supply Voltage, Operating	2.0	3.6	V	
	Supply Voltage, Data Retention Only	1.5	3.6		
V_{IH}	Input HIGH Voltage	2.0	—	V	
V_{IL}	Input LOW Voltage	—	0.8	V	
V_{IN}	Input Voltage	0	5.5	V	
V_{OUT}	Output Voltage in Active State	0	V_{CC}	V	
	Output Voltage in "OFF" State	0	5.5		
I_{OH}	Output Current HIGH	$V_{CC} = 3.0-3.6V$	—	-24	mA
		$V_{CC} = 2.7V$		-12	
I_{OL}	Output Current LOW	$V_{CC} = 3.0-3.6V$	—	24	mA
		$V_{CC} = 2.7V$	—	12	
$\Delta t/\Delta v$	Input Transition Slew Rate	—	10	ns/V	
T_A	Operating Free Air Temperature	-40	85	°C	

Table 5. DC Electrical Characteristics Over Operating Range

Industrial Temperature Range, $T_A = -40^{\circ}\text{C}$ to 85°C

Symbol	Parameter	Test Conditions	Min	Typ ⁽¹⁾	Max	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = 2.7\text{V}, I_{OH} = -100\mu\text{A}$ $V_{CC} = 2.7\text{V}, I_{OH} = -12\text{mA}$ $V_{CC} = 3.0\text{V}, I_{OH} = -12\text{mA}$ $V_{CC} = 3.0\text{V}, I_{OH} = -24\text{mA}$	$V_{CC} - 0.2$ 2.2 2.4 2.2	— — — —	— — — —	V
V_{OL}	Output LOW Voltage	$V_{CC} = 2.7\text{V}, I_{OL} = 100\mu\text{A}$ $V_{CC} = 2.7\text{V}, I_{OL} = 12\text{mA}$ $V_{CC} = 3.0\text{V}, I_{OL} = 24\text{mA}$	— — —	— — —	0.2 0.4 0.55	V
V_{IK}	Input Clamp Voltage	$V_{CC} = 2.7\text{V}, I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V
I_I	Input Leakage Current	$V_I = 0\text{V}, V_I = 5.5\text{V}, V_{CC} = 3.6\text{V}$	—	—	± 1.0	μA
$ I_{BH} $	Bus Hold Inputs Overdrive Current ^(2,3)	$V_{CC} = 3.6\text{V}, V_{IN} = 0\text{V}$ or $V_{IN} = V_{CC}$	—	—	50	μA
		$V_{CC} = 3.6\text{V}, 0.8\text{V} < V_{IN} < 2.0\text{V}$	—	—	500 ⁽⁴⁾	
I_{BHH} I_{BHL}	Bus Hold Input Sustaining Current	$V_{CC} = 3\text{V}$	$V_{IN} = 2.0\text{V}$	-75	—	μA
			$V_{IN} = 0.8\text{V}$	75	—	
I_{OZ}	High-Z I/O Leakage	$V_O = 0\text{V}, V_O = 5.5\text{V},$ $V_I = V_{IH}$ or $V_{IL}, V_{CC} = 3.6\text{V}$	—	—	± 1.0	μA
I_{OFF}	Power Off Leakage	$V_{CC} = 0\text{V}, V_I$ or $V_O = 5.5\text{V}$	—	—	10	μA
I_{CC}	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}, V_{IN} = V_{CC}$ or GND	—	0.1	10	μA
ΔI_{CC}	Quiescent Power Supply Current per Control Inputs at TTL HIGH	$V_{CC} = 3.6\text{V}, V_{IN} = V_{CC} - 0.6\text{V}^{(5)}$	—	2.0	3.0	μA
	Quiescent Power Supply Current per Bus Hold Inputs at TTL HIGH	$V_{CC} = 3.6\text{V}, V_{IN} = V_{CC} - 0.6\text{V}^{(5)}$	—	75	500	μA

Notes:

1. Typical values are at $V_{CC} = 3.3\text{V}$ and $T_A = 25^{\circ}\text{C}$.
2. These parameters are guaranteed by characterization, but not production tested.
3. Pins with Bus Hold are identified in the pin description.
4. An external driver must provide at least $|I_{BH}|$ during transition to guarantee that the Bus Hold input will change state.
5. Per TTL driven input. All other inputs at V_{CC} or GND.

Table 6. Dynamic Switching Characteristics

Symbol	Parameter	Test Conditions	Typ ⁽¹⁾	Unit	
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 50pF, V _{CC} = 3.3V V _{IH} = 3.3V, V _{IL} = 0V	0.8	V	
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 50pF, V _{CC} = 3.3V V _{IH} = 3.3V, V _{IL} = 0V	0.8	V	
C _{PD}	Power Dissipation	C _L = 50pF, f = 10MHz, V _{CC} = 3.3 ±0.3V	Output Enable	25	pF
			Output Disable	4	

Note:

1. Typical values are at V_{CC} = 3.3V, 25°C ambient.

Table 7. Capacitance⁽¹⁾

Symbol	Pins	Conditions	Typ	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V, V _{OUT} = 0V, f = 1MHz	7.0	pF
C _{I/O}	I/O Capacitance	V _{IN} = 0V, V _{OUT} = 0V, f = 1MHz	8.0	pF

Note:

1. Capacitance is characterized but not production tested.

Table 8. Switching Characteristics Over Operating Range

Industrial Temperature Range, T_A = -40°C to 85°C.

C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description ⁽¹⁾	V _{CC} = 3.3 ±0.3V		V _{CC} = 2.7V ⁽²⁾		Unit
		Min	Max	Min	Max	
t _{PD}	Propagation Delay Transparent Mode xAx to xBx or xBx to xAx	1.5	5.4	1.5	6.1	ns
	Propagation Delay xLEBA to xAx, xLEAB to xBx	1.5	6.1	1.5	7.4	ns
t _{EN}	Output Enable Time xOEBA or xOEAB to xAx or xBx, xCEBA or xCEAB to xAx or xBx	1.5	6.3	1.5	7.6	ns
t _{DIS}	Output Disable Time ⁽²⁾ xOEBA or xOEAB to xAx or xBx, xCEBA or xCEAB to xAx or xBx	1.5	6.3	1.5	6.9	ns
t _{SU}	Setup Time HIGH or LOW xAx or xBx to xLEBA or xLEAB	1.1	—	1.1	—	ns
t _H	Hold Time HIGH or LOW xAx or xBx to xLEBA or xLEAB	1.9	—	1.9	—	ns
t _W	Pulse Width LOW ⁽²⁾	3.3	—	3.3	—	ns
t _{SK(O)}	Output Skew ⁽³⁾	—	0.5	—	—	ns

Notes:

1. Minimums guaranteed but not tested. See Test Circuit and Waveforms.
2. Guaranteed by characterization.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by characterization but not production tested.

TEST CIRCUIT AND WAVEFORMS

Figure 3. Test Circuit

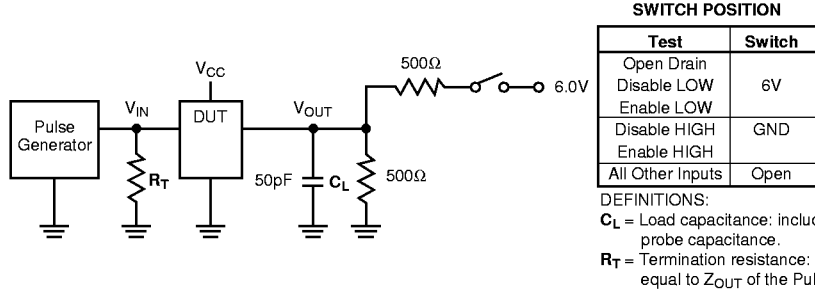


Figure 4. Setup, Hold, and Release Timing

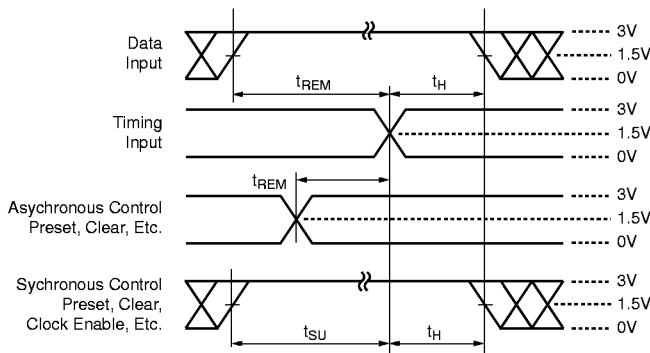


Figure 6. Pulse Width

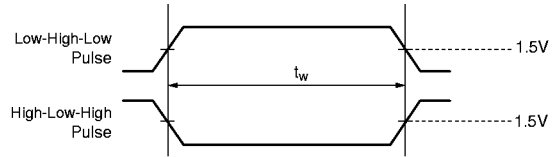


Figure 5. Enable and Disable Timing

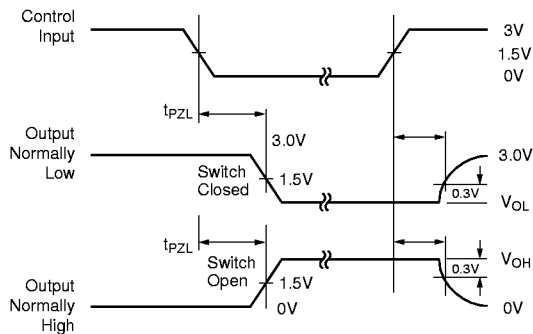
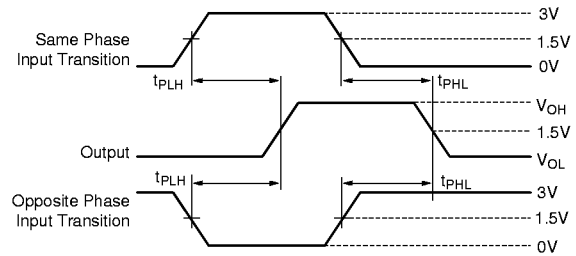


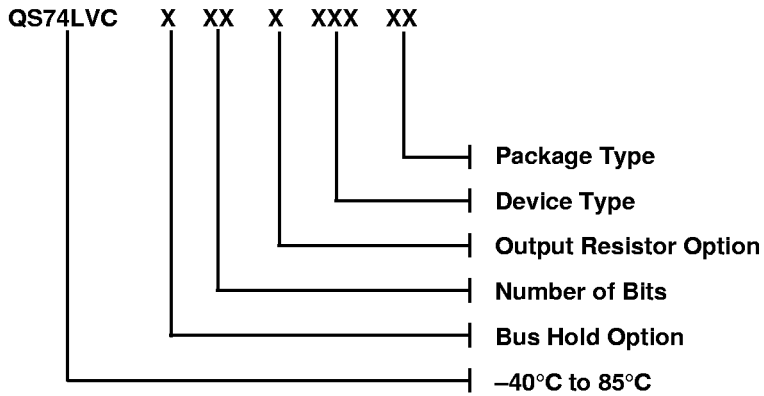
Figure 7. Propagation Delay



Notes:

1. Input Control Enable = LOW and Input Control Disable = HIGH.
2. Pulse Generator for All Pulses: Rate \leq 1.0MHz;
 $Z_{OUT} \leq 50\Omega$; $t_F, t_R \leq 2.5ns$.

ORDERING INFORMATION



Bus Hold Option:
H – with Bus Hold

Number of Bits:
16 – 16-Bit

Output Resistor Option:
Blank – No Output Resistor

Device Type:
543

Package Type:
PV – SSOP, 300 mil
PA – TSSOP, 240 mil