INTERSIL

# LF155, LF255, LF355, LF156, LF256, LF356, LF157, LF257, LF357

# Monolithic JFET Input Operational Amplifiers

## COMMON FEATURES

(LF155A, LF156A, LF157A)

- Low input bias current — 30 pA
- Low Input Offset Current — 3 pA
- High input impedance — $10^{12}\Omega$
- Low input offset voltage — 1 mV
- Low input offset voltage temperature drift — $3\mu V/^{\circ}C$
- Low input noise current — 0.01 $pA/\sqrt{Hz}$
- High common-mode rejection ratio — 100 dB
- Large dc voltage gain — 106 dB

## UNCOMMON FEATURES

| | LF155A | LF156A | LF157A ($A_V$=5) | UNITS |
|---|---|---|---|---|
| • Extremely fast settling time to 0.01% | 4 | 1.5 | 1.5 | $\mu s$ |
| • Fast slew rate | 5 | 12 | 50 | $V/\mu s$ |
| • Wide gain bandwidth | 2.5 | 5 | 20 | MHz |
| • Low input noise voltage | 20 | 12 | 12 | $nV/\sqrt{Hz}$ |

## APPLICATIONS

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

## GENERAL DESCRIPTION

These monolithic JFET input operational amplifiers incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BIFET Technology). These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

## ADVANTAGES

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (10,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

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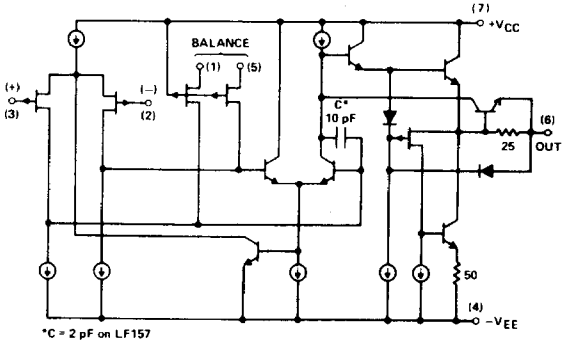
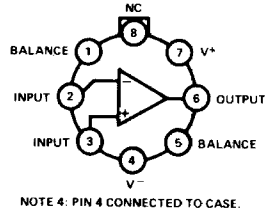
## SIMPLIFIED SCHEMATIC




*C = 2 pF on LF157

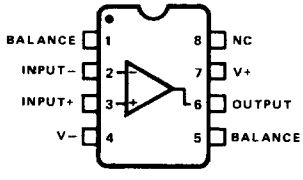
## CONNECTION DIAGRAM

**Metal Can Package**




NOTE 4: PIN 4 CONNECTED TO CASE.
TOP VIEW

**8 Pin Minidip**



## ABSOLUTE MAXIMUM RATINGS

| | LF155A/6A/7A | LF355A/6A/7A | LF155/6/7 | LF255/6/7 | LF355/6/7 |
|---|---|---|---|---|---|
| Supply Voltage | ±22V | ±22V | ±22V | ±22V | ±18V |
| Power Dissipation TO-99 (H package) (Note 1) | 670 mW | 500 mW | 670 mW | 570 mW | 500 mW |
| Operating Temperature Range | −55°C to +125°C | 0°C to +70°C | −55°C to +125°C | −25°C to +85°C | 0°C to +70°C |
| $T_{j(MAX)}$ | 150°C | 100°C | 150°C | 110°C | 100°C |
| Differential Input Voltage | ±40V | ±40V | ±40V | ±40V | ±30V |
| Input Voltage Range (Note 2) | ±20V | ±20V | ±20V | ±20V | ±16V |
| Output Short Circuit Duration | Continuous | Continuous | Continuous | Continuous | Continuous |
| Storage Temperature Range | −65°C to +150°C | −65°C to +150°C | −65°C to +150°C | −65°C to +150°C | −65°C to +150°C |
| Lead Temperature (Soldering, 10 seconds) | 300°C | 300°C | 300°C | 300°C | 300°C |

## DC ELECTRICAL CHARACTERISTICS (Note 3)

| SYMBOL | PARAMETER | CONDITIONS | LF155A/6A/7A | | | LF355A/6A/7A | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{OS}$ | Input Offset Voltage | $R_S = 50\Omega$, $T_A = 25°C$ | | 1 | 2 | | 1 | 2 | mV |
| | | Over Temperature | | | 2.5 | | | 2.3 | mV |
| $\Delta V_{OS}/\Delta T$ | Average TC of Input Offset Voltage | $R_S = 50\Omega$ | | 3 | 5 | | 3 | 5 | mV |
| $\Delta TC/\Delta V_{OS}$ | Change in Average TC with $V_{OS}$ Adjust | $R_S = 50\Omega$, (Note 4) | | 0.5 | | | 0.5 | | µV/°C per mV |
| $I_{OS}$ | Input Offset Current | $T_j = 25°C$, (Notes 3,5) | | 3 | 10 | | 3 | 10 | pA |
| | | $T_j \leq T_{HIGH}$ | | | 10 | | | 1 | nA |
| $I_B$ | Input Bias Current | $T_J = 25°C$, (Notes 3,5) | | 30 | 50 | | 30 | 50 | pA |
| | | $T_J \leq T_{HIGH}$ | | | 25 | | | 5 | nA |
| $R_{IN}$ | Input Resistance | $T_J = 25°C$ | | $10^{12}$ | | | $10^{12}$ | | Ω |
| $AV_{OL}$ | Large Signal Voltage Gain | $V_S = \pm15V$, $T_A = 25°C$ | 50 | 200 | | 50 | 200 | | V/mV |
| | | $V_O = \pm10V$, $R_L = 2k$ | | | | | | | |
| | | Over Temperature | 25 | | | 25 | | | V/mV |
| $V_O$ | Output Voltage Swing | $V_S = \pm15V$, $R_L = 10k$ | ±12 | ±13 | | ±12 | ±13 | | V |
| $V_{CM}$ | Input Common-Mode Voltage Range | $V_S = \pm15V$ | ±11 | +15.1 | | ±11 | +15.1 | | V |
| | | | | −12 | | | −12 | | V |
| CMRR | Common-Mode Rejection Ratio | | 85 | 100 | | 85 | 100 | | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 6) | 85 | 100 | | 85 | 100 | | dB |

## AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm15V$

| SYMBOL | PARAMETER | CONDITIONS | LF155A/355A | | | LF156A/356A | | | LF157A/357A | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| SR | Slew Rate | LF155A/6A: $A_V = 1$, LF157A: $A_V = 5$ | 3 | 5 | | 10 | 12 | | 40 | 50 | | V/µs |
| GBW | Gain-Bandwidth Product | | | 2.5 | | 4 | 4.5 | | 15 | 20 | | MHz |
| $t_s$ | Settling Time to 0.01% | (Note 7) | | 4 | | | 1.5 | | | 1.5 | | µs |
| $e_n$ | Equivalent Input Noise Voltage | $R_S = 100\Omega$ | | | | | | | | | | |
| | | f = 100 Hz | | 25 | | | 15 | | | 15 | | nV/$\sqrt{Hz}$ |
| | | f = 1000 Hz | | 20 | | | 12 | | | 12 | | nV/$\sqrt{Hz}$ |
| $i_n$ | Equivalent Input | f = 100 Hz | | 0.01 | | | 0.01 | | | 0.01 | | pA/$\sqrt{Hz}$ |
| | Noise Current | f = 1000 Hz | | 0.01 | | | 0.01 | | | 0.01 | | pA/$\sqrt{Hz}$ |
| $C_{IN}$ | Input Capacitance | | | 3 | | | 3 | | | 3 | | pF |

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## DC ELECTRICAL CHARACTERISTICS (Note 3)

| SYMBOL | PARAMETER | CONDITIONS | LF155/6/7 | | | LF255/6/7 | | | LF355/6/7 | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{OS}$ | Input Offset Voltage | $R_S = 50\Omega$, $T_A = 25°C$ | | 3 | 5 | | 3 | 5 | | 3 | 10 | mV |
| | | Over Temperature | | | 7 | | | 6.5 | | | 13 | mV |
| $\Delta V_{OS}/\Delta T$ | Average TC of Input Offset Voltage | $R_S = 50\Omega$ | | 5 | | | 5 | | | 5 | | $\mu V/°C$ |
| $\Delta TC/\Delta V_{OS}$ | Change in Average TC with $V_{OS}$ Adjust | $R_S = 50\Omega$, (Note 4) | | 0.5 | | | 0.5 | | | 0.5 | | $\mu V/°C$ per mV |
| $I_{OS}$ | Input Offset Current | $T_j = 25°C$, (Notes 3, 5) | | 3 | 20 | | 3 | 20 | | 3 | 50 | pA |
| | | $T_j \leq T_{HIGH}$ | | | 20 | | | 1 | | | 2 | nA |
| $I_B$ | Input Bias Current | $T_J = 25°C$, (Notes 3,5) | | 30 | 100 | | 30 | 100 | | 30 | 200 | pA |
| | | $T_J \leq T_{HIGH}$ | | | 50 | | | 5 | | | 8 | nA |
| $R_{IN}$ | Input Resistance | $T_J = 25°C$ | | $10^{12}$ | | | $10^{12}$ | | | $10^{12}$ | | $\Omega$ |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_S = \pm 15V$, $T_A = 25°C$ | 50 | 200 | | 50 | 200 | | 25 | 200 | | V/mV |
| | | $V_O = \pm 10V$, $R_L = 2k$ | | | | | | | | | | |
| | | Over Temperature | 25 | | | 25 | | | 15 | | | V/mV |
| $V_O$ | Output Voltage Swing | $V_S = \pm 15V$, $R_L = 10k$ | ±12 | ±13 | | ±12 | ±13 | | ±12 | ±13 | | V |
| $V_{CM}$ | Input Common-Mode Voltage Range | $V_S = \pm 15V$ | ±11 | +15.1 −12 | | ±11 | +15.1 −12 | | ±10 | +15.1 −12 | | V V |
| CMRR | Common-Mode Rejection Ratio | | 85 | 100 | | 85 | 100 | | 80 | 100 | | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 6) | 85 | 100 | | 85 | 100 | | 80 | 100 | | dB |

## DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$

| PARAMETER | LF155A/355A LF155/255 | | LF355 | | LF156A/356A LF156/256 | | LF356 | | LF157A/357A LF157/257 | | LF357 | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| Supply Current, | 2 | 4 | 2 | 4 | 5 | 7 | 5 | 10 | 5 | 7 | 5 | 10 | mA |

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## AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$

| SYMBOL | PARAMETER | CONDITIONS | LF155/LF255/ LF355 | LF156/LF256 | LF156/LF256/ LF356 | LF157/LF257 | LF157/LF257/ LF357 | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | TYP | MIN | TYP | MIN | TYP | |
| SR | Slew Rate | LF155/6: $A_V = 1$, LF157: $A_V = 5$ | 5 | 7.5 | 12 | 30 | 50 | V/μs |
| GBW | Gain-Bandwidth Product | | 2.5 | | 5 | | 20 | MHz |
| $t_s$ | Settling Time to 0.01% | (Note 7) | 4 | | 1.5 | | 1.5 | μs |
| $e_n$ | Equivalent Input Noise Voltage | $R_S = 100\Omega$ | | | | | | |
| | | f = 100 Hz | 25 | | 15 | | 15 | $nV/\sqrt{Hz}$ |
| | | f = 1000 Hz | 20 | | 12 | | 12 | $nV/\sqrt{Hz}$ |
| $i_n$ | Equivalent Input Current Noise | f = 100 Hz | 0.01 | | 0.01 | | 0.01 | $pA/\sqrt{Hz}$ |
| | | f = 1000 Hz | 0.01 | | 0.01 | | 0.01 | $pA/\sqrt{Hz}$ |
| $C_{IN}$ | Input Capacitance | | 3 | | 3 | | 3 | pF |

## NOTES FOR ELECTRICAL CHARACTERISTICS

**NOTE 1:** The TO-99 package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case.

**NOTE 2:** Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

**NOTE 3:** These specifications apply for $\pm 15V \leq V_S \leq \pm 20V$, $-55°C \leq T_A \leq +125°C$ and $T_{HIGH} = +125°C$ unless otherwise stated for the LF155A/6A/7A and the LF155/6/7. For the LF255/6/7, these specifications apply for $\pm 15V \leq V_S \leq \pm 20V$, $-25°C \leq T_A \leq +85°C$ and $T_{HIGH} = 85°C$ unless otherwise stated. For the LF355A/6A/7A, these specifications apply for $\pm 15V \leq V_S \leq \pm 20V$, $0°C \leq T_A \leq +70°C$ and $T_{HIGH} = +70°C$, and for the LF355/6/7 these specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq +70°C$. $V_{OS}$, $I_B$ and $I_{OS}$ are measured at $V_{CM} = 0$.

**NOTE 4:** The Temperature Coefficient of the adjusted input offset voltage changes only a small amount ($0.5\mu V/°C$ typically for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

**NOTE 5:** The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, $T_J$. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \Theta jA$ Pd where $\Theta jA$ is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

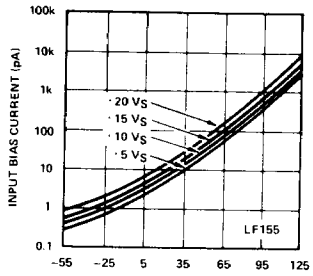
**NOTE 6:** Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

**NOTE 7:** Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF155/6. It is the time required for error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157, $A_V = -5$, the feedback resistor from output to input is 2 kΩ and the output step is 10V (See Settling Time Test Circuit, page 9).

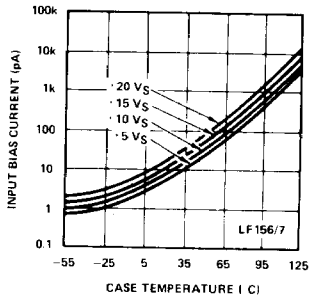
## TYPICAL DC PERFORMANCE CHARACTERISTICS

Curves are for LF155, LF156 and LF157 unless otherwise specified.

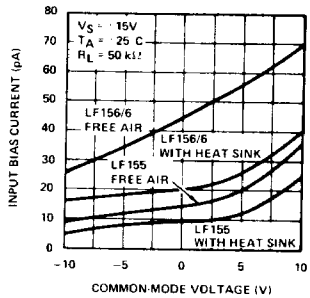
**Input Bias Current**



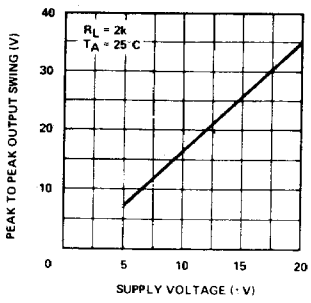

**Input Bias Current**



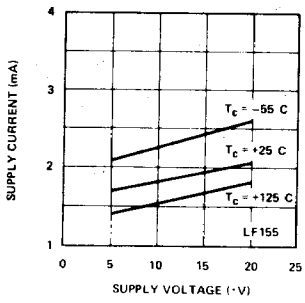

**Input Bias Current**



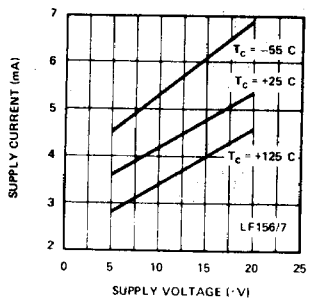

**Voltage Swing**



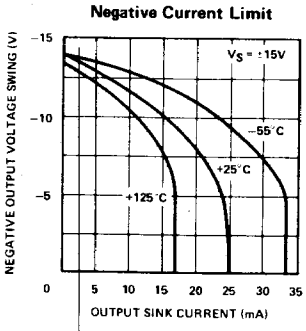

**Supply Current**



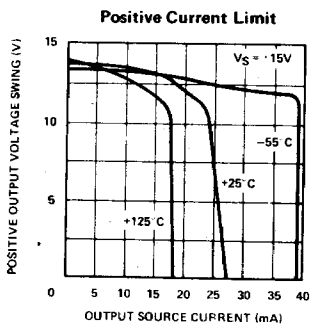

**Supply Current**



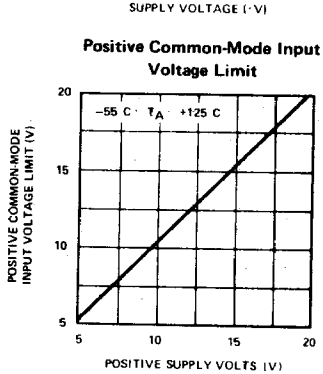

**Negative Current Limit**




**Positive Current Limit**




**Positive Common-Mode Input Voltage Limit**

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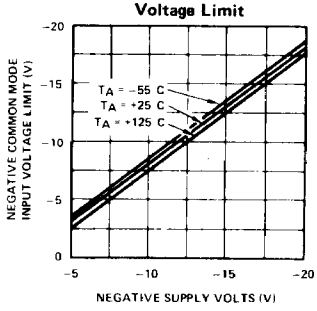
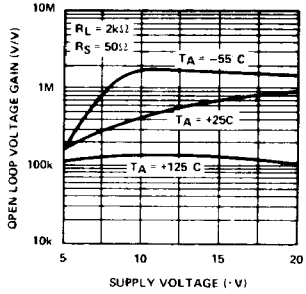
## TYPICAL DC PERFORMANCE CHARACTERISTICS (CON'T)

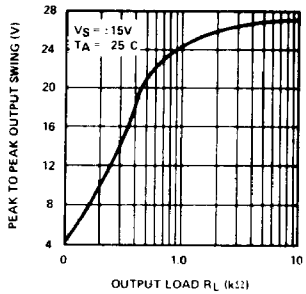
**Negative Common-Mode Input Voltage Limit**




**Open Loop Voltage Gain**

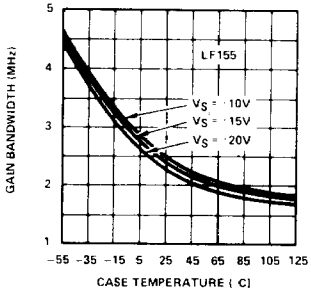


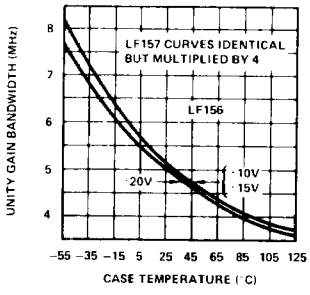

**Output Voltage Swing**



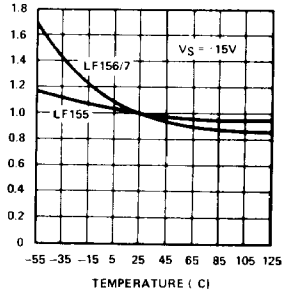

## TYPICAL AC PERFORMANCE CHARACTERISTICS

**Gain Bandwidth**

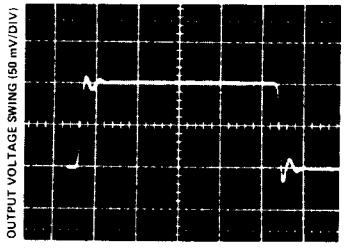


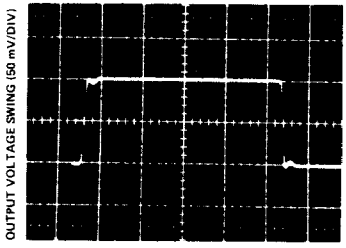

**Normalized Slew Rate**



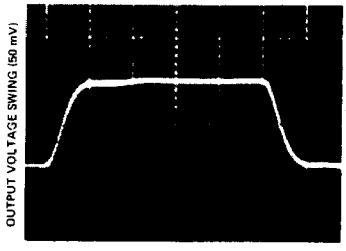

**LF155 Small Signal Pulse Response, $A_V$ = +1**



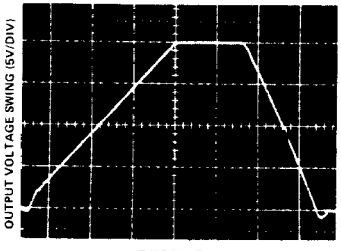

**LF156 Small Signal Pulse Response, $A_V$ = +1**



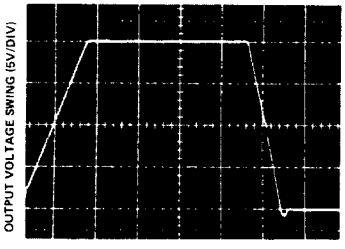

**LF157 Small Signal Pulse Response, $A_V$ = +5**



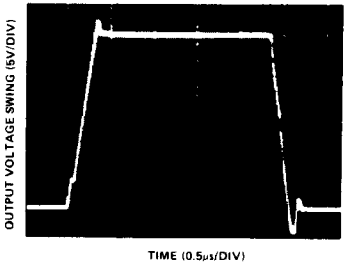

**LF155 Large Signal Pulse Response, $A_V$ = +1**




**LF156 Large Signal Pulse Response, $A_V$ = +1**




**LF157 Large Signal Pulse Response, $A_V$ = +5**

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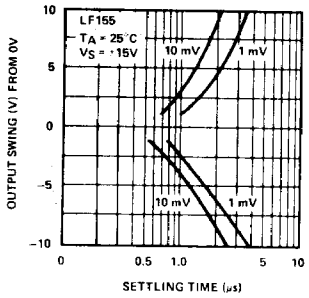
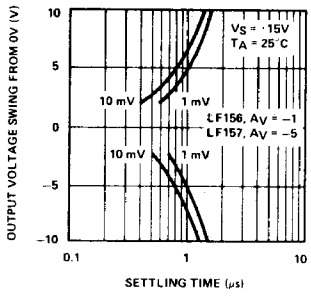
## TYPICAL AC PERFORMANCE CHARACTERISTICS (CON'T)

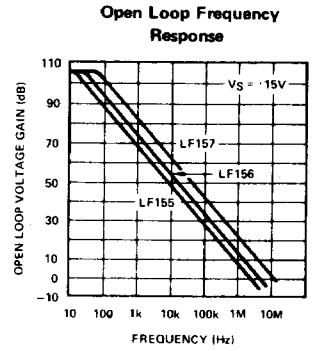
**Inverter Settling Time**



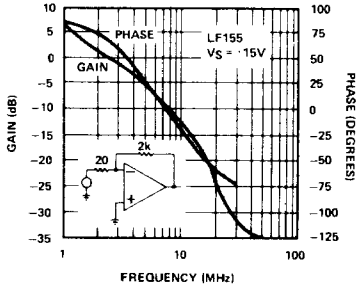

**Inverter Settling Time**



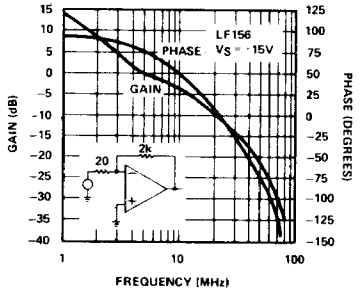

**Open Loop Frequency Response**



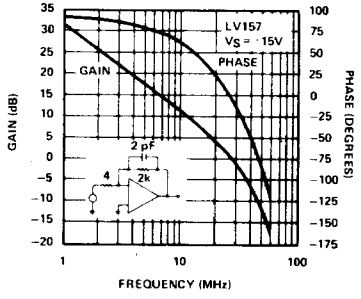

**Bode Plot**



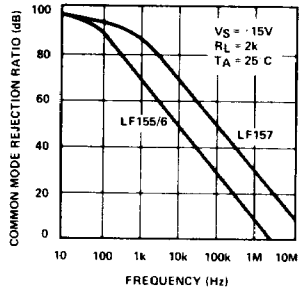

**Bode Plot**



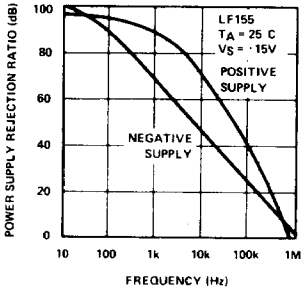

**Bode Plot**



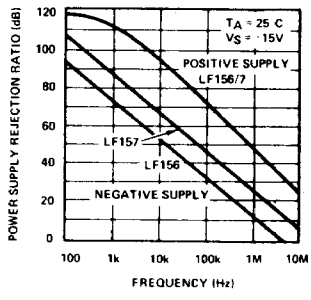

**Common-Mode Rejection Ratio**



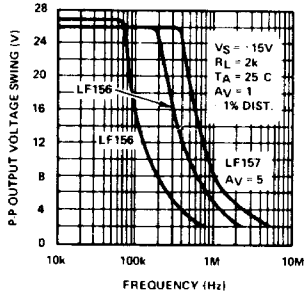

**Power Supply Rejection Ratio**



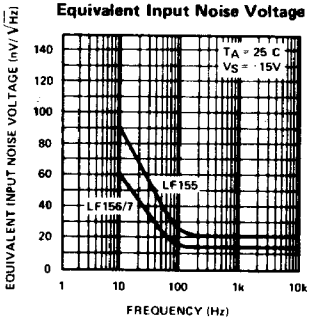

**Power Supply Rejection Ratio**



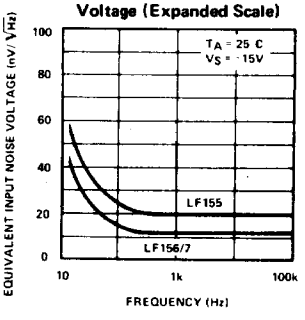

**Undistorted Output Voltage Swing**




**Equivalent Input Noise Voltage**




**Equivalent Input Noise Voltage (Expanded Scale)**

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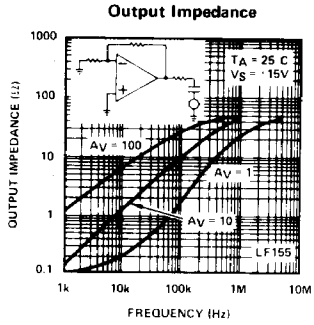
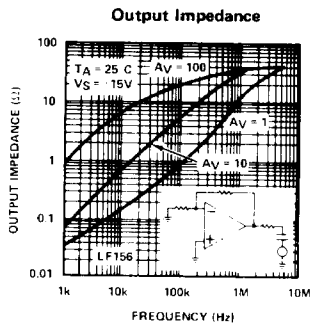
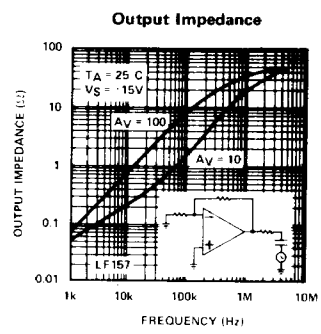
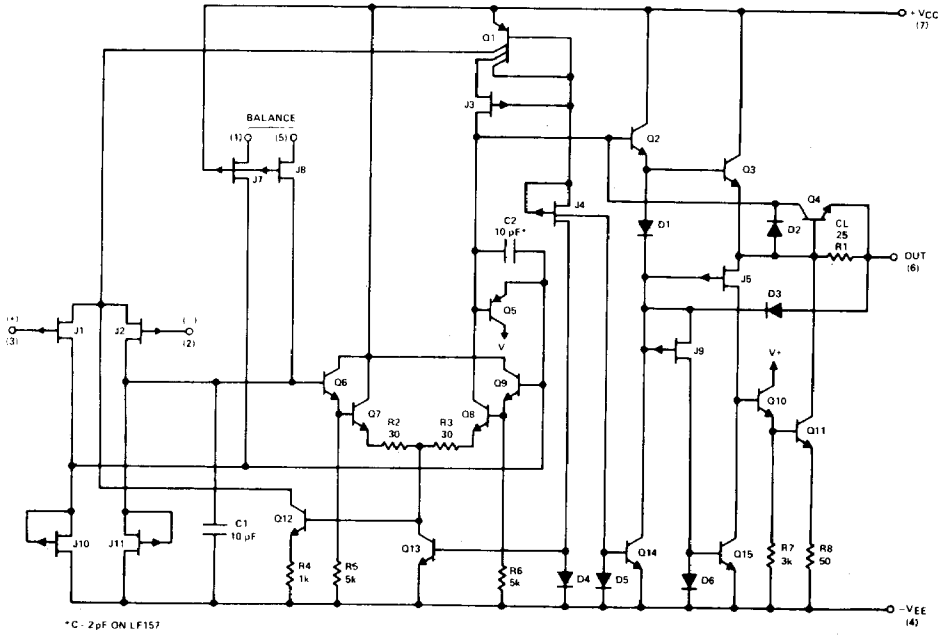
## TYPICAL AC PERFORMANCE CHARACTERISTICS (CON'T)



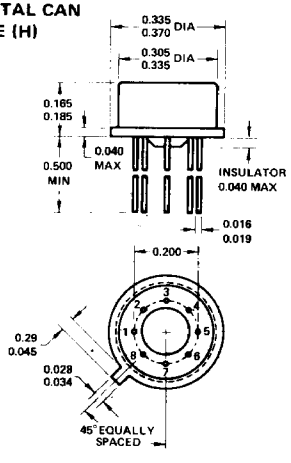




## DETAILED SCHEMATIC




## PACKAGE DIMENSIONS

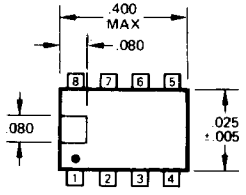
**TO-99 METAL CAN PACKAGE (H)**

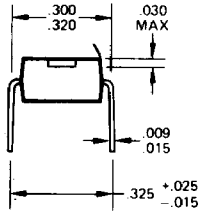


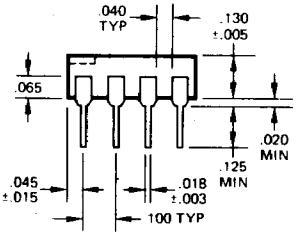

**ORDER NUMBER:**

**8 PIN MINIDIP**

LF155T
LF155AT
LF156T
LF156AT
LF157T
LF157AT
LF255T
LF256T
LF257T
LF355T
LF355AT
LF355AP
LF356T
LF356AT
LF356AP
LF357T
LF357AT
LF357AP

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## APPLICATION HINTS

The LF155/6/7 series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltage. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

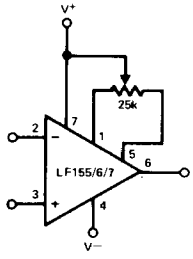
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

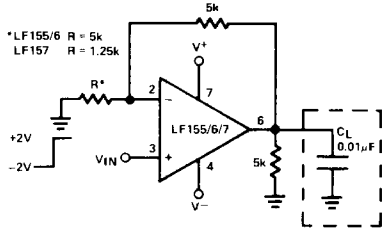
## TYPICAL CIRCUIT CONNECTIONS

**$V_{OS}$ Adjustment**




- $V_{OS}$ is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to $V^+$
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5μV/°C/m of adjustment.
- Typical overall drift: 50V/°C ≅ (0.5μV/°C/mV of adj.)

**Driving Capacitive Loads**



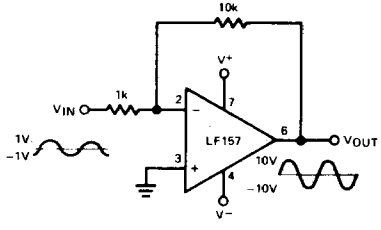

Due to a unique output stage design these amplifiers have the ability to drive large capacitive loads and still maintain stability.

$C_{L\ MAX} \cong 0.01\mu F$.

Overshoot ≤ 20%.

Settling time ($t_s$) ≅ 5μs

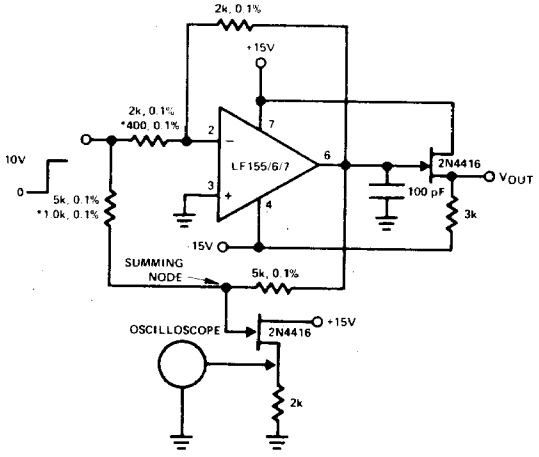
**LF157. A Large Power BW Amplifier**




For distortion < 1% and a 20 Vp-p $V_{OUT}$ swing power bandwidth is: 500 kHz.

## TYPICAL APPLICATIONS

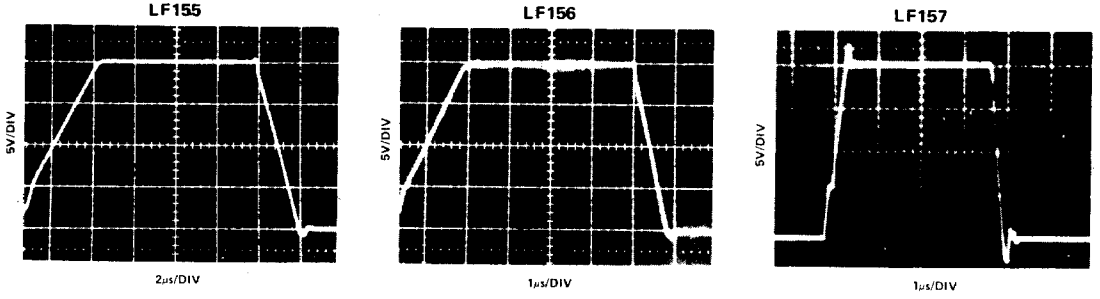
**Settling Time Test Circuit**




- Settling time is tested with the LF155/6 connected as unity gain inverter and LF157 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10V step

* $A_V = -5$ for LF157

**Large Signal Inverter Output, $V_{OUT}$ (from Settling Time Circuit)**

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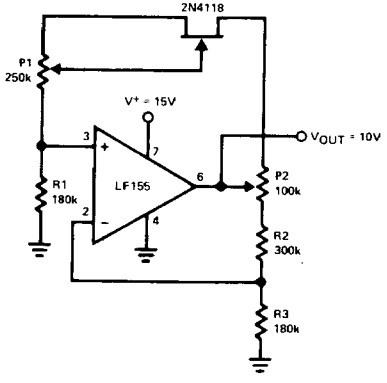
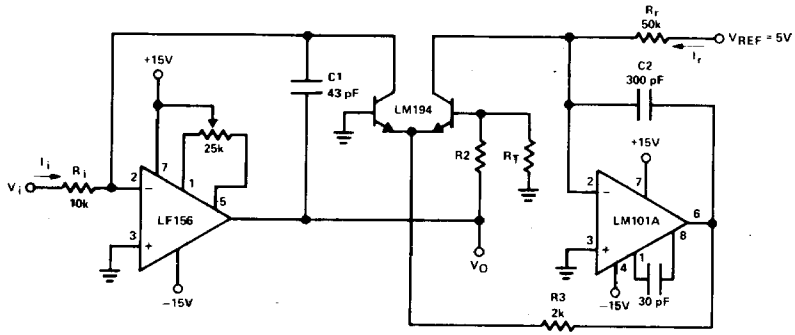
**Low Drift Adjustable Voltage Reference**




- $\Delta V_{OUT}/\Delta T = \pm 0.002\%/^{\circ}C$
- All resistors and potentiometers should be wire-wound
- P1: drift adjust
- P2: $V_{OUT}$ adjust
- Use LF155 for
  - Low $I_B$
  - Low drift
  - Low supply current

## TYPICAL APPLICATIONS (CON'T)

**Fast Logarithmic Converter**

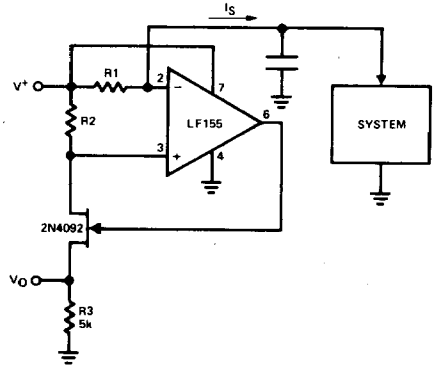



$$|V_{OUT}| = \left[1 + \frac{R2}{R_T}\right]\frac{kT}{q} \quad \text{Ln } V_i \left[\frac{R_r}{V_{REF} R_i}\right] = \log V_i \frac{1}{R_i I_r}$$

R2 = 15.7k, $R_T$ = 1k, 0.3%/°C (for temperature compensation)

- Dynamic range: 100μA ≤ $I_i$ ≤ 1 mA (5 decades), $|V_O|$ = 1V/decade
- Transient response: 3μs for $\Delta I_i$ = 1 decade
- C1, C2, R2, R3: added dynamic compensation
- $V_{OS}$ adjust the LF156 to minimize quiescent error
- $R_T$: Tel Labs type Q81 + 0.3%/°C.

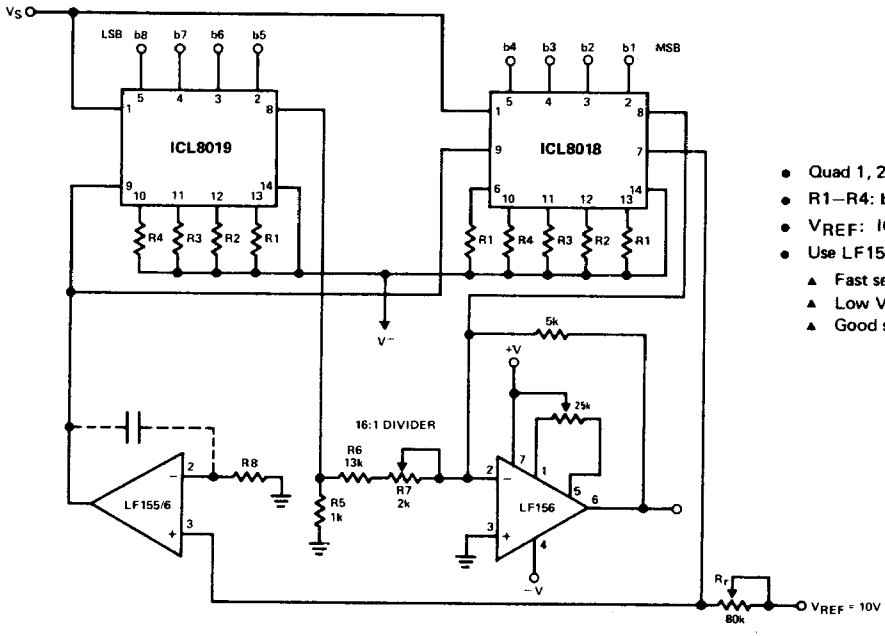
**Precision Current Monitor**




- $V_O = 5\frac{R1}{R2}$ (V/mA of $I_S$)
- R1, R2, R3: 0.1% resistors
- Use LF155 for
  - Common mode range to supply voltage
  - Low $I_B$
  - Low $V_{OS}$
  - Low supply current

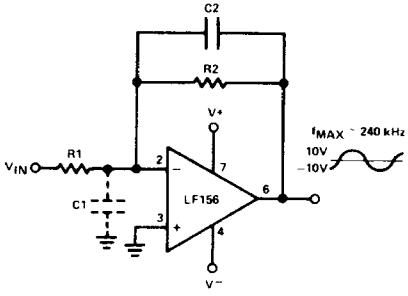
## TYPICAL APPLICATIONS (CON'T)

**LF156 as an Output Amplifier in a Fast 8-Bit DAC**



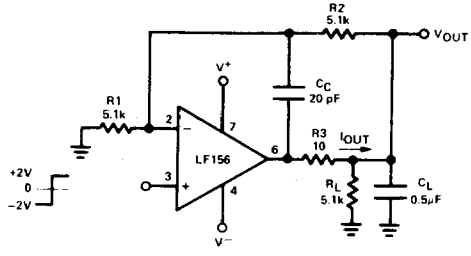

- Quad 1, 2: precision current switches
- R1–R4: binary ladder
- $V_{REF}$: ICL 8069
- Use LF155/6 for
  - ▲ Fast settling time
  - ▲ Low $V_{OS}$ drift
  - ▲ Good stability

**Wide BW Low Noise, Low Drift Amplifier**




- Power BW: $f_{MAX} = \frac{S_r}{2\pi V_P} \cong 240\ kHz$
- Parasitic input capacitance C1 ≅ (3 pF for LF155, LF156, and LF157 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2C2 ≅ R1C1.

**Isolating Large Capacitive Loads**



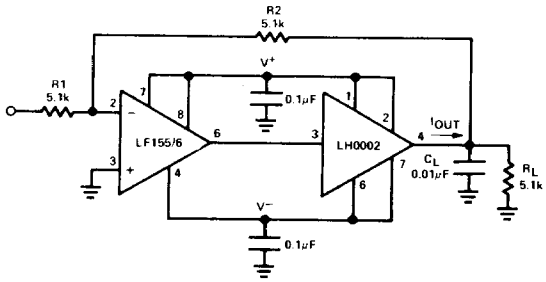

- Overshoot 6%
- $t_s$ 10μs
- When driving large $C_L$ the $V_{OUT}$ slew rate determined by $C_L$ and $I_{OUT\ MAX}$:

$$\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{OUT}}{C_L} \cong \frac{0.02}{0.5} \quad V/\mu s = 0.04 V/\mu s$$

(with $C_L$ shown)

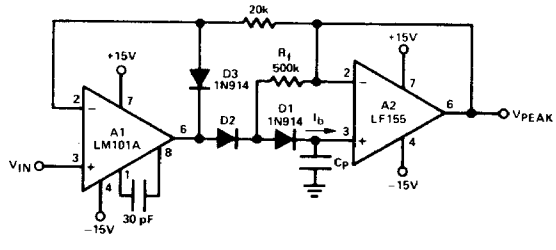
## TYPICAL APPLICATIONS (CON'T)

**Boosting the LF156 with a Current Amplifier**



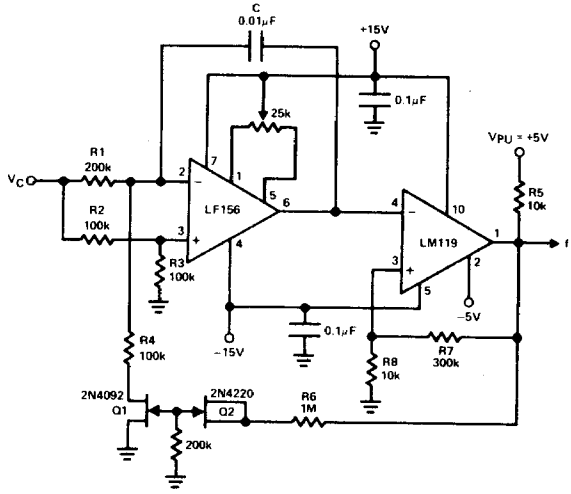

- $I_{OUT\ MAX} \cong 150$ mA (will drive $R_L \geq 100\Omega$)
- $\frac{\Delta V_{OUT}}{\Delta T} = 15 V/\mu sec$ (with $C_L$ shown)
- No additional phase shift added by the current amplifier

**Low Drift Peak Detector**




- By adding D1 and $R_f$, $V_{D1} = 0$ during hold mode. Leakage of D2 provided by feedback path through $R_f$.
- Leakage of circuit is essentially $I_b$ (LF155, LF156) plus capacitor leakage of $C_p$.
- Diode D3 clamps $V_{OUT}$ (A1) to $V_{IN} - V_{D3}$ to improve speed and to limit reverse bias of D2.
- Maximum input frequency should be $<< \frac{1}{2\pi R_f C_{D2}}$ where $C_{D2}$ is the shunt capacitance of D2.

**3 Decades VCO**

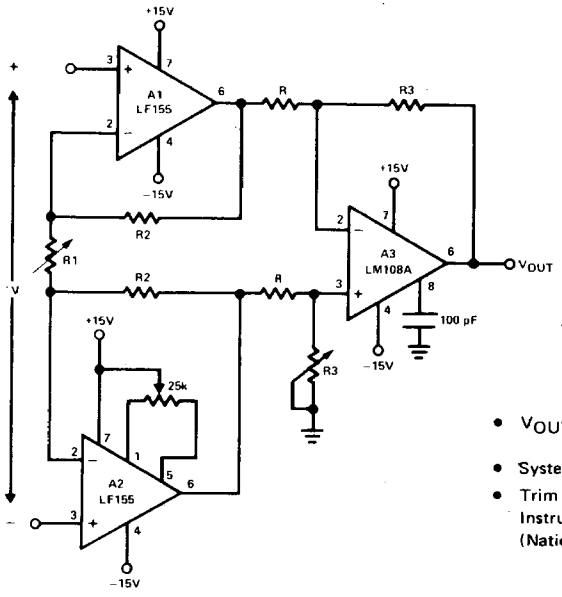



$$f = \frac{V_C (R8 + R7)}{[8\ V_{PU} R8 R1]\ C}, \quad 0 \leq V_C \leq 30V,\ 10\ Hz \leq f \leq 10\ kHz$$

R1, R4 matched. Linearity 0.1% over 2 decades.

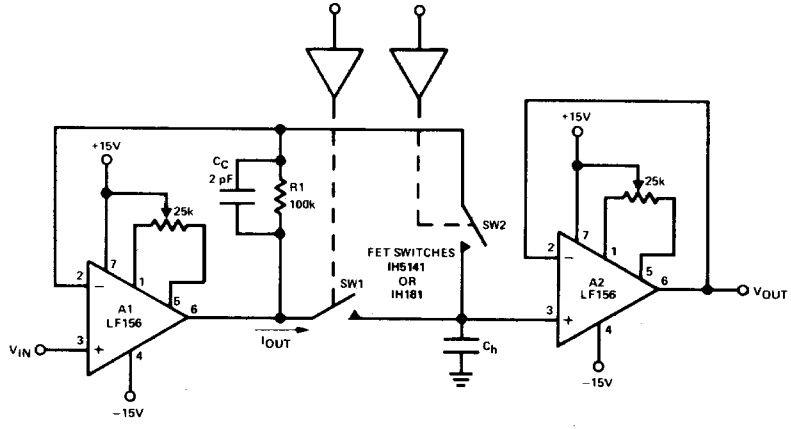
## TYPICAL APPLICATIONS (CON'T)

**High Impedance, Low Drift Instrumentation Amplifier**




- $V_{OUT} = \frac{R3}{R}\left[\frac{2R2}{R1} + 1\right]$ $\Delta V$, $V^- + 2V \leq V_{IN}$ Common-Mode $\leq V^+$
- System $V_{OS}$ adjusted via A2 $V_{OS}$ adjust
- Trim R3 to boost up CMRR to 120 dB. Instrumentation amplifier Resistor array RA201 (National Semiconductor) recommended

**Fast Sample and Hold**




- Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time, $T_A$, estimated by:

$$T_A \cong \left[\frac{2R_{ON} \cdot V_{IN} \cdot C_h}{S_r}\right]^{1/2}$$ provided that:

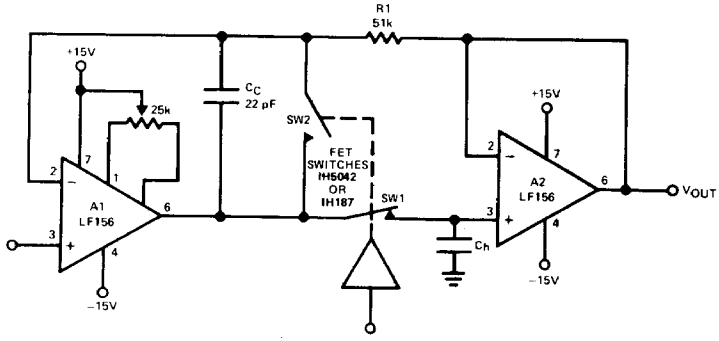
$$V_{IN} < 2\pi S_r R_{ON} C_h \text{ and } T_A > \frac{V_{IN} C_h}{I_{OUT\ MAX}}$$ , $R_{ON}$ is of SW1

If inequality not satisfied: $T_A \cong \frac{V_{IN} C_h}{20\ mA}$

- LF156 develops full $S_r$ output capability for $V_{IN} \geq 1V$
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2

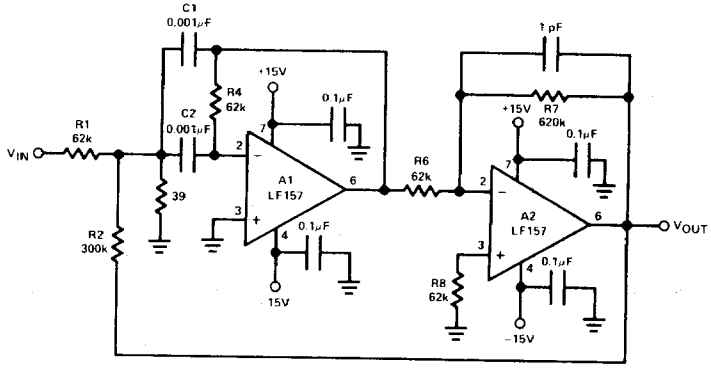
## TYPICAL APPLICATIONS (CON'T)

### High Accuracy Sample and Hold




- By closing the loop through A2 the $V_{OUT}$ accuracy will be determined uniquely by A1. No $V_{OS}$ adjust required for A2.
- $T_A$ can be estimated by same considerations as previously but because of the added propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, $C_C$: additional compensation
- Use LF156 for
  - Fast settling time
  - Low $V_{OS}$

### High Q Band Pass Filter



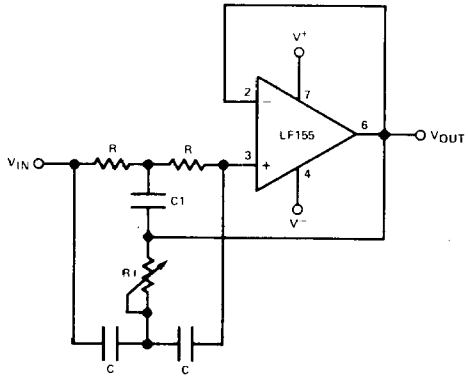

- By adding positive feedback (R2) Q increases to 40
- $f_{BP}$ = 100 kHz

$$\frac{V_{OUT}}{V_{IN}} = 10\sqrt{Q}$$

- Clean layout recommended
- Response to a 1 Vp-p tone burst: 300μs

## TYPICAL APPLICATIONS (CON'T)

**High Q Notch Filter**




- $2R1 = R = 10M\Omega$
  $2C = C1 = 300\ pF$
- Capacitors should be matched to obtain high Q
- $f_{NOTCH} = 120$ Hz, notch = −55 dB, $Q > 100$
- Use LF155 for
  - Low $I_B$
  - Low supply current

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## DEFINITION OF TERMS

**Input Offset Voltage:** That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

**Input Offset Current:** The difference in the currents into the two input terminals when the output is at zero.

**Input Bias Current:** The average of the two input currents.

**Input Common-Mode Voltage Range:** The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

**Common-Mode Rejection Ratio:** The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

**Input Resistance:** The ratio of the change in input voltage to the change in input current on either input with the other grounded.

**Supply Current:** The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

**Output Voltage Swing:** The peak output voltage swing, referred to zero, that can be obtained without clipping.

**Large-Signal Voltage Gain:** The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

**Power Supply Rejection Ratio:** The ratio of the change in input offset voltage to the change in power supply voltage producing it. The typical curves in this sheet show values for each supply independently changed. The electrical specification, however, is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

**Settling Time:** The time required for the error between input and output to settle to within a specified limit after an input is applied to the test circuit shown in typical applications.