SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SG124/224/324

Quad Operational Amplifier

The SG124 series integrated circuit contains four true-differential, independent operational amplifiers. Each amplifier has been designed to operate from either a single supply voltage or plus and minus voltages and features internal frequency compensation, high gain, and very low supply current requirements. An additional significant advantage of these amplifiers is that when using a single supply, the input and output can be operated down to ground potential. Thus, they can be powered by a standard +5V DC logic supply and still be compatible with all forms of logic inputs and outputs.

- **Four internally compensated op amps in a single package**
- **Inputs and outputs can go to ground with a single supply voltage**
- **Input bias current is both low and constant with temperature**
- **Wide supply voltage compatibility with low current drain**
- **Available in 14-pin plastic or cerdip package**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V^+	$32V_{DC}$ or $\pm16V_{DC}$
Differential Input Voltage	$32V_{DC}$
Input Voltage	$-0.3V_{DC}$ to $+32V_{DC}$
Power Dissipation (Note 1)	
N Package (plastic)	600mW
Derate above 25°C	6.0mW/°C
J Package (cerdip)	1000mW
Derate above 25°C	6.7mW/°C
Output Short-Circuit to Gnd (Note 2) $V^+ \leq 15V_{DC}$ and $T_A = 25°C$	Continuous
Operating Temperature Range	
SG124	−55°C to +125°C
SG224	−25°C to +85°C
SG324	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Electrical Characteristics ($V^+ = +5V$ DC and $T_A = 25°C$ unless otherwise noted)

Parameter	Conditions	SG124 Min.	SG124 Typ.	SG124 Max.	SG224/SG324 Min.	SG224/SG324 Typ.	SG224/SG324 Max.	Units
Input Offset Voltage	$R_S = 0\Omega$	—	2	5	—	2	7	mV_{DC}
Input Bias Current (Note 3)		—	45	150	—	45	250	nA_{DC}
Input Offset Current	$I_{IN}(+) - I_{IN}(-)$	—	±3	±30	—	±5	±50	nA_{DC}
Input Common-Mode Voltage Range (Note 4)		0	—	V^+-1.5	0	—	V^+-1.5	V_{DC}
Supply Current	$R_L = \infty$ On All Op Amps	—	0.8	1.2	—	0.8	1.2	mA_{DC}
Large Signal Voltage Gain	$R_L \geq 2k\Omega$	50	100	—	25	100	—	V/mV
Output Voltage Swing	$R_L = 2\ k\Omega$	0	—	V^+-1.5	0	—	V^+-1.5	V_{DC}
Common Mode Rejection Ratio	DC	70	85	—	65	85	—	dB
Power Supply Rejection Ratio	DC	65	100	—	65	100	—	dB
Amplifier-to-Amplifier Coupling	f = 1 kHz to 20 kHz (Input Referred)	—	−120	—	—	−120	—	dB
Output Current Source	$V_{IN}^+ = +1V_{DC}$, $V_{IN}^- = 0\ V_{DC}$	20	40	—	20	40	—	mA_{DC}
Output Current Sink	$V_{IN}^- = +1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$	10	20	—	10	20	—	mA_{DC}

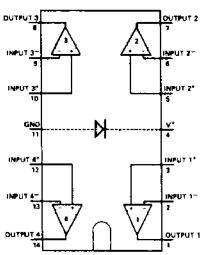
Note 1: For operating at high temperatures, the SG324 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The SG224 and SG124 can be derated based on a +150°C maximum junction temperature.

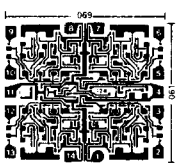
Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of $+15V_{DC}$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.

Note 3: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 4: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+-1.5V, but either or both inputs can go to $+30V_{DC}$ without damage.

CONNECTION DIAGRAM





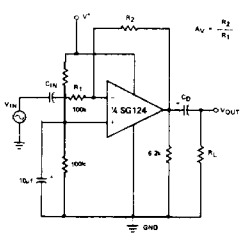
CHIP BONDING DIAGRAM

APPLICATIONS INFORMATION

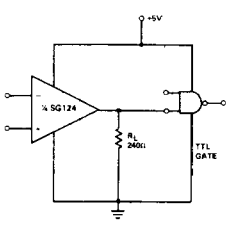
To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For AC applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in DC applications, there is no crossover distortion.

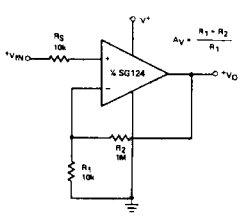
Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.



SINGLE SUPPLY INVERTING AC AMPLIFIER WITH INPUT BIASED TO ONE-HALF SUPPLY



TTL INTERFACE



SINGLE SUPPLY NON-INVERTING DC AMPLIFIER (0V INPUT = 0V OUTPUT)