Integrated Device Technology, Inc.

HIGH SPEED BiCMOS 10-BIT MEMORY DRIVERS

ADVANCE INFORMATION
IDT54/74FBT2827A/B
IDT54/74FBT2828A/B

FEATURES

- IDT54/74FBT2827A/2828A is equivalent to 54/74BCT2827A/2828A
- **IDT54/74FBT2827B/2828B is 30% faster than BCT**
- 25Ω output resistors reduce overshoot and undershoot when driving MOS RAMs
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Higher static VOH for improved noise immunity and reduced system power dissipation
- Low power in all three states
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

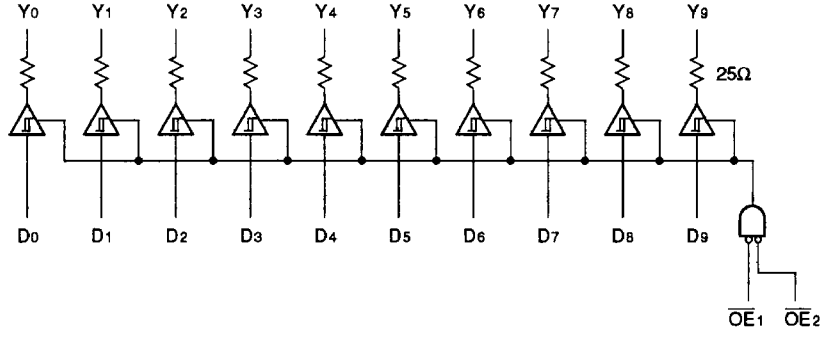
DESCRIPTION

The FBT series of BiCMOS Memory Drivers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT2827A/B and IDT54/74FBT2828A/B are 3-state 10-bit buffers where each output is terminated with a 25Ω series resistor. The output buffers are enabled when the two Active-LOW output enable pins are logic LOW.

The FBT series of memory line drivers are ideal for use in designs needed to drive large capacitive loads, with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection. They are also designed for rail-to-rail output switching. This higher output level in the high state will result in significant reduction in overall system power dissipation.

FUNCTIONAL BLOCK DIAGRAM



2516 drw 01

PRODUCT SELECTOR GUIDE

	10-Bit Memory Driver
Non-inverting	IDT 54/74FBT2827A/B
Inverting	IDT 54/74FBT2828A/B

2516 tbl 01

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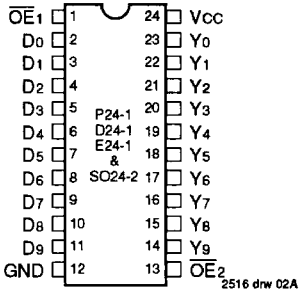
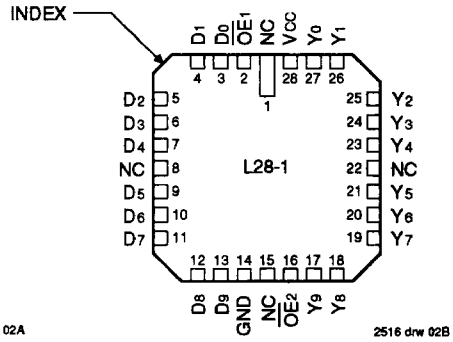
PIN CONFIGURATIONS

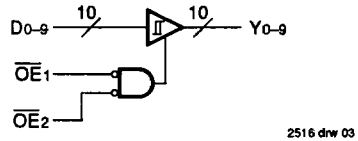


DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW

LOGIC SYMBOL



PIN DESCRIPTION

Name	I/O	Description
$\overline{OE_1}$ $\overline{OE_2}$	I	When both are LOW, the outputs are enabled. When either one or both are HIGH the outputs are High Z.
D_I	I	10-bit data input.
Y_I	O	10-bit data output.

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FUNCTION TABLES

IDT54/74FBT2827A/B (Non-Inverting)(1)

Inputs			Output	
$\overline{OE_1}$	$\overline{OE_2}$	D_I	Y_I	Function
L	L	L	L	Transparent
L	L	H	H	
H	X	X	Z	3-State
X	H	X	Z	

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

2516 tbl 03

IDT54/74FBT2828A/B (Inverting)(1)

Inputs			Output	
$\overline{OE_1}$	$\overline{OE_2}$	D_I	Y_I	Function
L	L	L	H	Transparent
L	L	H	L	
H	X	X	Z	3-State
X	H	X	Z	

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2516 tbl 06

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Condition	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2516 tbl 07

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	–10	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	–50	
I_I	Input HIGH Current	V_{CC} = Max., V_I = 5.5V		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output Drive Current	V_{CC} = Min., V_O = 2.25V		–35	—	—	mA
I_{ODL}	Output Drive Current	V_{CC} = Min., V_O = 2.25V		50	—	—	mA
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND(3)		–60	—	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –300µA(4)	V_{HC}	V_{CC}	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –1mA	2.4	3.3	—	
			I_{OH} = –12mA	2.0	3.2	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 300µA(4)	—	GND	V_{LC}	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 1mA	—	0.1	0.5	
			I_{OL} = 12mA	—	0.35	0.8	
V_H	Input Hysteresis	—		—	200	—	mV
I_{CCH} I_{CCZ} I_{CCL}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES: 2516 tbl 05

1. For condition shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This condition is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Condition[1]		Min.	Typ.	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}_1$ = $\overline{OE}_2$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	
		$\overline{OE}_1$ = $\overline{OE}_2$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	4.0	7.8[5]	mA
		$\overline{OE}_1$ = $\overline{OE}_2$ = GND Ten Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	6.5	17.8[5]	

NOTES:
2516 tbl 08

1. For condition shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Quiescent Current
   D_H = Duty Cycle for a TTL High Input (V_{IN} = 3.4V)
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in MHz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

		FBT2827A				FBT2827B			
		Commercial		Military		Commercial		Military	
Symbol	Parameter	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.
t_{PHL} t_{PLH}	Prop Delay, Di to Yi	1.5	7.0	1.5	7.5	1.5	5.0	1.5	6.5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Yi	1.5	13.0	1.5	14	1.5	8.0	1.5	9.0
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Yi	1.5	13.0	1.5	14	1.5	7.0	1.5	8.0

		FBT2828A				FBT2828B			
		Commercial		Military		Commercial		Military	
Symbol	Parameter	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.
t_{PHL} t_{PLH}	Prop Delay, Di to Yi	1.5	8.0	1.5	8.5	1.5	5.5	1.5	6.5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Yi	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Yi	1.5	14.0	1.5	15.0	1.5	7.0	1.5	8.0

NOTES:
2516 tbl 09

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.