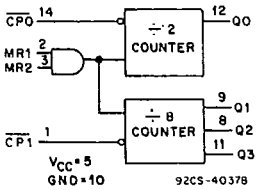
File Number 1849

CD54/74HC93
CD54/74HCT93

High-Speed CMOS Logic

4-Bit Binary Ripple Counter

Type Features:
- *Can be configured to divide by 2, 8, and 16*
- *Asynchronous Master Reset*



FUNCTIONAL DIAGRAM

The RCA-CD54/74HC93 and the CD54/74HCT93 are high-speed silicon-gate CMOS devices and are pin-compatible with low power Schottky TTL (LSTTL). These 4-bit binary ripple counters consist of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate clock input ($\overline{CP0}$ and $\overline{CP1}$) to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Qn outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous master reset (MR1 and MR2) is provided which overrides both clocks and resets (clears) all flip-flops.

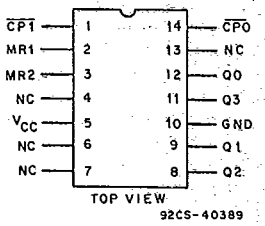
Because the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes.

In a 4-bit ripple counter the output Q0 must be connected externally to input $\overline{CP1}$. The input count pulses are applied to clock input $\overline{CP0}$. Simultaneous frequency divisions of 2, 4, 8, and 16 are performed at the Q0, Q1, Q2, and Q3 outputs as shown in the function table. As a 3-bit ripple counter the input count pulses are applied to input $\overline{CP1}$.

Simultaneous frequency divisions of 2, 4, and 8 are available at the Q1, Q2, and Q3 outputs. Independent use of the first flip-flop is available if the reset function coincides with the reset of the 3-bit ripple-through counter.

The CD54HC93 and CD54HCT93 are supplied in 14-lead hermetic dual-in-line frit-seal ceramic packages (F suffix). The CD74HC93 and CD74HCT93 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range:*
  CD74HC/HCT: −40 to +85°C
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC types:*
  2 to 6 V operation
  High noise immunity:
  N_{IL}=30%, N_{IH}=30% of V_{CC}; @ V_{CC}=5 V
- *CD54HCT/CD74HCT types:*
  4.5 to 5.5 V operation
  Direct LSTTL input logic compatibility
  V_{IL}=0.8 V max., V_{IH}=2 V min.
  CMOS input compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC93
CD54/74HCT93

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o <$ V_{CC} +0.5 V) ..... ±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F,H) ..... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F,H) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F,H ..... -55 to +125° C
PACKAGE TYPE E,M ..... -40 to +85° C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300° C

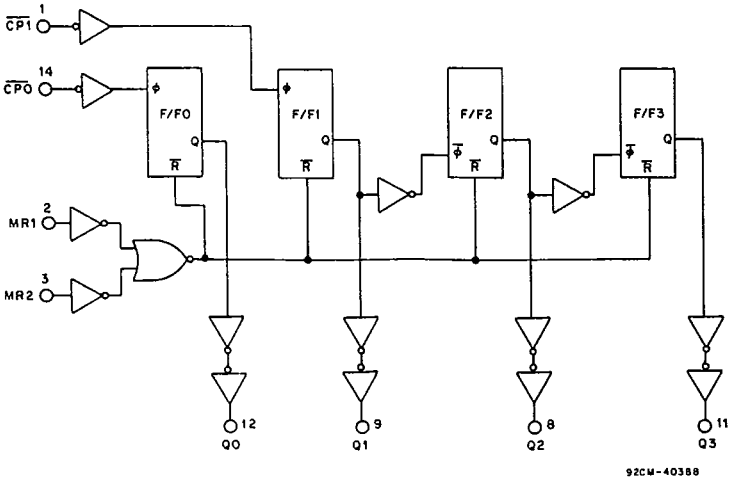


Fig. 1 - HC/HCT93 logic diagram.

FUNCTION TABLE
(Q0 connected to CP1)

COUNT	OUTPUTS			
	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

MODE SELECTION

RESET INPUTS		OUTPUTS			
MR1	MR2	Q0	Q1	Q2	Q3
H	H	L	L	L	L
L	H	count			
H	L	count			
L	L	count			

H = HIGH voltage level
L = LOW voltage level

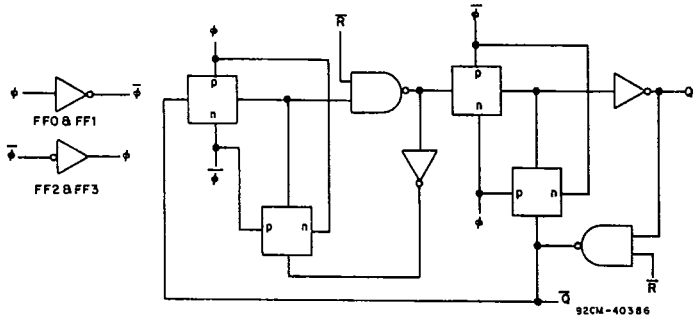


Fig. 2 - Flip-flop (0-3) logic detail.

CD54/74HC93
CD54/74HCT93

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC93/CD54HC93										CD74HCT93/CD54HCT93									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS*
$\overline{CP0}$, $\overline{CP1}$	0.6
MR1, MR2	0.4

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g. 360 μA max. @ 25°C.

CD54/74HC93
CD54/74HCT93

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r,t_f:			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25° C, Input t_r,t_f=6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL VALUES HC	TYPICAL VALUES HCT	UNITS
Propagation Delay:	t_{PLH}	15	10	14	ns
$\overline{CP0}$ to Q0 Output	t_{PHL}				
$\overline{CP1}$ to Q3			21	24	ns
MRn to Qn Output			13	13	ns
Power Dissipation Capacitance*	C_{PD}	—	25	25	pF

*C_{PD} is used to determine the dynamic power consumption, per counter.

$P_D = C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$ where f_i = input frequency

f_o = output frequency

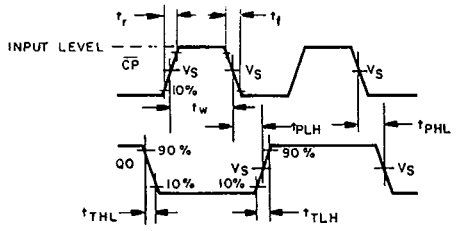
C_L = output load capacitance

V_{CC} = supply voltage.

PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	TEST CONDITIONS V_{CC} (V)	LIMITS 25° C HC Min.	25° C HC Max.	25° C HCT Min.	25° C HCT Max.	-40° C to +85° C 74HC Min.	-40° C to +85° C 74HC Max.	-40° C to +85° C 74HCT Min.	-40° C to +85° C 74HCT Max.	-55° C to +125° C 54HC Min.	-55° C to +125° C 54HC Max.	-55° C to +125° C 54HCT Min.	-55° C to +125° C 54HCT Max.	UNITS
Maximum Clock Frequency f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
	4.5	30	—	30	—	24	—	24	—	20	—	20	—	MHz
	6	35	—	—	—	28	—	—	—	24	—	—	—	MHz
Clock Pulse Width t_W $\overline{CP0}$, $\overline{CP1}$	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
	4.5	16	—	16	—	20	—	20	—	24	—	24	—	ns
	6	14	—	—	—	17	—	—	—	20	—	—	—	ns
Reset Pulse Width t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
	4.5	16	—	16	—	20	—	20	—	24	—	24	—	ns
	6	14	—	—	—	17	—	—	—	20	—	—	—	ns
Reset Removal Time t_{REM}	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
	4.5	10	—	10	—	13	—	13	—	15	—	15	—	ns
	6	9	—	—	—	11	—	—	—	13	—	—	—	ns

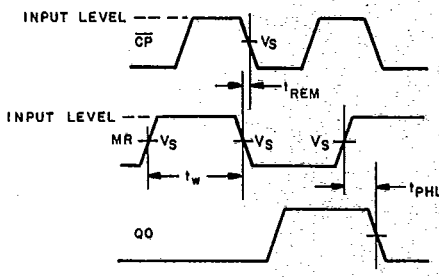
CD54/74HC93
CD54/74HCT93



	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3 V
SWITCHING VOLTAGE, V_S	50% V_{CC}	1.3 V

92CS-38370R2

Fig. 3 - Pre-requisite, propagation-delay, and output-transition times.



	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3 V
SWITCHING VOLTAGE, V_S	50%	1.3 V

92CS-38371R2

Fig. 4 - Master-Reset pre-requisite and propagation-delay times.

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC		V_{CC}	LIMITS												UNITS
			25°C				-40°C to +85°C				-55°C to +125°C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Time:	t_{PLH}	2	—	125	—	—	—	155	—	—	—	190	—	—	ns
	t_{PHL}	4.5	—	25	—	34	—	31	—	43	—	38	—	51	
$\overline{CP0}$ to Q0		6	—	21	—	—	—	26	—	—	—	32	—	—	
		2	—	135	—	—	—	170	—	—	—	205	—	—	
$\overline{CP1}$ to Q1		4.5	—	27	—	34	—	34	—	43	—	41	—	51	
		6	—	23	—	—	—	29	—	—	—	35	—	—	
		2	—	185	—	—	—	230	—	—	—	280	—	—	
$\overline{CP1}$ to Q2		4.5	—	37	—	46	—	46	—	58	—	56	—	69	
		6		31	—	—	—	39	—	—	—	48	—	—	
		2	—	245	—	—	—	305	—	—	—	370	—	—	
$\overline{CP1}$ to Q3		4.5	—	49	—	58	—	61	—	73	—	74	—	87	
		6	—	42	—	—	—	52	—	—	—	63	—	—	
		2	—	155	—	—	—	195	—	—	—	235	—	—	
MR1, MR2 to Qn		4.5	—	31	—	33	—	39	—	41	—	47	—	50	
		6	—	26	—	—	—	33	—	—	—	40	—	—	
Output Transition Time	t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	
	t_{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF