

128K x 36 SYNCHRONOUS PIPELINED STATIC RAM

ADVANCE INFORMATION
JUNE 1997

FEATURES

- Fast access time:
 - 3.5ns-166 MHz; 3.8ns-150 MHz;
 - 4ns-133 MHz; 5ns-100 MHz
- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Pentium™ or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining
- Common data inputs and data outputs
- JEDEC 100-Pin TQFP and 119-pin PBGA package
- Single +3.3V ± 10% power supply
- Power-down snooze mode

DESCRIPTION

The *ISSI* IS61SP12836 is a high-speed, low-power synchronous static RAM designed to provide a burstable, high-performance, secondary cache for the i486™, Pentium™, 680X0™, and PowerPC™ microprocessors. It is organized as 131,072 words by 36 bits, fabricated with *ISSI*'s advanced CMOS technology. The device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be from one to four bytes wide as controlled by the write control inputs.

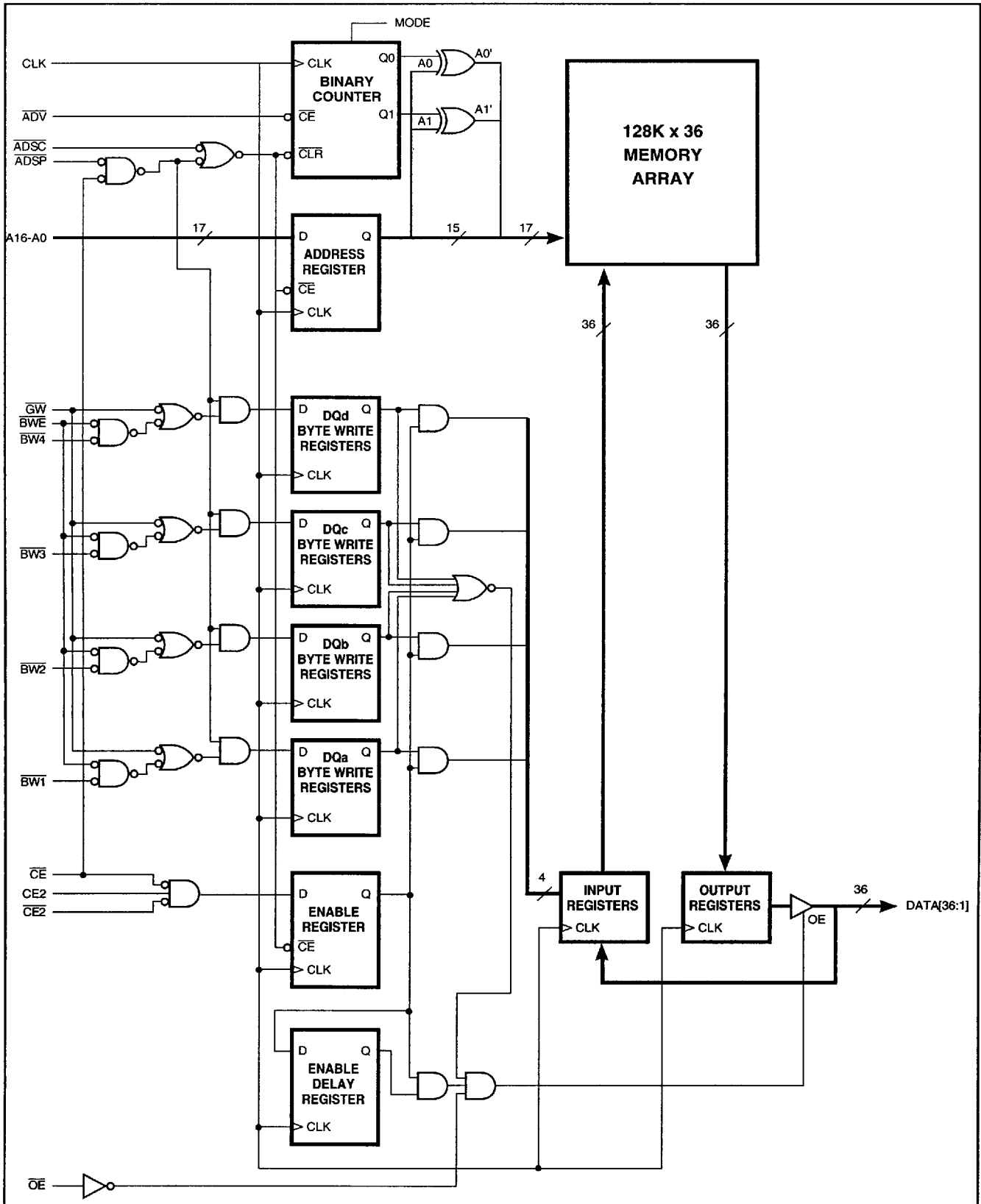
Separate byte enables allow individual bytes to be written. $\overline{BW1}$ controls DQa, $\overline{BW2}$ controls DQb, $\overline{BW3}$ controls DQc, $\overline{BW4}$ controls DQd, conditioned by \overline{BWE} being LOW. A LOW on \overline{GW} input would cause all bytes to be written.

Bursts can be initiated with either \overline{ADSP} (Address Status Processor) or \overline{ADSC} (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally by the IS61SP12836 and controlled by the \overline{ADV} (burst address advance) input pin.

The mode pin is used to select the burst sequence order, Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

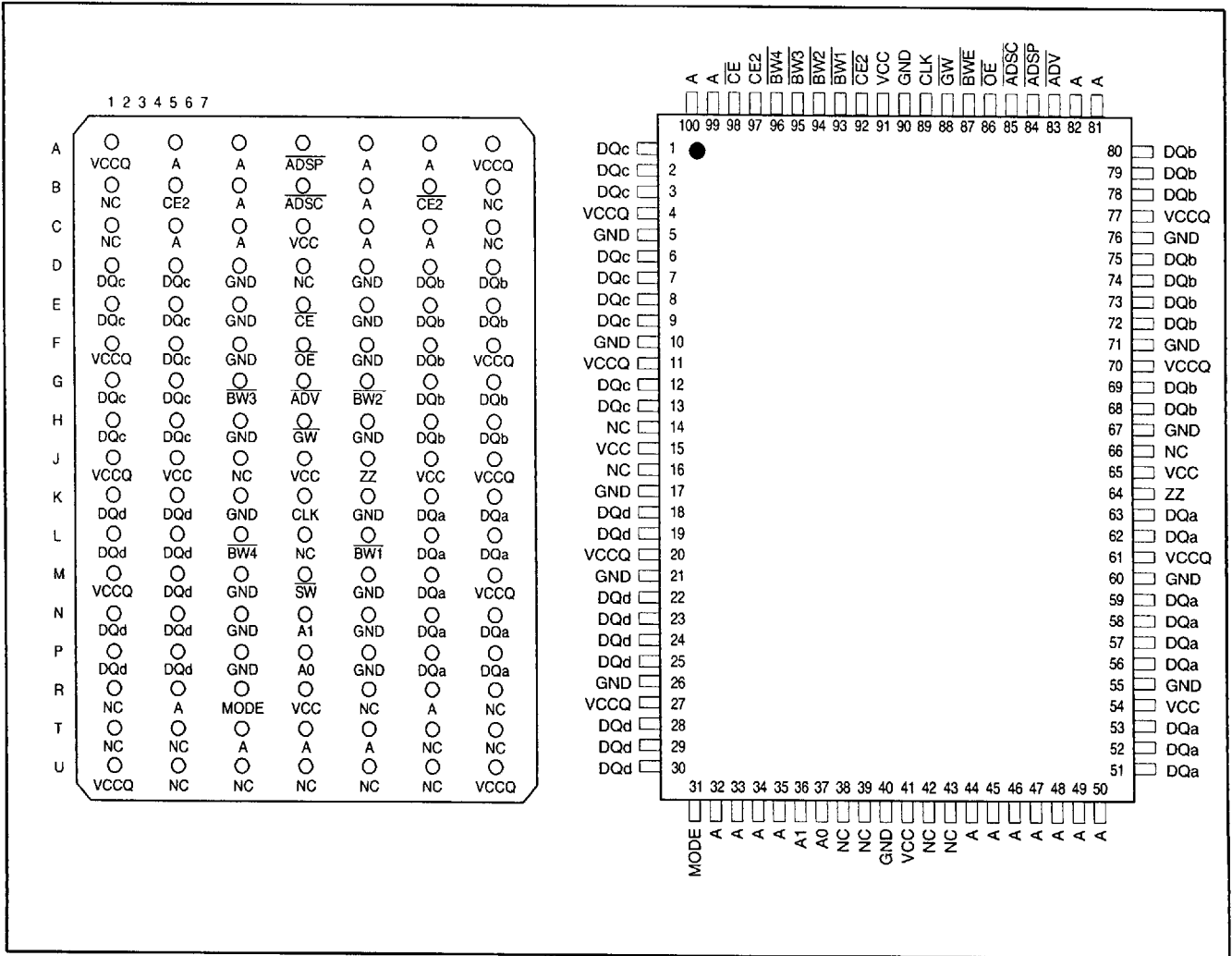
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BLOCK DIAGRAM



PIN CONFIGURATION

119-pin PBGA (Top View) and 100-Pin TQFP



PIN DESCRIPTIONS

| | | | |
|----------------------|--|--------------|--------------------------------------|
| A_0, A_1 | Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus. | GW | Synchronous Global Write Enable |
| A | Synchronous Address Inputs | CE, CE2, CE2 | Synchronous Chip Enable |
| CLK | Synchronous Clock | OE | Output Enable |
| \overline{ADSP} | Synchronous Processor Address Status | DQa-DQd | Synchronous Data Input/Output |
| \overline{ADSC} | Synchronous Controller Address Status | MODE | Burst Sequence Mode Selection |
| ADV | Synchronous Burst Address Advance | Vcc | +3.3V Power Supply |
| $\overline{BW1-BW4}$ | Synchronous Byte Write Enable | GND | Ground |
| \overline{BWE} | Synchronous Byte Write Enable | Vccq | Isolated Output Buffer Supply: +3.3V |
| | | ZZ | Snooze Enable |
| | | GNDq | Isolated Output Buffer Ground |

TRUTH TABLE

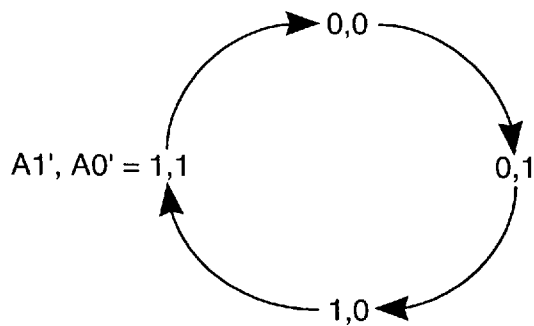
| OPERATION | ADDRESS USED | ADDRESS | | | | | | | | |
|-----------------------------|-----------------|-----------------|------------------|-----|-------------------|-------------------|------------------|--------------------|-----------------|--------|
| | | \overline{CE} | $\overline{CE2}$ | CE2 | \overline{ADSP} | \overline{ADSC} | \overline{ADV} | \overline{WRITE} | \overline{OE} | DQ |
| Deselected, Power-down | None | H | X | X | X | L | X | X | X | High-Z |
| Deselected, Power-down | None | L | X | H | L | X | X | X | X | High-Z |
| Deselected, Power-down | None | L | L | X | L | X | X | X | X | High-Z |
| Deselected, Power-down | None | X | X | H | H | L | X | X | X | High-Z |
| Deselected, Power-down | None | X | 0 | X | H | L | X | X | X | High-Z |
| Read Cycle, Begin Burst | External | L | H | L | L | X | X | X | X | High-Z |
| Read Cycle, Begin Burst | External | L | H | L | H | 0 | X | Read | X | High-Z |
| Write Cycle, Begin Burst | External | L | H | L | H | L | X | Write | X | High-Z |
| Read Cycle, Continue Burst | Next | X | X | X | H | H | L | Read | L | Q |
| Read Cycle, Continue Burst | Next | X | X | X | H | H | L | Read | H | High-Z |
| Read Cycle, Continue Burst | Next | H | X | X | X | H | L | Read | L | Q |
| Read Cycle, Continue Burst | Next | H | X | X | X | H | L | Read | H | High-Z |
| Write Cycle, Continue Burst | Next | X | X | X | H | H | L | Write | X | High-Z |
| Write Cycle, Continue Burst | Next | H | X | X | X | H | L | Write | X | High-Z |
| Read Cycle, Suspend Burst | Current | X | X | X | H | H | H | Read | L | Q |
| Read Cycle, Suspend Burst | Current | X | X | X | H | H | H | Read | H | High-Z |
| Read Cycle, Suspend Burst | Current | H | X | X | X | H | H | Read | L | Q |
| Read Cycle, Suspend Burst | Current | H | X | X | X | H | H | Read | H | High-Z |
| Write Cycle, Suspend Burst | Current | X | X | X | H | H | H | Write | X | High-Z |
| Write Cycle, Suspend Burst | Current | H | X | X | X | H | H | Write | X | High-Z |

PARTIAL TRUTH TABLE

| FUNCTION | \overline{GW} | \overline{BWE} | $\overline{BW1}$ | $\overline{BW2}$ | $\overline{BW3}$ | $\overline{BW4}$ |
|-----------------|-----------------|------------------|------------------|------------------|------------------|------------------|
| READ | H | H | X | X | X | X |
| READ | H | L | H | H | H | H |
| WRITE Byte 1 | H | L | L | H | H | H |
| WRITE All Bytes | H | L | L | L | L | L |
| WRITE All Bytes | L | X | X | X | X | X |

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{CCQ} or No Connect)

| External Address A1 A0 | 1st Burst Address A1 A0 | 2nd Burst Address A1 A0 | 3rd Burst Address A1 A0 |
|---------------------------|----------------------------|----------------------------|----------------------------|
| 00 | 01 | 10 | 11 |
| 01 | 00 | 11 | 10 |
| 10 | 11 | 00 | 01 |
| 11 | 10 | 01 | 00 |

LINEAR BURST ADDRESS TABLE (MODE = GND_Q)**ABSOLUTE MAXIMUM RATINGS⁽¹⁾**

| Symbol | Parameter | Value | Unit |
|------------------------------------|---|--------------------------------|------|
| T _{BIAS} | Temperature Under Bias | -40 to +85 | °C |
| T _{STG} | Storage Temperature | -55 to +150 | °C |
| P _D | Power Dissipation | 1.6 | W |
| I _{OUT} | Output Current (per I/O) | 100 | mA |
| V _{IN} , V _{OUT} | Voltage Relative to GND for I/O Pins | -0.5 to V _{CCQ} + 0.3 | V |
| V _{IN} | Voltage Relative to GND for for Address and Control Inputs | -0.5 to V _{CC} + 0.5 | V |
| V _{CC} | Voltage on V _{CC} Supply Relative to GND | -0.5 to 4.6 | V |

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE

| Range | Ambient Temperature | V _{CC} |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C | 3.3V ±10% |
| Industrial | -40°C to +85°C | 3.3V ±10% |

DC ELECTRICAL CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|-----------------|------------------------|--|--------------|------------------------|--------------|
| V _{OH} | Output HIGH Voltage | I _{OH} = -2.0 mA | 1.7 | — | V |
| V _{OL} | Output LOW Voltage | I _{OL} = 2.0 mA | — | 0.7 | V |
| V _{IH} | Input HIGH Voltage | | 1.7 | V _{CCQ} + 0.3 | V |
| V _{IL} | Input LOW Voltage | | -0.3 | 0.8 | V |
| I _{LI} | Input Leakage Current | GND ≤ V _{IN} ≤ V _{CCQ} ⁽²⁾ | Com. Ind. | -1 5 | 1 5 μA |
| I _{LO} | Output Leakage Current | GND ≤ V _{OUT} ≤ V _{CCQ} , $\overline{OE} = V_{IH}$ | Com. Ind. | -1 -5 | 1 5 μA |

POWER SUPPLY CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | Test Conditions | -3.5 | | -3.8 | | -4 | | -5 | | Unit | |
|-----------------|-----------------------------|---|------|------|------|------|------|------|------|------|------|----|
| | | | Typ. | Max. | Typ. | Max. | Typ. | Max. | Typ. | Max. | | |
| I _{CC} | AC Operating Supply Current | Device Selected, All Inputs = V _{IL} or V _{IH} $\overline{OE} = V_{IH}$, V _{CC} = Max. Cycle Time ≥ t _{kc} min. | Com. | 200 | 230 | 190 | 220 | 180 | 210 | 170 | 200 | mA |
| | | | Ind. | — | — | 200 | 230 | 190 | 220 | 180 | 210 | |
| I _{SB} | Standby Current | Device Deselected, V _{CC} = Max., All Inputs = V _{IH} or V _{IL} CLK Cycle Time ≥ t _{kc} min. | Com. | 45 | 70 | 45 | 70 | 45 | 70 | 45 | 65 | mA |
| | | | Ind. | — | — | 50 | 75 | 50 | 75 | 50 | 70 | |
| I _{ZZ} | Power-down Mode Current | ZZ = V _{CCQ} Clock Running All Inputs ≤ GND + 0.2V or ≥ V _{CC} - 0.2V | Com. | — | 5 | — | 5 | — | 5 | — | 5 | mA |
| | | | Ind. | — | 5 | — | 5 | — | 5 | — | 5 | |

Note:

- The MODE pin has an internal pullup. This pin may be a No Connect, tied to GND, or tied to V_{CCQ}.
- The MODE pin should be tied to V_{CC} or GND. It exhibits ±10 μA maximum leakage current when tied to ≤ GND + 0.2V or ≥ V_{CC} - 0.2V.

CAPACITANCE^(1,2)

| Symbol | Parameter | Conditions | Max. | Unit |
|-----------|--------------------------|----------------|------|------|
| C_{IN} | Input Capacitance | $V_{IN} = 0V$ | 5 | pF |
| C_{OUT} | Input/Output Capacitance | $V_{OUT} = 0V$ | 8 | pF |

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: $T_A = 25^\circ C$, $f = 1 \text{ MHz}$, $V_{CC} = 3.3V$.

AC TEST CONDITIONS

| Parameter | Unit |
|---|---------------------|
| Input Pulse Level | 0V to 3.0V |
| Input Rise and Fall Times | 1.5 ns |
| Input and Output Timing and Reference Level | 1.5V |
| Output Load | See Figures 1 and 2 |

AC TEST LOADS

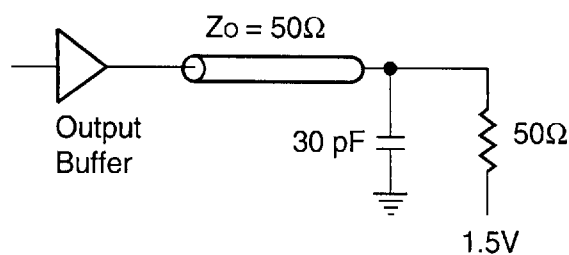


Figure 1

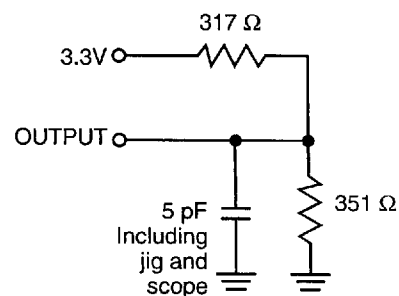


Figure 2

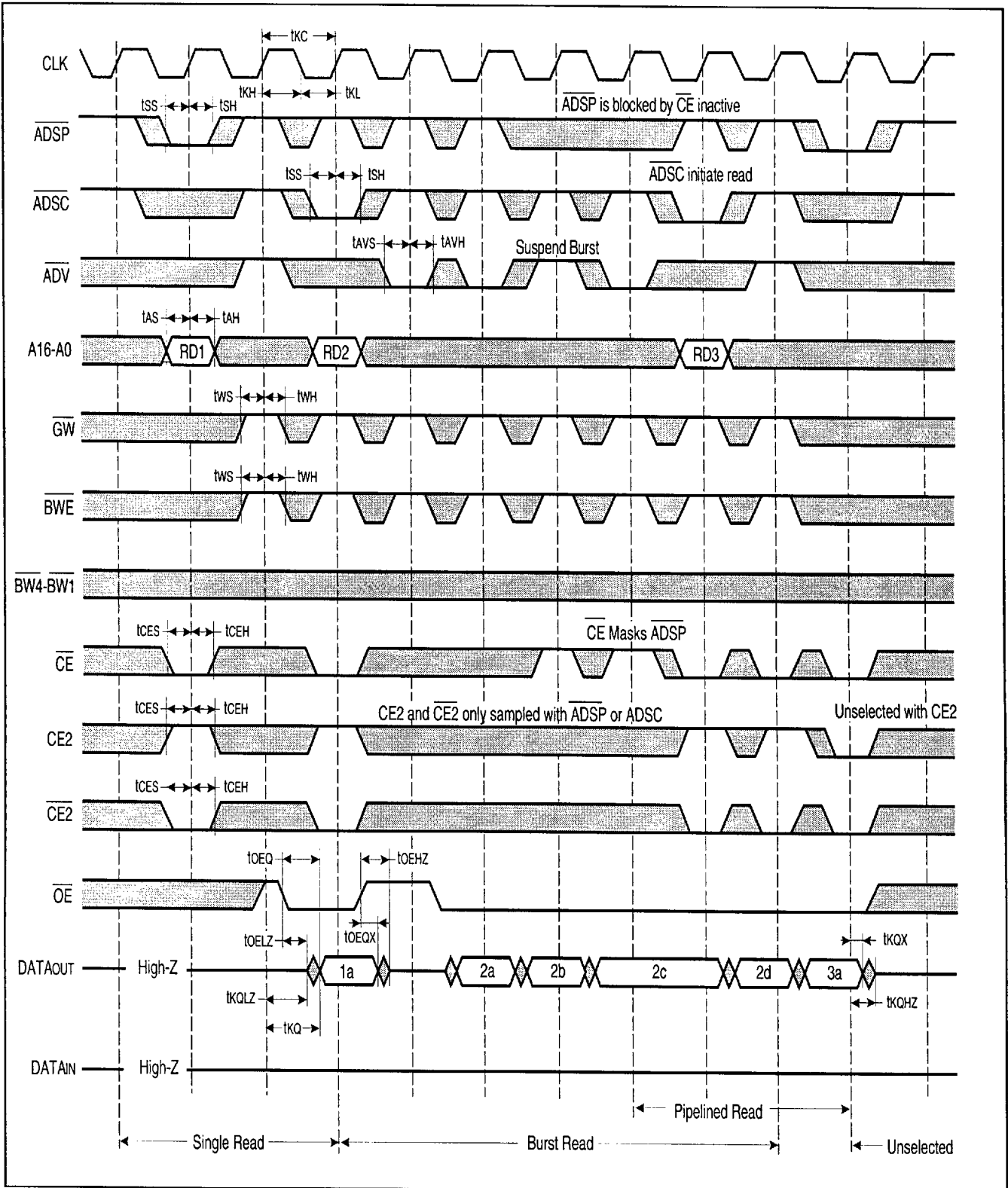
READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | 3.5 | | 3.8 | | 4 | | 5 | | Unit |
|----------------------|----------------------------------|------|---------|------|--------|------|---------|------|---------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| fMAX | Clock Frequency | — | 166 MHz | — | 150MHz | — | 133 MHz | — | 100 MHz | — |
| tkc | Cycle Time | 6 | — | 6.7 | — | 7.5 | — | 10 | — | ns |
| tkH | Clock High Time | 2.4 | — | 2.6 | — | 2.8 | — | 4 | — | ns |
| tkL | Clock Low Time | 2.4 | — | 2.6 | — | 2.8 | — | 4 | — | ns |
| tkQ | Clock Access Time | — | 3.5 | — | 3.8 | — | 4 | — | 5 | ns |
| tkQX ⁽¹⁾ | Clock High to Output Invalid | 1.5 | — | 1.5 | — | 1.5 | — | 2.5 | — | ns |
| tkQLZ ⁽¹⁾ | Clock High to Output Low-Z | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| tkQHZ ⁽¹⁾ | Clock High to Output High-Z | 1.5 | 6 | 1.5 | 6.7 | 1.5 | 7.5 | 1.5 | 10 | ns |
| toEQ | Output Enable to Output Valid | — | 3.5 | — | 3.5 | — | 3.8 | — | 5 | ns |
| toEQX ⁽¹⁾ | Output Disable to Output Invalid | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| toELZ ⁽¹⁾ | Output Enable to Output Low-Z | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| toEHZ ⁽¹⁾ | Output Disable to Output High-Z | 2 | 3.5 | 2 | 3.5 | 2 | 3.8 | 2 | 5 | ns |
| tAS | Address Setup Time | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| tSS | Address Status Setup Time | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| tWS | Write Setup Time | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| tCES | Chip Enable Setup Time | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| tAVS | Address Advance Setup Time | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| tAH | Address Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| tSH | Address Status Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| tWH | Write Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| tCEH | Chip Enable Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| tAVH | Address Advance Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |

Note:

1. Guaranteed but not 100% tested. This parameter is periodically sampled.

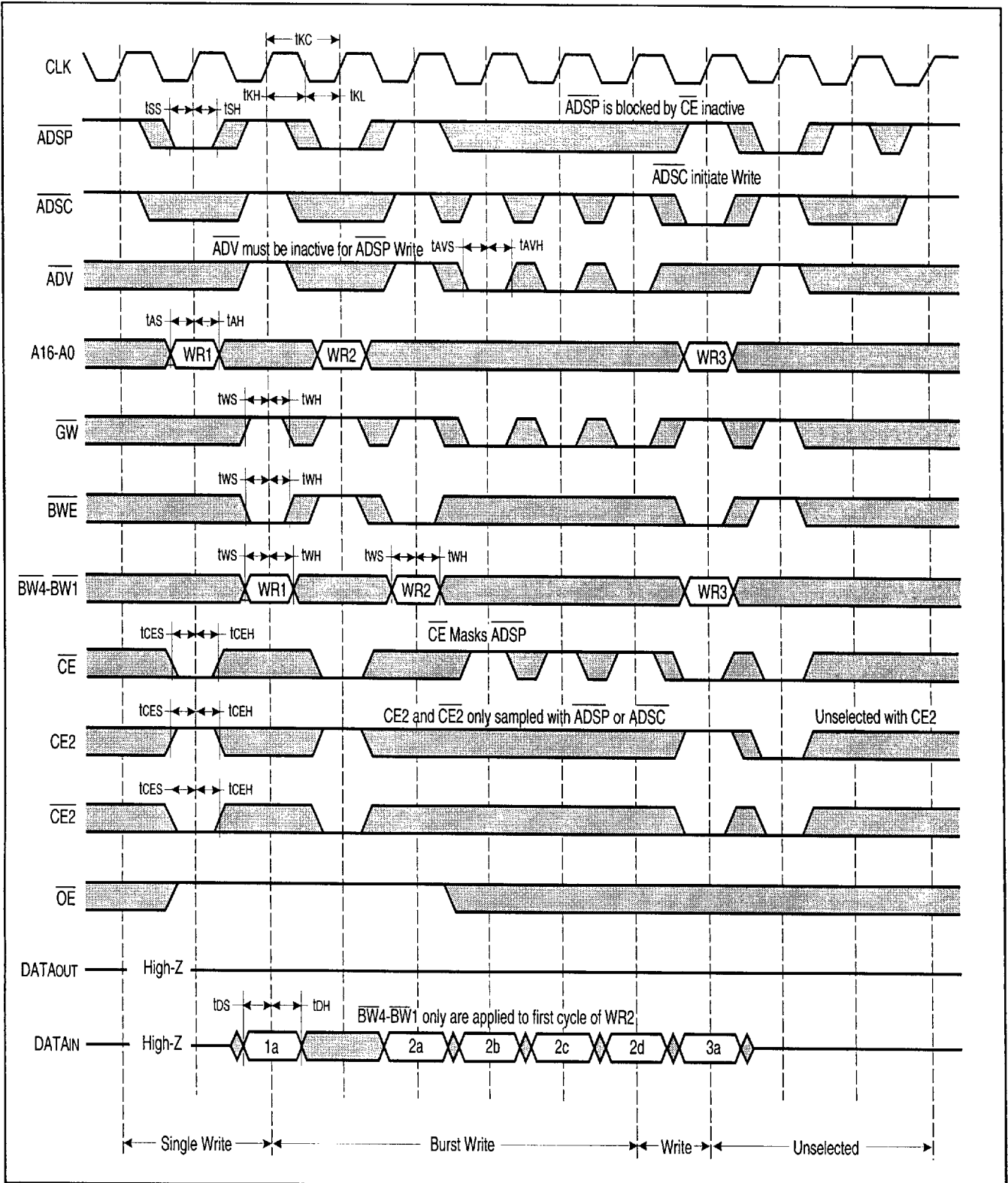
READ/WRITE CYCLE TIMING



WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | 3.5 | | 3.8 | | 4 | | 5 | | Unit |
|------------------|----------------------------|------|------|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{KC} | Cycle Time | 6 | — | 6.7 | — | 7.5 | — | 10 | — | ns |
| t _{KH} | Clock High Time | 2.4 | — | 2.6 | — | 2.8 | — | 4 | — | ns |
| t _{KL} | Clock Low Time | 2.4 | — | 2.6 | — | 2.8 | — | 4 | — | ns |
| t _{AS} | Address Setup Time | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| t _{SS} | Address Status Setup Time | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| t _{WS} | Write Setup Time | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| t _{DS} | Data In Setup Time | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| t _{CES} | Chip Enable Setup Time | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| t _{AVS} | Address Advance Setup Time | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| t _{AH} | Address Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{SH} | Address Status Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{DH} | Data In Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{WH} | Write Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{CEH} | Chip Enable Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{AVH} | Address Advance Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |

WRITE CYCLE TIMING



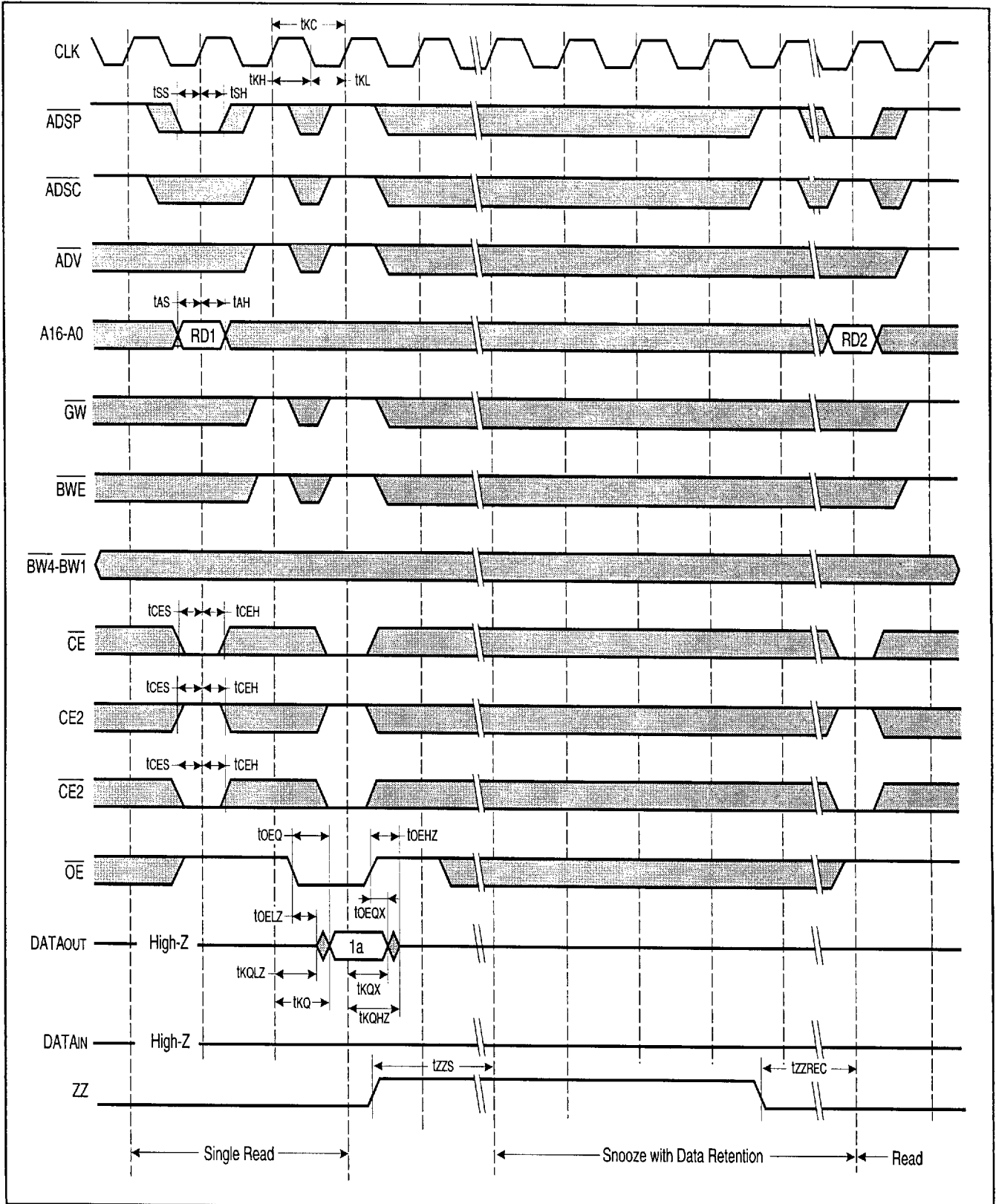
SNOOZE AND RECOVERY CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | 3.5 | | 3.8 | | 4 | | 5 | | Unit |
|----------------------------------|----------------------------------|------|------|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{KC} | Cycle Time | 6 | — | 6.7 | — | 7.5 | — | 10 | — | ns |
| t _{KH} | Clock High Time | 2.4 | — | 2.6 | — | 2.8 | — | 4 | — | ns |
| t _{KL} | Clock Low Time | 2.4 | — | 2.6 | — | 2.8 | — | 4 | — | ns |
| t _{KQ} | Clock Access Time | — | 3.5 | — | 3.8 | — | 4 | — | 5 | ns |
| t _{KQX} ⁽¹⁾ | Clock High to Output Invalid | 1.5 | — | 1.5 | — | 1.5 | — | 2.5 | — | ns |
| t _{KQLZ} ⁽¹⁾ | Clock High to Output Low-Z | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{KQHZ} ⁽¹⁾ | Clock High to Output High-Z | 1.5 | 3.6 | 1.5 | 6.7 | 1.5 | 7.5 | 1.5 | 10 | ns |
| t _{OEQ} | Output Enable to Output Valid | — | 3.5 | — | 3.5 | — | 3.9 | — | 5 | ns |
| t _{OEQX} ⁽¹⁾ | Output Disable to Output Invalid | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{OELZ} ⁽¹⁾ | Output Enable to Output Low-Z | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{OEHZ} ⁽¹⁾ | Output Disable to Output High-Z | 2 | 3.5 | 2 | 3.5 | 2 | 3.8 | 2 | 5 | ns |
| t _{AS} | Address Setup Time | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| t _{SS} | Address Status Setup Time | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| t _{CES} | Chip Enable Setup Time | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| t _{AH} | Address Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{SH} | Address Status Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{CEH} | Chip Enable Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{ZZS} | ZZ Standby | — | 2 | — | 2 | — | 2 | — | 2 | ns |
| t _{ZZREC} | ZZ Recovery | 2 | — | 2 | — | 2 | — | 2 | — | ns |

Notes:

1. Guaranteed but not 100% tested. This parameter is periodically sampled.

SNOOZE AND RECOVERY CYCLE TIMING



ORDERING INFORMATION**Commercial Range: 0°C to +70°C**

| Speed (ns) | Order Part Number | Package |
|------------|-------------------|---------|
| 3.5 | IS61SP12836-3.5TQ | TQFP |
| | IS61SP12836-3.5B | PBGA |
| 3.8 | IS61SP12836-3.8TQ | TQFP |
| | IS61SP12836-3.8B | PBGA |
| 4 | IS61SP12836-4TQ | TQFP |
| | IS61SP12836-4B | PBGA |
| 5 | IS61SP12836-5TQ | TQFP |
| | IS61SP12836-5B | PBGA |

Industrial Range: -40°C to +85°C

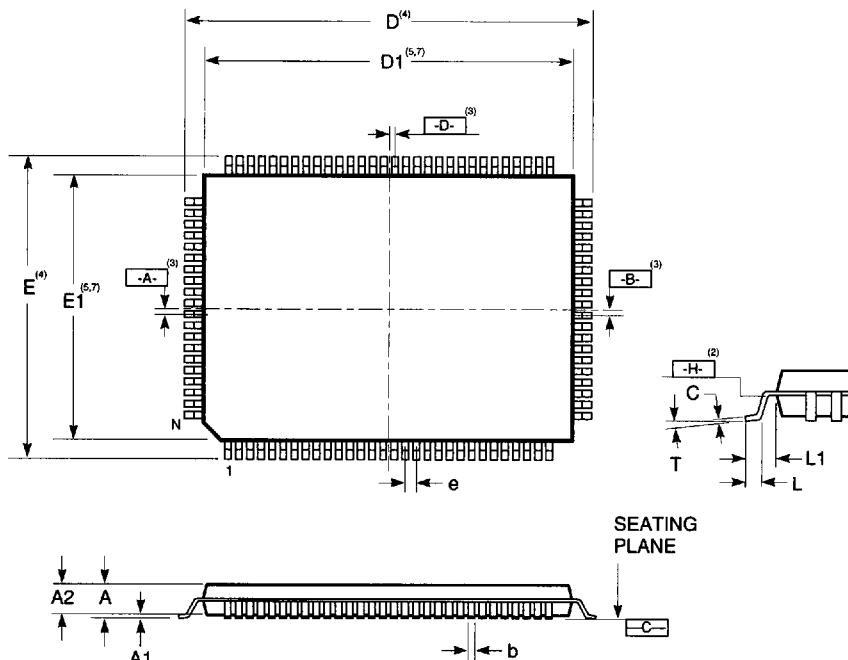
| Speed (ns) | Order Part Number | Package |
|------------|--------------------|---------|
| 3.8 | IS61SP12836-3.8TQI | TQFP |
| 4 | IS61SP12836-4TQI | TQFP |
| 5 | IS61SP12836-5TQI | TQFP |

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<http://www.issiusa.com>

TQFP (Thin Quad Flat Pack Package)

Package Code: TQ



Thin Quad Flatpack (TQFP)

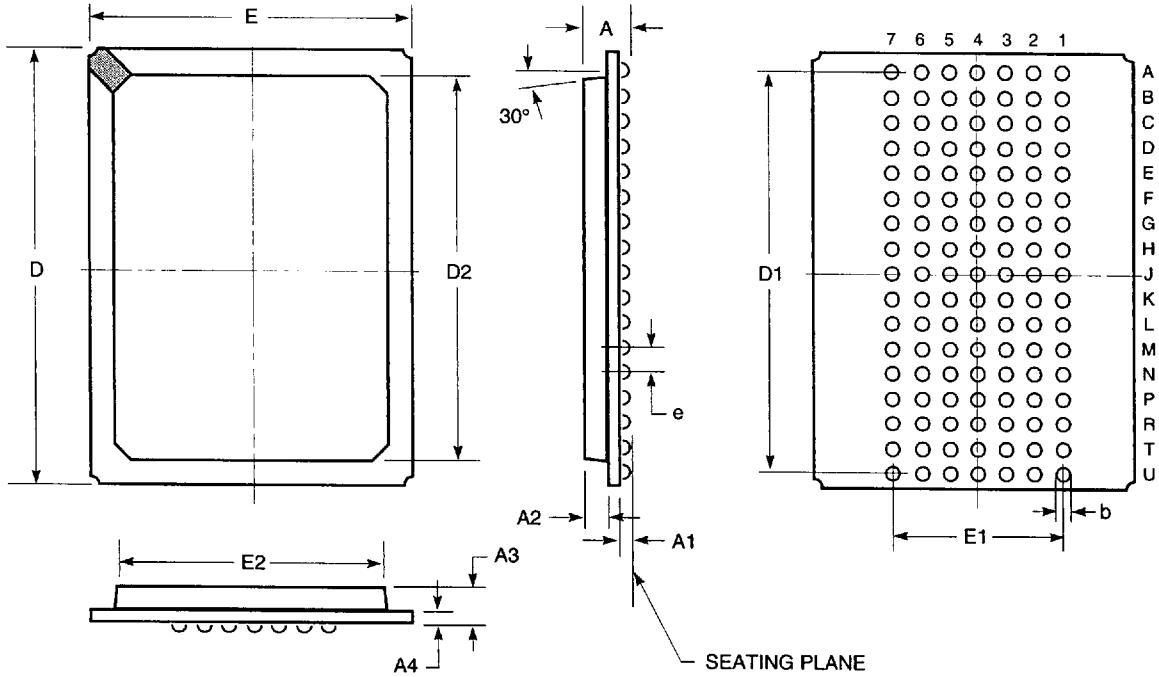
inches

| Symbol | Min | Max |
|-----------|-------|-------|
| Ref. Std. | | |
| No. Leads | 100 | |
| A | 0.055 | 0.063 |
| A1 | 0.002 | 0.006 |
| A2 | 0.053 | 0.057 |
| b | 0.009 | 0.015 |
| C | 0.004 | 0.008 |
| D | 0.862 | 0.870 |
| D1 | 0.783 | 0.791 |
| E | 0.626 | 0.634 |
| E1 | 0.547 | 0.555 |
| e | 0.026 | |
| L | 0.018 | 0.030 |
| L1 | 0.039 | Ref. |
| T | 0° | 10° |

Notes:

1. All dimensioning and tolerancing conforms to ANSI Y14.5M-1982.
2. Datum plane -H- located at bottom of lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
3. Datums -A-, -B-, and -D- to be determined at datum plane -H- where the center two leads exit the plastic body.
4. To be determined at seating plane -C-.
5. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 do include mold mismatch and are determined at datum plane -H-.
6. Details of pin 1 identifier are optional.
7. These dimensions to be determined at datum plane -H-.
8. Controlling dimension: inches.

Plastic Ball Grid Array
 Package Code: B



| Plastic Ball Grid Array (B) | | |
|-----------------------------|-----------|-------|
| Millimeters | | |
| Symbol | Min | Max |
| Ref. Std. | | |
| No. Leads | 119 | |
| A | — | 2.41 |
| A1 | 0.50 | 0.70 |
| A2 | 0.80 | 1.00 |
| A3 | 1.30 | 1.70 |
| A4 | 0.56 BSC | |
| b | 0.60 | 0.90 |
| D | 21.80 | 22.20 |
| D1 | 20.32 BSC | |
| D2 | 19.40 | 19.60 |
| E | 13.80 | 14.20 |
| E1 | 7.62 BSC | |
| E2 | 11.90 | 12.10 |
| e | 1.27 BSC | |