REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add generic part number HA-2841 as device type 03. Add case outline C to device type 01. Make changes to 1.2.1, 1.3, TABLE I, and FIGURE 2.	94-05-16	M. A. FRYE
B	Drawing updated to reflect current requirements. - ro	00-05-24	R. MONNIN
C	Replaced reference to MIL-STD-973 with reference to MIL-PRF-38535. Drawing updated to reflect current requirements. - gt	04-06-09	R. MONNIN

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV																				
SHEET																				
REV STATUS				REV			C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
RICK C. OFFICER

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH R. PITHADIA

APPROVED BY
MICHAEL A. FRYE

DRAWING APPROVAL DATE
90-06-28

MICROCIRCUIT, LINEAR, WIDEBAND, FAST SETTLING, OPERATIONAL AMPLIFIER, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
C	A	**67268**	**5962-87785**

SHEET 1 OF 14

DSCC FORM 2233
APR 97

5962-E277-04

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-87785	01	C	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HA-2541	Fast settling, unity gain stable, wideband operational amplifier
02	EL-2041	Fast settling, unity gain stable, wideband operational amplifier
03	HA-2841	Fast settling, unity gain stable, video operational amplifier

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line package
P	GDIP1-T8 or CDIP2-T8	8	Dual-in-line package
X	See figure 1	12	Can
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Voltage between +V and -V terminals ..... 35 V dc
Differential input voltage (V_{IN}) ..... ±6.0 V dc
Voltage at either input terminal ..... V+ to V-
Peak output current (< 10% duty cycle) ..... 50 mA
Maximum power dissipation (P_D) ..... 2.0 W 1/
Storage temperature range ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) :
  Device types 01 and 02 ..... +275°C
  Device type 03 ..... +300°C
Junction temperature (T_J) ..... +175°C
Thermal resistance, junction-to-case (θ_{JC}) :
  Cases C, P, and 2 ..... See MIL-STD-1835
  Case X ..... 82°C/W
Thermal resistance, junction-to-ambient (θ_{JA}): ..... 50°C/W

1/ Derate linearly above T_A = +75°C at 20 mW/°C.

1.4 Recommended operating conditions.

Positive supply voltage range (+V) ..... +12 V dc to +15 V dc
Negative supply voltage range (-V) ..... -12 V dc to -15 V dc
Common mode input voltage (V_{CM}) ..... ≤ (+V – (-V)) / 2
Load resistance (R_L) ..... 1.0 kΩ
Ambient operating temperature range (T_A) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or www.dodssp.daps.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input offset voltage	V_{IO}	V_{CM} = 0 V	1	01,02	-2.0	+2.0	mV
				03	-4.0	+4.0	
			2,3	01	-6.0	+6.0	
				02	-10.0	+10.0	
				03	-8.0	+8.0	
Input bias current	$+I_{IB}$	V_{CM} = 0 V, $+R_S$ = 1.1 kΩ, $-R_S$ = 100 Ω	1	01	-35	+35	µA
			2,3		-50	+50	
			1	02	-15	+15	
			2,3		-20	+20	
			1	03	-10	+10	
			2,3		-20	+20	
	$-I_{IB}$	V_{CM} = 0 V, $+R_S$ = 100 Ω, $-R_S$ = 1.1 kΩ	1	01	-35	+35	
			2,3		-50	+50	
			1	02	-15	+15	
			2,3		-20	+20	
			1	03	-10	+10	
			2,3		-20	+20	
Input offset current	I_{IO}	V_{CM} = 0 V, $+R_S$ = 1.1 kΩ, $-R_S$ = 1.1 kΩ	1	01	-7.0	+7.0	µA
			2,3		-9.0	+9.0	
			1	02	-4.0	+4.0	
			2,3		-6.0	+6.0	
			1	03	-1.0	+1.0	
			2,3		-2.0	+2.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Common mode input range	$+V_{CM}$	+V = 5.0 V, -V = -25 V	1,2,3	01,03	10		V
				02	8		
	$-V_{CM}$	+V = 25 V, -V = -5.0 V		01,03	-10		
				02	-8		
Large signal voltage range	$+A_{VOL}$	V_{OUT} = 0 V and 10 V, R_L = 1.0 kΩ	4	01,03	10		kV/V
				02	7		
			5,6	All	5		
	$-A_{VOL}$	V_{OUT} = 0 V and -10 V, R_L = 1.0 kΩ	4	01,03	10		
				02	7		
			5,6	All	5		
Common mode rejection ratio	+CMRR	ΔV_{CM} = 10 V, -V = -25 V, +V = 5.0 V, V_{OUT} = -10 V	1,2,3	01,02	70		dB
			1	03	86		
			2,3		80		
	-CMRR	ΔV_{CM} = -10 V, +V = 25 V, -V = -5.0 V, V_{OUT} = 10 V	1,2,3	01,02	70		
			1	03	86		
			2,3		80		
Output current	$+I_{OUT}$	V_{OUT} = -10 V	1	01	10		mA
				02	25		
		V_{OUT} = -5 V 2/	1	03	25		
			2,3		15		
	$-I_{OUT}$	V_{OUT} = 10 V	1	01	-10		
				02	-25		
		V_{OUT} = +5 V 2/	1	03	-25		
			2,3		-15		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output voltage swing	$+V_{OUT}$	R_L = 1.0 kΩ	1,2,3	01,03	10		V
				02	11		
	$-V_{OUT}$	R_L = 1.0 kΩ	1,2,3	01,03	-10		
				02	-11		
Quiescent power supply current	$+I_{CC}$	V_{OUT} = 0 V, I_{OUT} = 0 mA	1,2,3	01		39	mA
				02		17	
				03		11	
	$-I_{CC}$	V_{OUT} = 0 V, I_{OUT} = 0 mA	1,2,3	01		-39	
				02		-17	
				03		-11	
Power supply rejection ratio	+PSRR	+V = 5.0 and 15 V, -V = -15 V	1,2,3	01	70		dB
				02	60		
		+V = 10 and 20 V, -V = -15 V		03	70		
	-PSRR	-V = -5.0 V and -15 V, +V = +15 V	1,2,3	01	70		
				02	60		
		-V = -10 and -20 V, +V = +15 V		03	70		
Offset voltage adjustment	$+V_{IO}$ (adj)	T_A = +25°C 3/	1	All	V_{IO} -1.0		mV
	$-V_{IO}$ (adj)	T_A = +25°C 3/	1	All	V_{IO} +1.0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Differential input 4/ resistance	R_{IN}	V_{CM} = 0 V, T_A = +25°C	4	01,02	40		kΩ
Slew rate 4/	+SR	V_{OUT} = -3.0 V to 3.0 V,	7	01	200		V/µs
		R_L = 1 kΩ, A_V = 1 V/V	8		150		
	-SR	V_{OUT} = 3.0 V to -3.0 V,	7		200		
		R_L = 1 kΩ, A_V = 1 V/V	8		150		
	+SR	V_{OUT} = -3.0 V to 3.0 V,	7	02	180		
		R_L = 1 kΩ, A_V = 1 V/V	8		130		
	-SR	V_{OUT} = 3.0 V to -3.0 V,	7		180		
		R_L = 1 kΩ, A_V = 1 V/V	8		130		
	+SR	V_{OUT} = -3.0 V to 3.0 V,	7	03	200		
		R_L = 1 kΩ, A_V = 1 V/V	8		187		
	-SR	V_{OUT} = 3.0 V to -3.0 V,	7		200		
		R_L = 1 kΩ, A_V = 1 V/V	8		187		
Gain bandwidth 4/ product	GBWP	V_{OUT} = ±100 mV, R_L = 1 kΩ, f_1 = 100 kHz, f_2 = 10 MHz, T_A = +25°C	4	All	38		MHz
		V_{OUT} = ±200 mV, R_L = 1 kΩ, f_O = 100 kHz, T_A = +25°C		03	42		
		V_{OUT} = ±200 mV, R_L = 1 kΩ, f_O = 10 MHz, T_A = +25°C			44		
Full power bandwidth 4/ 5/	FPBW	V_{PK} = 10 V, R_L = 1 kΩ	4	01	3.0		MHz
			5,6		2.4		
			4	02	2.8		
			5,6		2.0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Full power bandwidth 4/ 5/	FPBW	V_{PK} = 10 V, R_L = 1 kΩ	4	03	3.1		MHz
			5,6		3.0		
Closed loop stable gain 4/	CLSG	R_L = 1 kΩ, $C_L \le 10$ pF	4,5,6	All	1.0		V/V
Rise time 4/ 6/	t_r	V_{OUT} = 0 V to +200 mV	9,10,11	01,02		10	ns
				03		6	
Fall time 4/ 6/	t_f	V_{OUT} = 0 V to –200 mV	9,10,11	01,02		10	ns
			9	03		5	
			10,11			6	
Settling time 4/	t_s	A_V = -1 V/V, 10 V step to 0.1 %, T_A = +25°C	9	01		150	ns
		A_V = -1 V/V, 10 V step to 0.01 %, T_A = +25°C				300	
		A_V = -1 V/V, 10 V step to 0.05 %, T_A = +25°C	9	02		350	
Overshoot 4/	+OS	V_{OUT} = 0 V to +200 mV	9,10,11	01,02		40	%
			9	03		60	
			10,11			65	
	-OS	V_{OUT} = 0 V to –200 mV	9,10,11	01,02		40	
			9	03		60	
			10,11			70	
Output resistance 4/	R_{OUT}	Open loop, T_A = +25°C	4	01,02		25	Ω
Quiescent power consumption 7/	P_C	V_{OUT} = 0 V, I_{OUT} = 0 mA	1,2,3	01		1.17	W
				02		.51	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

1/ Unless otherwise specified, for dc tests, R_S = 100 Ω, R_L = 100 kΩ, V_{OUT} = 0 V. Unless otherwise specified, for ac tests, A_V = ±1 V/V and R_L = 1 kΩ.

2/ Device type 03 is designed to handle I_{OUT} = 10 mA at a 50 % duty cycle for T_J = +175°C. For I_{OUT} = 15 mA and T_J = +175°C, a duty cycle of less than or equal to 33 % is required.

3/ Offset adjustment range is V_{IO} (measured) ±1.0 mV minimum referred to output. This test is for functionality only to assure adjustment through 0 V.

4/ If not tested, shall be guaranteed to the limits specified in table I herein.

5/ Full power bandwidth = SR / (2 x π x V_{PK}).

6/ Rise and fall times measured between 10 percent and 90 percent point.

7/ Quiescent power consumption is based on quiescent supply current test maximum (no load outputs).

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

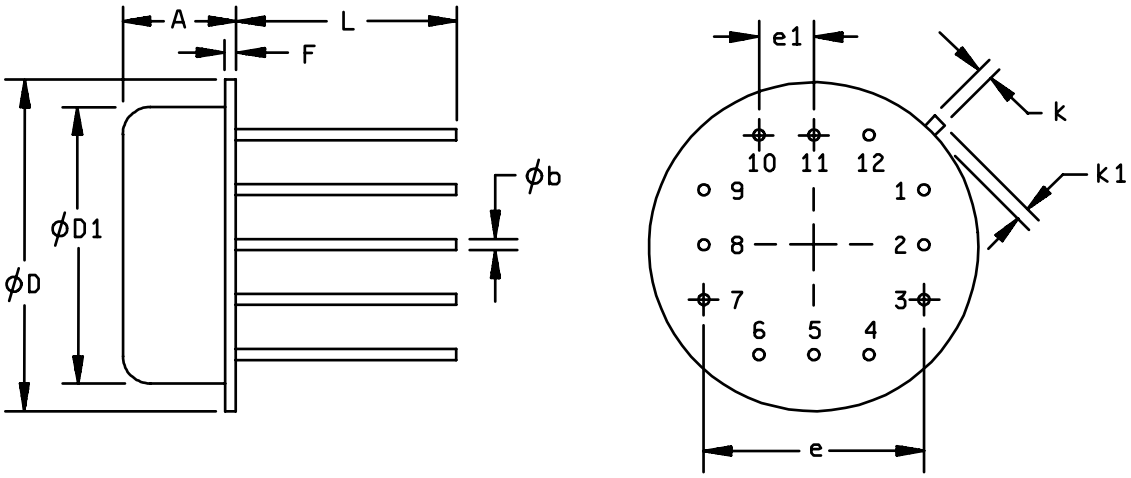
b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

Case X



Letter	Inches		Millimeters	
	Min	Max	Min	Max
A	.130	.150	3.30	3.81
ϕb	.016	.021	0.41	0.53
ϕD	.585	.615	14.86	15.62
ϕD1	.545	.555	13.84	14.10
e	.400 BSC		10.16 BSC	
e1	.100 BSC		2.54 BSC	
F	.020	.040	0.51	1.02
k	.027	.034	0.69	0.86
k1	.027	.045	0.69	1.14
L	.505	.562	12.83	14.27

NOTES: 1. The US government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
2. Pin numbers are for reference only and do not appear on package.

FIGURE 1. Case outline.

Device types	01 and 02	01, 02, and 03	02	03
Case outlines	X	C	2	P
Terminal number	Terminal symbol			
1	NC	NC	NC	BAL
2	NC	NC	BAL	-IN
3	BAL	BAL	NC	+IN
4	BAL	-IN	NC	-V
5	-IN	+IN	-IN	NC
6	+IN	-V	NC	OUT
7	NC	NC	+IN	+V
8	NC	NC	NC	BAL
9	NC	NC	NC	---
10	-V	OUTPUT	-V	---
11	OUTPUT	+V	NC	---
12	+V	BAL	NC	---
13	---	NC	NC	---
14	---	NC	NC	---
15	---	---	OUT	---
16	---	---	NC	---
17	---	---	+V	---
18	---	---	NC	---
19	---	---	NC	---
20	---	---	BAL	---

NC = No connection

FIGURE 1. Terminal connections.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2,3,4,5,6
Group A test requirements (method 5005)	1,2,3,4,5,6,7**,8**,9**10**,11**
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** Subgroups 7, 8, 9, 10, and 11, if not tested, shall be guaranteed to the limits specified in table I herein.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 04-06-09

Approved sources of supply for SMD 5962-87785 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-383535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8778501CA	34371	HA1-2541/883
5962-8778501XA	3/	HA2-2541/883
5962-8778501XC	34371	HA2-2541/883
5962-8778502CA	3/	EL2041J/883B
5962-8778502XA	3/	EL2041G/883B
5962-87785022A	3/	EL2041L/883B
5962-8778503CA	34371	HA1-2841/883
5962-8778503PA	3/	HA7-2841/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from approved source of supply.

Vendor CAGE number	Vendor name and address
34371	Intersil Corporation 2401 Palm Bay Blvd PO Box 883 Melbourne, FL 32902-0883