

## MSM51V16165B/BSL

**1,048,576-Word × 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO**

### DESCRIPTION

The MSM51V16165B/BSL is a 1,048,576-word × 16-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM51V16165B/BSL achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/double-layer metal CMOS process. The MSM51V16165B/BSL is available in a 42-pin plastic SOJ or 50/44-pin plastic TSOP. The MSM51V16165BSL (the self-refresh version) is specially designed for lower-power applications.

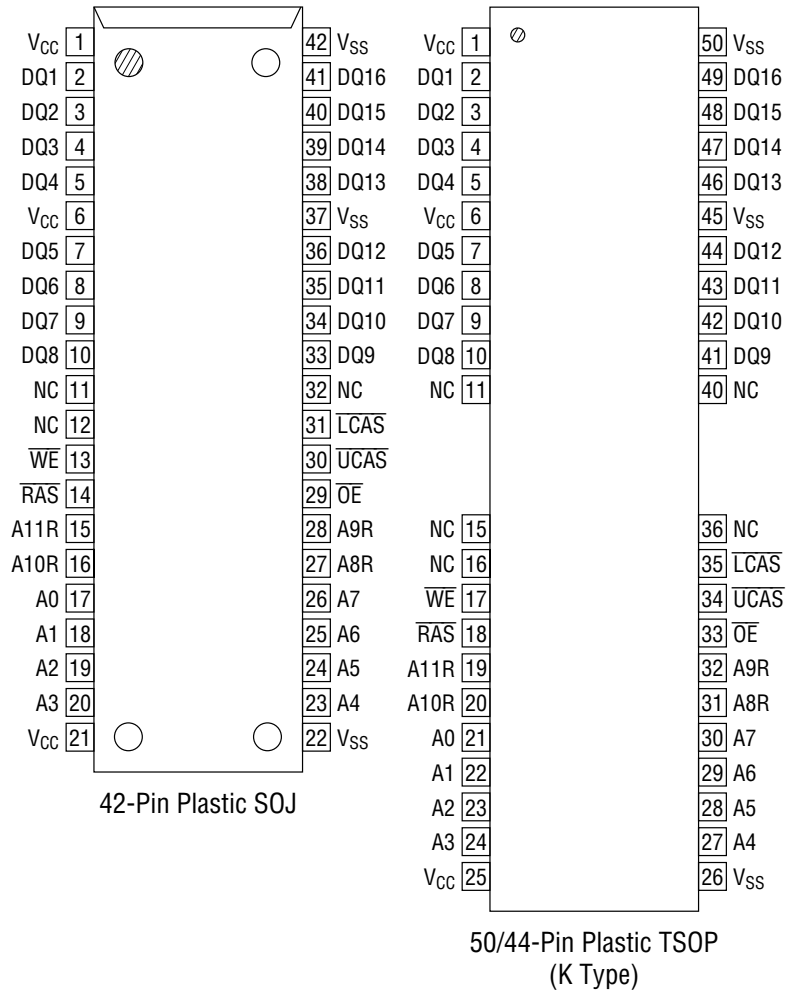
### FEATURES

- 1,048,576-word × 16-bit configuration
  - Single 3.3 V power supply, ±0.3 V tolerance
  - Input : LVTTTL compatible, low input capacitance
  - Output : LVTTTL compatible, 3-state
  - Refresh : 4096 cycles/64 ms, 4096 cycles/128 ms (SL version)
  - Fast page mode with EDO, read modify write capability
  - $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh, hidden refresh,  $\overline{\text{RAS}}$ -only refresh capability
  - $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  self-refresh capability (SL version)
  - Package options:
    - 42-pin 400 mil plastic SOJ (SOJ42-P-400-1.27) (Product : MSM51V16165B/BSL-xxJS)
    - 50/44-pin 400 mil plastic TSOP (TSOPII50/44-P-400-0.80-K) (Product : MSM51V16165B/BSL-xxTS-K)
- xx indicates speed rank.

### PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t <sub>RAC</sub>	t <sub>AA</sub>	t <sub>CAC</sub>	t <sub>OEA</sub>		Operating (Max.)	Standby (Max.)
MSM51V16165B/BSL-50	50 ns	25 ns	13 ns	13 ns	84 ns	576 mW	1.8 mW/ 0.72 mW (SL version)
MSM51V16165B/BSL-60	60 ns	30 ns	15 ns	15 ns	104 ns	468 mW	
MSM51V16165B/BSL-70	70 ns	35 ns	20 ns	20 ns	124 ns	396 mW	

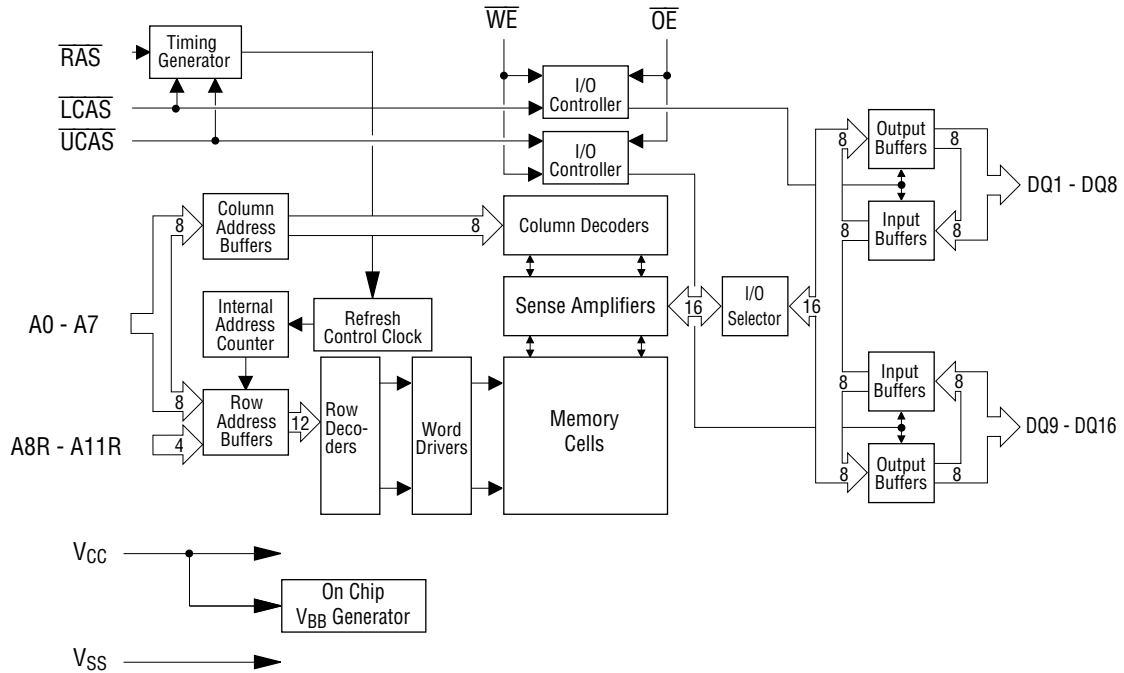
**PIN CONFIGURATION (TOP VIEW)**



Pin Name	Function
A0 - A7, A8R - A11R	Address Input
RAS	Row Address Strobe
LCAS	Lower Byte Column Address Strobe
UCAS	Upper Byte Column Address Strobe
DQ1 - DQ16	Data Input/Data Output
OE	Output Enable
WE	Write Enable
V <sub>CC</sub>	Power Supply (3.3 V)
V <sub>SS</sub>	Ground (0 V)
NC	No Connection

Note : The same power supply voltage must be provided to every V<sub>CC</sub> pin, and the same GND voltage level must be provided to every V<sub>SS</sub> pin.

**BLOCK DIAGRAM**



**FUNCTION TABLE**

Input Pin					DQ Pin		Function Mode
RAS	LCAS	UCAS	WE	OE	DQ1 - DQ8	DQ9 - DQ16	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	H	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	D <sub>OUT</sub>	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	D <sub>OUT</sub>	Upper Byte Read
L	L	L	H	L	D <sub>OUT</sub>	D <sub>OUT</sub>	Word Read
L	L	H	L	H	D <sub>IN</sub>	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D <sub>IN</sub>	Upper Byte Write
L	L	L	L	H	D <sub>IN</sub>	D <sub>IN</sub>	Word Write
L	L	L	H	H	High-Z	High-Z	—

\*: "H" or "L"

**ELECTRICAL CHARACTERISTICS****Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V <sub>SS</sub>	V <sub>T</sub>	-0.5 to 4.6	V
Short Circuit Output Current	I <sub>OS</sub>	50	mA
Power Dissipation	P <sub>D</sub> *	1	W
Operating Temperature	T <sub>opr</sub>	0 to 70	°C
Storage Temperature	T <sub>stg</sub>	-55 to 150	°C

\*: T<sub>a</sub> = 25°C**Recommended Operating Conditions**(T<sub>a</sub> = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V <sub>CC</sub>	3.0	3.3	3.6	V
	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.0	—	V <sub>CC</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.3	—	0.8	V

**Capacitance**(V<sub>CC</sub> = 3.3 V ± 0.3 V, T<sub>a</sub> = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A7, A8R - A11R)	C <sub>IN1</sub>	—	5	pF
Input Capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{LCAS}}$ , $\overline{\text{UCAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$ )	C <sub>IN2</sub>	—	7	pF
Output Capacitance (DQ1 - DQ16)	C <sub>I/O</sub>	—	7	pF

DC Characteristics

(V<sub>CC</sub> = 3.3 V ±0.3 V, T<sub>a</sub> = 0°C to 70°C)

Parameter	Symbol	Condition	MSM51V16165B/BSL-50		MSM51V16165B/BSL-60		MSM51V16165B/BSL-70		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
			Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -2.0 mA	2.4	V <sub>CC</sub>	2.4		
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.0 mA	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I <sub>LI</sub>	0 V ≤ V <sub>I</sub> ≤ V <sub>CC</sub> + 0.3 V; All other pins not under test = 0 V	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I <sub>LO</sub>	DQ disable 0 V ≤ V <sub>O</sub> ≤ V <sub>CC</sub>	-10	10	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I <sub>CC1</sub>	$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ cycling, t <sub>RC</sub> = Min.	—	110	—	90	—	80	mA	1, 2
Power Supply Current (Standby)	I <sub>CC2</sub>	$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ = V <sub>IH</sub>	—	2	—	2	—	2	mA	1
		$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ ≥ V <sub>CC</sub> - 0.2 V	—	0.5	—	0.5	—	0.5	μA	1, 5
			—	200	—	200	—	200	μA	
Average Power Supply Current ( $\overline{\text{RAS}}$ -only Refresh)	I <sub>CC3</sub>	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ = V <sub>IH</sub> , t <sub>RC</sub> = Min.	—	110	—	90	—	80	mA	1, 2
Power Supply Current (Standby)	I <sub>CC5</sub>	$\overline{\text{RAS}}$ = V <sub>IH</sub> , $\overline{\text{CAS}}$ = V <sub>IL</sub> , DQ = enable	—	5	—	5	—	5	mA	1
Average Power Supply Current ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	I <sub>CC6</sub>	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	—	110	—	90	—	80	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I <sub>CC7</sub>	$\overline{\text{RAS}}$ = V <sub>IL</sub> , $\overline{\text{CAS}}$ cycling, t <sub>HPC</sub> = Min.	—	160	—	130	—	110	mA	1, 3
Average Power Supply Current (Battery Backup)	I <sub>CC10</sub>	t <sub>RC</sub> = 31.3 μs, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ , t <sub>RAS</sub> ≤ 1 μs	—	400	—	400	—	400	μA	1, 4, 5
Average Power Supply Current ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	I <sub>CC8</sub>	$\overline{\text{RAS}}$ ≤ 0.2 V, $\overline{\text{CAS}}$ ≤ 0.2 V	—	300	—	300	—	300	μA	1, 5

- Notes :
1. I<sub>CC</sub> Max. is specified as I<sub>CC</sub> for output open condition.
  2. The address can be changed once or less while  $\overline{\text{RAS}}$  = V<sub>IL</sub>.
  3. The address can be changed once or less while  $\overline{\text{CAS}}$  = V<sub>IH</sub>.
  4. V<sub>CC</sub> - 0.2 V ≤ V<sub>IH</sub> ≤ V<sub>CC</sub> + 0.3 V, -0.3 V ≤ V<sub>IL</sub> ≤ 0.2 V.
  5. SL version.

## AC Characteristics (1/2)

(V<sub>CC</sub> = 3.3 V ±0.3 V, T<sub>a</sub> = 0°C to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM51V16165 B/BSL-50		MSM51V16165 B/BSL-60		MSM51V16165 B/BSL-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t <sub>RC</sub>	84	—	104	—	124	—	ns	
Read Modify Write Cycle Time	t <sub>RWC</sub>	110	—	135	—	160	—	ns	
Fast Page Mode Cycle Time	t <sub>HPC</sub>	20	—	25	—	30	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t <sub>HPRWC</sub>	58	—	68	—	78	—	ns	
Access Time from $\overline{\text{RAS}}$	t <sub>RAC</sub>	—	50	—	60	—	70	ns	4, 5, 6
Access Time from $\overline{\text{CAS}}$	t <sub>CAC</sub>	—	13	—	15	—	20	ns	4, 5
Access Time from Column Address	t <sub>AA</sub>	—	25	—	30	—	35	ns	4, 6
Access Time from $\overline{\text{CAS}}$ Precharge	t <sub>CPA</sub>	—	30	—	35	—	40	ns	4, 13
Access Time from $\overline{\text{OE}}$	t <sub>OEA</sub>	—	13	—	15	—	20	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t <sub>CLZ</sub>	0	—	0	—	0	—	ns	4
Data Output Hold After $\overline{\text{CAS}}$ Low	t <sub>DOH</sub>	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ to Data Output Buffer Turn-off Delay Time	t <sub>CEZ</sub>	0	13	0	15	0	20	ns	7, 8
$\overline{\text{RAS}}$ to Data Output Buffer Turn-off Delay Time	t <sub>REZ</sub>	0	13	0	15	0	20	ns	7, 8
$\overline{\text{OE}}$ to Data Output Buffer Turn-off Delay Time	t <sub>OEZ</sub>	0	13	0	15	0	20	ns	7
$\overline{\text{WE}}$ to Data Output Buffer Turn-off Delay Time	t <sub>WEZ</sub>	0	13	0	15	0	20	ns	7
Transition Time	t <sub>T</sub>	1	50	1	50	1	50	ns	3
Refresh Period	t <sub>REF</sub>	—	64	—	64	—	64	ms	
Refresh Period (SL version)	t <sub>REF</sub>	—	128	—	128	—	128	ms	16
$\overline{\text{RAS}}$ Precharge Time	t <sub>RP</sub>	30	—	40	—	50	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t <sub>RAS</sub>	50	10,000	60	10,000	70	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode with EDO)	t <sub>RASP</sub>	50	100,000	60	100,000	70	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t <sub>RSH</sub>	7	—	10	—	13	—	ns	
$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	t <sub>ROH</sub>	7	—	10	—	13	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode with EDO)	t <sub>CP</sub>	7	—	10	—	10	—	ns	15
$\overline{\text{CAS}}$ Pulse Width	t <sub>CAS</sub>	7	10,000	10	10,000	13	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t <sub>CSH</sub>	35	—	40	—	45	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t <sub>CRP</sub>	5	—	5	—	5	—	ns	13
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t <sub>RHCP</sub>	30	—	35	—	40	—	ns	13
$\overline{\text{OE}}$ Hold Time from $\overline{\text{CAS}}$ (DQ Disable)	t <sub>CHO</sub>	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t <sub>RCD</sub>	11	37	14	45	14	50	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t <sub>RAD</sub>	9	25	12	30	12	35	ns	6
Row Address Set-up Time	t <sub>ASR</sub>	0	—	0	—	0	—	ns	
Row Address Hold Time	t <sub>RAH</sub>	7	—	10	—	10	—	ns	
Column Address Set-up Time	t <sub>ASC</sub>	0	—	0	—	0	—	ns	12
Column Address Hold Time	t <sub>CAH</sub>	7	—	10	—	13	—	ns	12
Column Address to $\overline{\text{RAS}}$ Lead Time	t <sub>RAL</sub>	25	—	30	—	35	—	ns	

## AC Characteristics (2/2)

(V<sub>CC</sub> = 3.3 V ±0.3 V, T<sub>a</sub> = 0°C to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM51V16165						Unit	Note
		B/BSL-50		B/BSL-60		B/BSL-70			
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Command Set-up Time	t <sub>RCS</sub>	0	—	0	—	0	—	ns	12
Read Command Hold Time	t <sub>RCH</sub>	0	—	0	—	0	—	ns	9, 12
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t <sub>RRH</sub>	0	—	0	—	0	—	ns	9
Write Command Set-up Time	t <sub>WCS</sub>	0	—	0	—	0	—	ns	10, 12
Write Command Hold Time	t <sub>WCH</sub>	7	—	10	—	13	—	ns	12
Write Command Pulse Width	t <sub>WP</sub>	7	—	10	—	10	—	ns	
$\overline{\text{WE}}$ Pulse Width (DQ Disable)	t <sub>WPE</sub>	7	—	10	—	10	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t <sub>OEH</sub>	7	—	10	—	13	—	ns	
$\overline{\text{OE}}$ Precharge Time	t <sub>OEP</sub>	7	—	10	—	10	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t <sub>OCH</sub>	7	—	10	—	10	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t <sub>RWL</sub>	7	—	10	—	13	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t <sub>CWL</sub>	7	—	10	—	13	—	ns	14
Data-in Set-up Time	t <sub>DS</sub>	0	—	0	—	0	—	ns	11, 12
Data-in Hold Time	t <sub>DH</sub>	7	—	10	—	13	—	ns	11, 12
$\overline{\text{OE}}$ to Data-in Delay Time	t <sub>OED</sub>	13	—	15	—	20	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t <sub>CWD</sub>	30	—	34	—	44	—	ns	10
Column Address to $\overline{\text{WE}}$ Delay Time	t <sub>AWD</sub>	42	—	49	—	59	—	ns	10
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t <sub>RWD</sub>	67	—	79	—	94	—	ns	10
$\overline{\text{CAS}}$ Precharge $\overline{\text{WE}}$ Delay Time	t <sub>CPWD</sub>	47	—	54	—	64	—	ns	10
$\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge	t <sub>RPC</sub>	5	—	5	—	5	—	ns	12
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	t <sub>CSR</sub>	5	—	5	—	5	—	ns	12
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	t <sub>CHR</sub>	10	—	10	—	10	—	ns	13
$\overline{\text{RAS}}$ Pulse Width ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	t <sub>RASS</sub>	100	—	100	—	100	—	μs	16
$\overline{\text{RAS}}$ Precharge Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	t <sub>RPS</sub>	90	—	110	—	130	—	ns	16
$\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	t <sub>CHS</sub>	-50	—	-50	—	-50	—	ns	16

- Notes:
1. A start-up delay of  $200\ \mu\text{s}$  is required after power-up, followed by a minimum of eight initialization cycles (RAS-only refresh or CAS before RAS refresh) before proper device operation is achieved.
  2. The AC characteristics assume  $t_T = 2\ \text{ns}$ .
  3.  $V_{IH}$  (Min.) and  $V_{IL}$  (Max.) are reference levels for measuring input timing signals. Transition times ( $t_T$ ) are measured between  $V_{IH}$  and  $V_{IL}$ .
  4. This parameter is measured with a load circuit equivalent to 1 TTL load and 100 pF. The output timing reference levels are  $V_{OH} = 2.0\ \text{V}$  and  $V_{OL} = 0.8\ \text{V}$ .
  5. Operation within the  $t_{RCD}$  (Max.) limit ensures that  $t_{RAC}$  (Max.) can be met.  $t_{RCD}$  (Max.) is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (Max.) limit, then the access time is controlled by  $t_{CAC}$ .
  6. Operation within the  $t_{RAD}$  (Max.) limit ensures that  $t_{RAC}$  (Max.) can be met.  $t_{RAD}$  (Max.) is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (Max.) limit, then the access time is controlled by  $t_{AA}$ .
  7.  $t_{CEZ}$  (Max.),  $t_{REZ}$  (Max.),  $t_{WEZ}$  (Max.) and  $t_{OEZ}$  (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
  8.  $t_{CEZ}$  and  $t_{REZ}$  must be satisfied for open circuit condition.
  9.  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
  10.  $t_{WCS}$ ,  $t_{CWD}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}$  (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If  $t_{CWD} \geq t_{CWD}$  (Min.),  $t_{RWD} \geq t_{RWD}$  (Min.),  $t_{AWD} \geq t_{AWD}$  (Min.) and  $t_{CPWD} \geq t_{CPWD}$  (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
  11. These parameters are referenced to the  $\overline{UCAS}$  and  $\overline{LCAS}$ , leading edges in an early write cycle, and to the  $\overline{WE}$  leading edge in an  $\overline{OE}$  control write cycle, or a read modify write cycle.
  12. These parameters are determined by the falling edge of either  $\overline{UCAS}$  or  $\overline{LCAS}$ , whichever is earlier.
  13. These parameters are determined by the rising edge of either  $\overline{UCAS}$  or  $\overline{LCAS}$ , whichever is later.
  14.  $t_{CWL}$  should be satisfied by both  $\overline{UCAS}$  and  $\overline{LCAS}$ .
  15.  $t_{CP}$  is determined by the time both  $\overline{UCAS}$  and  $\overline{LCAS}$  are high.
  16. Only SL version.