



Integrated Device Technology, Inc.

# CMOS ASYNCHRONOUS FIFO WITH RETRANSMIT

1K x 9, 2K x 9, 4K x 9

IDT72021  
IDT72031  
IDT72041

**NOTE:** The IDT72021/72031/72041s have been obsoleted and the last time buy will be on 4/30/98. These devices should not be used in new designs.

### FEATURES:

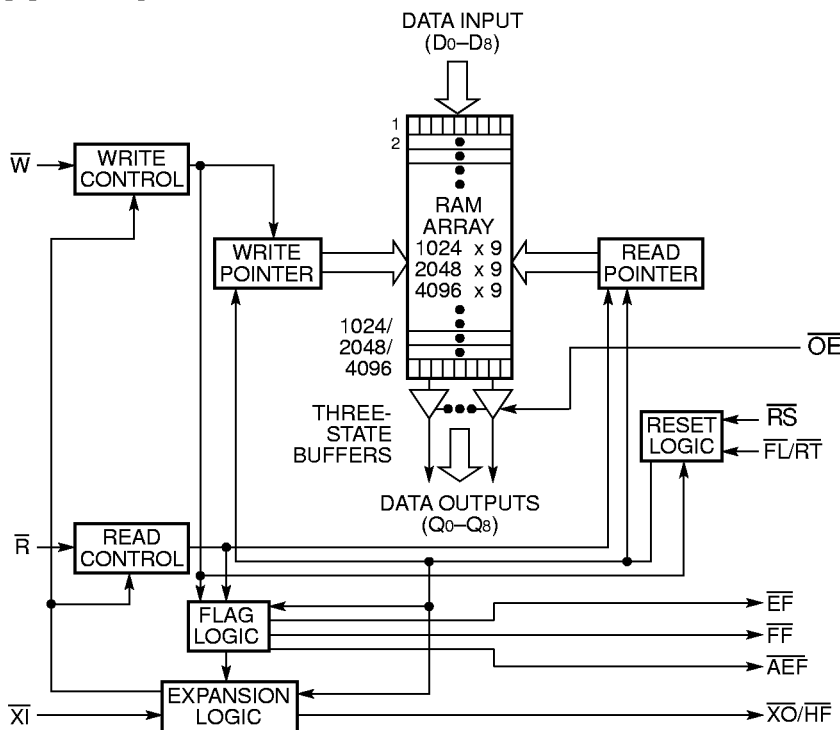
- First-In/First-Out Dual-Port memory
- Bit organization
  - IDT72021—1K x 9
  - IDT72031—2K x 9
  - IDT72041—4K x 9
- Ultra high speed
  - IDT72021—25ns access time
  - IDT72031—35ns access time
  - IDT72041—35ns access time
- Easily expandable in word depth and/or width
- Asynchronous and simultaneous read and write
- Functionally equivalent to IDT7202/03/04 with Output Enable ( $\overline{OE}$ ) and Almost Empty/Almost Full Flag ( $\overline{AEF}$ )
- Four status flags: Full, Empty, Half-Full (single device mode), and Almost Empty/Almost Full (7/8 empty or 7/8 full in single device mode)
- Output Enable controls the data output port
- Auto-retransmit capability
- Available in 32-pin DIP and PLCC
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ) is available

### DESCRIPTION:

IDT72021/031/041s are high-speed, low-power, dual-port memory devices commonly known as FIFOs (First-In/First-Out). Data can be written into and read from the memory at independent rates. The order of information stored and extracted does not change, but the rate of data entering the FIFO might be different than the rate leaving the FIFO. Unlike a Static RAM, no address information is required because the read and write pointers advance sequentially. The IDT72021/031/041s can perform asynchronous and simultaneous read and write operations. There are four status flags, ( $\overline{HF}$ ,  $\overline{FF}$ ,  $\overline{EF}$ ,  $\overline{AEF}$ ) to monitor data overflow and underflow. Output Enable ( $\overline{OE}$ ) is provided to control the flow of data through the output port. Additional key features are Write ( $\overline{W}$ ), Read ( $\overline{R}$ ), Retransmit ( $\overline{RT}$ ), First Load ( $\overline{FL}$ ), Expansion In ( $\overline{XI}$ ) and Expansion Out ( $\overline{XO}$ ). The IDT72021/031/041s are designed for those applications requiring data control flags and Output Enable ( $\overline{OE}$ ) in multiprocessing and rate buffer applications.

The IDT72021/031/041s are fabricated using IDT's CMOS technology. Military grade product is manufactured in compliance with the latest version of MIL-STD-883, Class B, for high reliability systems.

### FUNCTIONAL BLOCK DIAGRAM



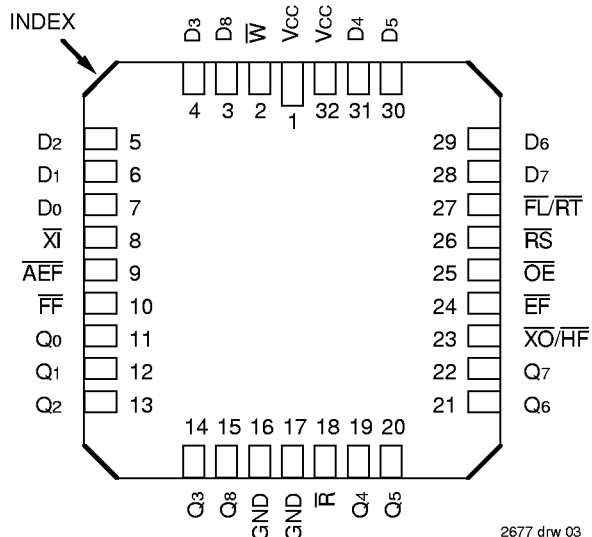
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2677 drw 01

### MILITARY AND COMMERCIAL TEMPERATURE RANGES

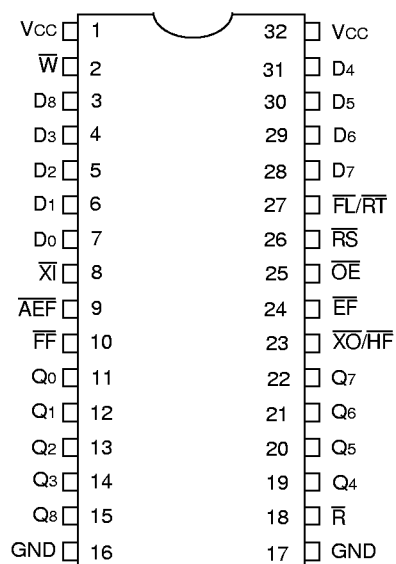
JUNE 1997

## PIN CONFIGURATIONS



2677 drw 03

PLCC (J32-1, order code: J)  
 TOP VIEW



2677 drw 02

CERDIP (D32-1, order code: D)  
 TOP VIEW

## PIN DESCRIPTIONS

Symbol	Name	I/O	Description
$\overline{D}_0$ – $\overline{D}_8$	Inputs	I	Data inputs for 9-bit wide data.
$\overline{R}S$	Reset	I	When $\overline{R}S$ is set LOW, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{H}F$ and $\overline{F}F$ go HIGH, and $\overline{A}E\overline{F}$ and $\overline{E}F$ go LOW. A reset is required before an initial WRITE after power-up. $\overline{R}$ and $\overline{W}$ must be HIGH during $\overline{R}S$ cycle.
$\overline{W}$	Write	I	When WRITE is LOW, data can be written into the RAM array sequentially, independent of READ. In order for WRITE to be active, $\overline{F}F$ must be HIGH. When the FIFO is full ( $\overline{F}F$ -LOW), the internal WRITE operation is blocked.
$\overline{R}$	Read	I	When READ is LOW, data can be read from the RAM array sequentially, independent of WRITE. In order for READ to be active, $\overline{E}F$ must be HIGH. When the FIFO is empty ( $\overline{E}F$ -LOW), the internal READ operation is blocked. The three-state output buffer is controlled by the read signal and the external output control ( $\overline{O}E$ ).
$\overline{F}L/RT$	First Load/ Retransmit	I	This is a dual-purpose input. In the single device configuration ( $\overline{X}_I$ grounded), activating retransmit ( $\overline{F}L/RT$ -LOW) will set the internal READ pointer to the first location. There is no effect on the WRITE pointer. $\overline{R}$ and $\overline{W}$ must be HIGH before setting $\overline{F}L/RT$ LOW. Retransmit is not compatible with depth expansion. In the depth expansion configuration, $\overline{F}L/RT$ -LOW indicates the first activated device.
$\overline{X}_I$	Expansion In	I	In the single device configuration, $\overline{X}_I$ is grounded. In depth expansion or daisy chain expansion, $\overline{X}_I$ is connected to $\overline{X}O$ (expansion out) of the previous device.
$\overline{O}E$	Output Enable	I	When $\overline{O}E$ is set HIGH, the data flow through the three-state output buffer is inhibited regardless of an active READ operation. A read operation does increment the read pointer in this situation. When $\overline{O}E$ is set LOW, $Q_0$ – $Q_8$ are still in a HIGH impedance condition if no READ occurs. For a complete READ operation with data appearing on $Q_0$ – $Q_8$ , both $\overline{R}$ and $\overline{O}E$ should be asserted LOW.
$\overline{F}F$	Full Flag	O	When $\overline{F}F$ goes LOW, the device is full and further WRITE operations are inhibited. When $\overline{F}F$ is HIGH, the device is not full.
$\overline{E}F$	Empty Flag	O	When $\overline{E}F$ goes LOW, the device is empty and further READ operations are inhibited. When $\overline{E}F$ is HIGH, the device is not empty.
$\overline{A}E\overline{F}$	Almost-Empty/ Almost-Full Flag	O	When $\overline{A}E\overline{F}$ is LOW, the device is empty to 1/8 full or 7/8 to completely full. When $\overline{A}E\overline{F}$ is HIGH, the device is greater than 1/8 full, but less than 7/8 full.
$\overline{X}O/H\overline{F}$	Expansion Out/ Half-Full Flag	O	This is a dual purpose output. In the single device configuration ( $\overline{X}_I$ grounded), the device is more than half full when $\overline{H}F$ is LOW. In the depth expansion configuration ( $\overline{X}O$ connected to $\overline{X}_I$ of the next device), a pulse is sent from $\overline{X}O$ to $\overline{X}_I$ when the last location in the RAM array is filled.
$Q_0$ – $Q_8$	Outputs	O	Data outputs for 9-bit wide data.

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## STATUS FLAG

Number of Words in FIFO			FF	AEF	HF	EF
1K	2K	4K				
0	0	0	H	L	H	L
1-127	1-255	1-511	H	L	H	H
128-512	256-1024	512-2048	H	H	H	H
513-896	1025-1792	2049-3584	H	H	L	H
897-1023	1793-2047	3585-4095	H	L	L	H
1024	2048	4096	L	L	L	H

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## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +155	°C
IOUT	DC Output Current	50	50	mA

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- NOTE:**
- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE (TA = +25°C, f = 1.0 MHz)

Symbol	Parameter <sup>(1)</sup>	Condition	Max.	Unit
CIN	Input Capacitance	VIN = 0V	10	pF
COU	Output Capacitance	VOUT = 0V	10	pF

**NOTE:**

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- These parameters are sampled and not 100% tested.

## RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage Commercial	2.0	—	—	V
VIH	Input High Voltage Military	2.2	—	—	V
VIL <sup>(1)</sup>	Input Low Voltage Commercial and Military	—	—	0.8	V

**NOTE:**

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- 1.5V undershoots are allowed for 10ns once per cycle.

### DC ELECTRICAL CHARACTERISTICS — IDT72021

(Commercial:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ ; Military:  $V_{CC} = 5V \pm 10\%$ ,  $T_A = -55^\circ C$  to  $+125^\circ C$ )

Symbol	Parameter	IDT72021 Commercial $t_A = 25,35ns$			IDT72021 Military $t_A = 30,40ns$			IDT72021 Commercial $t_A = 50ns$			IDT72021 Military $t_A = 50ns$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
$I_{L1}^{(1)}$	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	-1	—	1	-10	—	10	$\mu A$
$I_{L0}^{(2)}$	Output Leakage Current	-10	—	10	-10	—	10	-10	—	10	-10	—	10	$\mu A$
$V_{OH}$	Output Logic "1" Voltage $I_{OH} = -2mA$	2.4	—	—	2.4	—	—	2.4	—	—	2.4	—	—	V
$V_{OL}$	Output Logic "0" Voltage $I_{OL} = 8mA$	—	—	0.4	—	—	0.4	—	—	0.4	—	—	0.4	V
$I_{CC1}^{(3,4)}$	Active Power Supply Current	—	—	120	—	—	140	—	50	80	—	70	100	mA
$I_{CC2}^{(3)}$	Standby Current ( $\bar{R} = \bar{W} = \bar{RS} = \bar{FL}/\bar{RT} = V_{IH}$ )	—	—	12	—	—	20	—	5	8	—	8	15	mA
$I_{CC3}^{(3)}$	Power Down Current (All Input = $V_{CC} - 0.2V$ )	—	—	500	—	—	900	—	—	500	—	—	900	$\mu A$

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### DC ELECTRICAL CHARACTERISTICS — IDT72031, IDT72041

(Commercial:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ ; Military:  $V_{CC} = 5V \pm 10\%$ ,  $T_A = -55^\circ C$  to  $+125^\circ C$ )

Symbol	Parameter	IDT72031 IDT72041 Commercial $t_A = 35,50ns$			IDT72031 IDT72041 Military $t_A = 40,50ns$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
$I_{L1}^{(1)}$	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	$\mu A$
$I_{L0}^{(2)}$	Output Leakage Current	-10	—	10	-10	—	10	$\mu A$
$V_{OH}$	Output Logic "1" Voltage $I_{OUT} = -2mA$	2.4	—	—	2.4	—	—	V
$V_{OL}$	Output Logic "0" Voltage $I_{OUT} = 8mA$	—	—	0.4	—	—	0.4	V
$I_{CC1}^{(3,5)}$	Active Power Supply Current	—	75	120	—	100	150	mA
$I_{CC2}^{(3)}$	Standby Current ( $\bar{R} = \bar{W} = \bar{RS} = \bar{FL}/\bar{RT} = V_{IH}$ )	—	8	12	—	12	25	mA
$I_{CC3}^{(3)}$	Power Down Current (All Input = $V_{CC} - 0.2V$ )	—	—	2	—	—	4	mA

**NOTES:**

- Measurements with  $0.4 \leq V_{IN} \leq V_{CC}$ .
- $\bar{R} \geq V_{IH}$ ,  $0.4 \leq V_{OUT} \leq V_{CC}$ .
- $I_{CC}$  measurements are made with  $\bar{OE} = \text{HIGH}$ .
- Tested at  $f = 20MHz$ .
- Tested at  $f = 15.3 MHz$ .

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### AC ELECTRICAL CHARACTERISTICS — IDT72021<sup>(1)</sup>

(Commercial: V<sub>CC</sub> = 5.0V±10%, T<sub>A</sub> = 0°C to +70°C; Military: V<sub>CC</sub> = 5V±10%, T<sub>A</sub> = -55°C to +125°C)

Symbol	Parameter	Com'l		Mil.		Com'l		Mil.		Com'l & Mil.		Unit
		72021L25		72021L30		72021L35		72021L40		72021L50		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
fs	Shift Frequency	—	28.5	—	25	—	22.2	—	20	—	15	MHz
t <sub>RC</sub>	$\bar{R}$ Cycle Time	35	—	40	—	45	—	50	—	65	—	ns
t <sub>A</sub>	Access Time	—	25	—	30	—	35	—	40	—	50	ns
t <sub>RR</sub>	$\bar{R}$ Recovery Time	10	—	10	—	10	—	10	—	15	—	ns
t <sub>RPW</sub>	$\bar{R}$ Pulse Width <sup>(2)</sup>	25	—	30	—	35	—	40	—	50	—	ns
t <sub>RLZ</sub>	$\bar{R}$ Pulse LOW to Data Bus at Low-Z <sup>(3)</sup>	5	—	5	—	5	—	5	—	10	—	ns
t <sub>WLZ</sub>	$\bar{W}$ Pulse HIGH to Data Bus at Low-Z <sup>(3,4)</sup>	5	—	5	—	5	—	5	—	5	—	ns
t <sub>DV</sub>	Data Valid from $\bar{R}$ Pulse HIGH	5	—	5	—	5	—	5	—	5	—	ns
t <sub>RHZ</sub>	$\bar{R}$ Pulse HIGH to Data Bus at High-Z <sup>(3)</sup>	—	18	—	20	—	20	—	25	—	30	ns
t <sub>WC</sub>	$\bar{W}$ Cycle Time	35	—	40	—	45	—	50	—	65	—	ns
t <sub>WPW</sub>	$\bar{W}$ Pulse Width <sup>(2)</sup>	25	—	30	—	35	—	40	—	50	—	ns
t <sub>WR</sub>	$\bar{W}$ Recovery Time	10	—	10	—	10	—	10	—	15	—	ns
t <sub>DS</sub>	Data Set-up Time	15	—	18	—	18	—	20	—	30	—	ns
t <sub>DH</sub>	Data Hold Time	0	—	0	—	0	—	0	—	5	—	ns
t <sub>RSC</sub>	$\bar{R}\bar{S}$ Cycle Time	35	—	40	—	45	—	50	—	65	—	ns
t <sub>RS</sub>	$\bar{R}\bar{S}$ Pulse Width <sup>(2)</sup>	25	—	30	—	35	—	40	—	50	—	ns
t <sub>RSS</sub>	$\bar{R}\bar{S}$ Set-up Time	25	—	30	—	35	—	40	—	50	—	ns
t <sub>RSR</sub>	$\bar{R}\bar{S}$ Recovery Time	10	—	10	—	10	—	10	—	15	—	ns
t <sub>RTC</sub>	$\bar{R}\bar{T}$ Cycle Time	35	—	40	—	45	—	50	—	65	—	ns
t <sub>RT</sub>	$\bar{R}\bar{T}$ Pulse Width <sup>(2)</sup>	25	—	30	—	35	—	40	—	50	—	ns
t <sub>RTR</sub>	$\bar{R}\bar{T}$ Recovery Time	10	—	10	—	10	—	10	—	15	—	ns
t <sub>RSF1</sub>	$\bar{R}\bar{S}$ to $\bar{E}\bar{F}$ and $\bar{A}\bar{E}\bar{F}$ LOW	—	35	—	40	—	45	—	50	—	65	ns
t <sub>RSF2</sub>	$\bar{R}\bar{S}$ to $\bar{H}\bar{F}$ and $\bar{F}\bar{F}$ HIGH	—	35	—	40	—	45	—	50	—	65	ns
t <sub>REF</sub>	$\bar{R}$ LOW to $\bar{E}\bar{F}$ LOW	—	25	—	30	—	30	—	35	—	45	ns
t <sub>RFF</sub>	$\bar{R}$ HIGH to $\bar{F}\bar{F}$ HIGH	—	25	—	30	—	30	—	35	—	45	ns
t <sub>RPE</sub>	$\bar{R}$ Pulse Width After $\bar{E}\bar{F}$ HIGH	25	—	30	—	35	—	40	—	50	—	ns
t <sub>WEF</sub>	$\bar{W}$ HIGH to $\bar{E}\bar{F}$ HIGH	—	25	—	30	—	30	—	35	—	45	ns
t <sub>WFF</sub>	$\bar{W}$ LOW to $\bar{E}\bar{F}$ LOW	—	25	—	30	—	30	—	35	—	45	ns
t <sub>WHF</sub>	$\bar{W}$ LOW to $\bar{H}\bar{F}$ LOW	—	35	—	40	—	45	—	50	—	65	ns
t <sub>RHF</sub>	$\bar{R}$ HIGH to $\bar{H}\bar{F}$ HIGH	—	35	—	40	—	45	—	50	—	65	ns
t <sub>WPF</sub>	$\bar{W}$ Pulse Width after $\bar{F}\bar{F}$ HIGH	25	—	30	—	35	—	40	—	50	—	ns
t <sub>RF</sub>	$\bar{R}$ HIGH to Transitioning $\bar{A}\bar{E}\bar{F}$	—	35	—	40	—	45	—	50	—	65	ns
t <sub>WF</sub>	$\bar{W}$ LOW to Transitioning $\bar{A}\bar{E}\bar{F}$	—	35	—	40	—	45	—	50	—	65	ns
t <sub>OEZH</sub>	$\bar{O}\bar{E}$ HIGH to High-Z (Disable) <sup>(3)</sup>	0	12	0	15	0	17	0	20	0	25	ns
t <sub>OEZL</sub>	$\bar{O}\bar{E}$ LOW to Low-Z (Enable) <sup>(3)</sup>	0	12	0	15	0	17	0	20	0	25	ns
t <sub>AOE</sub>	$\bar{O}\bar{E}$ LOW Data Valid (Q <sub>0</sub> -Q <sub>8</sub> )	—	15	—	18	—	20	—	25	—	30	ns

**NOTES:**

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

2677 tbl 08

## AC ELECTRICAL CHARACTERISTICS — IDT72031, IDT72041<sup>(1)</sup>

(Commercial: V<sub>CC</sub> = 5.0V±10%, T<sub>A</sub> = 0°C to +70°C; Military: V<sub>CC</sub> = 5V±10%, T<sub>A</sub> = -55°C to +125°C)

Symbol	Parameter	Com'l		Mil.		Com'l and Mil.		Unit
		72031L35 72041L35		72031L40 72041L40		72031L50 72041L50		
		Min.	Max.	Min.	Max.	Min.	Max.	
f <sub>S</sub>	Shift Frequency	—	22.2	—	20	—	15	MHz
t <sub>RC</sub>	$\overline{R}$ Cycle Time	45	—	50	—	65	—	ns
t <sub>A</sub>	Access Time	—	35	—	40	—	50	ns
t <sub>RR</sub>	$\overline{R}$ Recovery Time	10	—	10	—	15	—	ns
t <sub>RPW</sub>	$\overline{R}$ Pulse Width <sup>(2)</sup>	35	—	40	—	50	—	ns
t <sub>RLZ</sub>	$\overline{R}$ Pulse LOW to Data Bus at Low-Z <sup>(3)</sup>	5	—	5	—	10	—	ns
t <sub>WLZ</sub>	$\overline{W}$ Pulse HIGH to Data Bus at Low-Z <sup>(3,4)</sup>	5	—	5	—	5	—	ns
t <sub>DV</sub>	Data Valid from $\overline{R}$ Pulse HIGH	5	—	5	—	5	—	ns
t <sub>RHZ</sub>	$\overline{R}$ Pulse HIGH to Data Bus at High-Z <sup>(3)</sup>	—	20	—	25	—	30	ns
t <sub>WC</sub>	$\overline{W}$ Cycle Time	45	—	50	—	65	—	ns
t <sub>WPW</sub>	$\overline{W}$ Pulse Width <sup>(2)</sup>	35	—	40	—	50	—	ns
t <sub>WR</sub>	$\overline{W}$ Recovery Time	10	—	10	—	15	—	ns
t <sub>DS</sub>	Data Set-up Time	18	—	20	—	30	—	ns
t <sub>DH</sub>	Data Hold Time	0	—	0	—	5	—	ns
t <sub>RSC</sub>	$\overline{RS}$ Cycle Time	45	—	50	—	65	—	ns
t <sub>RS</sub>	$\overline{RS}$ Pulse Width <sup>(2)</sup>	35	—	40	—	50	—	ns
t <sub>RSS</sub>	$\overline{RS}$ Set-up Time	35	—	40	—	50	—	ns
t <sub>RSR</sub>	$\overline{RS}$ Recovery Time	10	—	10	—	15	—	ns
t <sub>RTC</sub>	$\overline{RT}$ Cycle Time	45	—	50	—	65	—	ns
t <sub>RT</sub>	$\overline{RT}$ Pulse Width <sup>(2)</sup>	35	—	40	—	50	—	ns
t <sub>RTR</sub>	$\overline{RT}$ Recovery Time	10	—	10	—	15	—	ns
t <sub>RSF1</sub>	$\overline{RS}$ to $\overline{EF}$ and $\overline{AEF}$ LOW	—	45	—	50	—	65	ns
t <sub>RSF2</sub>	$\overline{RS}$ to $\overline{HF}$ and $\overline{FF}$ HIGH	—	45	—	50	—	65	ns
t <sub>REF</sub>	$\overline{R}$ LOW to $\overline{EF}$ LOW	—	30	—	35	—	45	ns
t <sub>RFF</sub>	$\overline{R}$ HIGH to $\overline{FF}$ HIGH	—	30	—	35	—	45	ns
t <sub>RPE</sub>	$\overline{R}$ Pulse Width After $\overline{EF}$ HIGH	35	—	40	—	50	—	ns
t <sub>WEF</sub>	$\overline{W}$ HIGH to $\overline{EF}$ HIGH	—	30	—	35	—	45	ns
t <sub>WFF</sub>	$\overline{W}$ LOW to $\overline{EF}$ LOW	—	30	—	35	—	45	ns
t <sub>WHF</sub>	$\overline{W}$ LOW to $\overline{HF}$ LOW	—	45	—	50	—	65	ns
t <sub>RHF</sub>	$\overline{R}$ HIGH to $\overline{HF}$ HIGH	—	45	—	50	—	65	ns
t <sub>WPF</sub>	$\overline{W}$ Pulse Width after $\overline{FF}$ HIGH	35	—	40	—	50	—	ns
t <sub>RF</sub>	$\overline{R}$ HIGH to Transitioning $\overline{AEF}$	—	45	—	50	—	65	ns
t <sub>WF</sub>	$\overline{W}$ LOW to Transitioning $\overline{AEF}$	—	45	—	50	—	65	ns
t <sub>OEHZ</sub>	$\overline{OE}$ HIGH to High-Z (Disable) <sup>(3)</sup>	0	17	0	20	0	25	ns
t <sub>OELZ</sub>	$\overline{OE}$ LOW to Low-Z (Enable) <sup>(3)</sup>	0	17	0	20	0	25	ns
t <sub>AOE</sub>	$\overline{OE}$ LOW Data Valid (Q <sub>0</sub> –Q <sub>8</sub> )	—	20	—	25	—	30	ns

### NOTES:

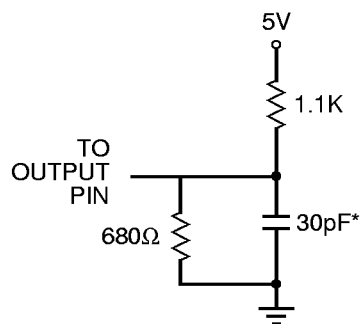
1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

2677 tbl 09

### AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2677 tbl 10

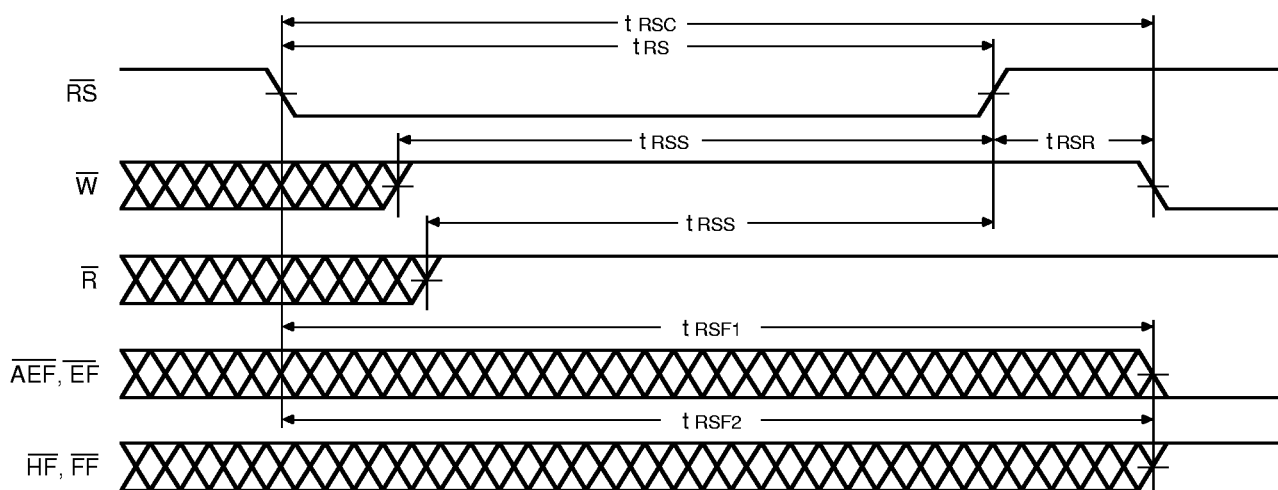


2677 drw 04

or equivalent circuit

**Figure 1. Output Load**

\* Includes scope and jig capacitances.

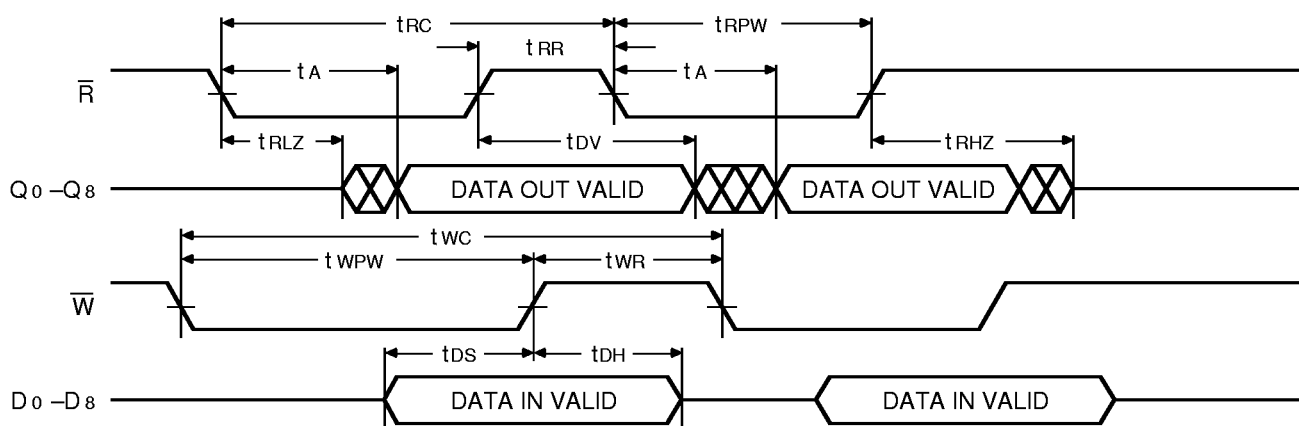


2677 drw 05

**Figure 2. Reset**

**NOTES:**

1.  $\overline{EF}$ ,  $\overline{FF}$ ,  $\overline{HF}$ , and  $\overline{AEF}$  may change status during Reset, but flags will be valid at  $t_{RSC}$ .
2.  $\overline{W}$  and  $\overline{R} = V_{IH}$  around the rising edge of  $\overline{RS}$ .

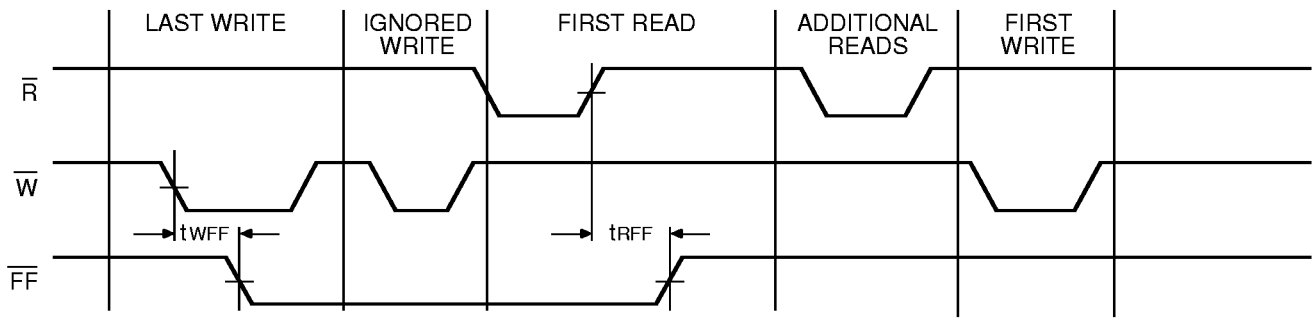


2677 drw 06

**Figure 3. Asynchronous Write and Read Operation**

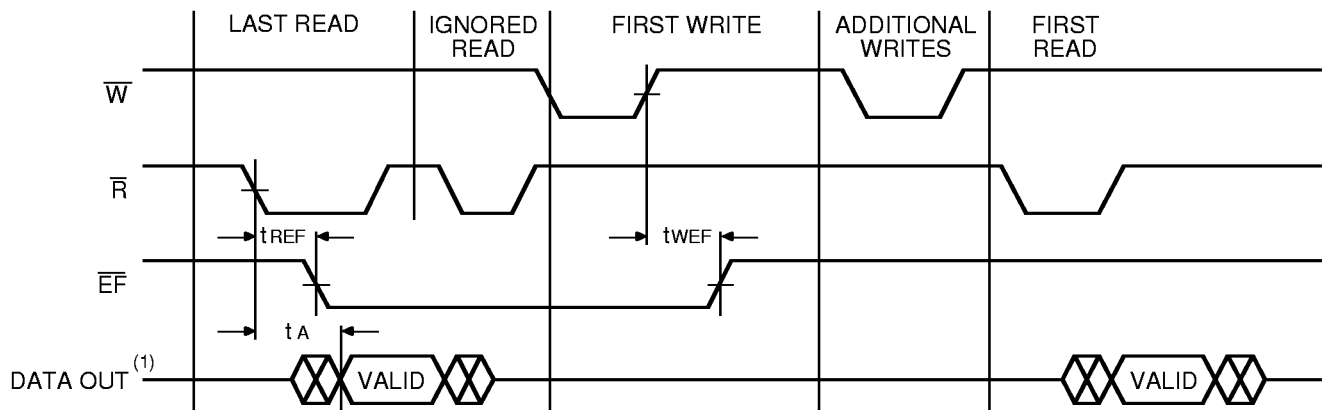
**NOTE:**

1. Assume  $\overline{OE}$  is asserted LOW.



2677 drw 07

Figure 4. Full Flag From Last Write to First Read

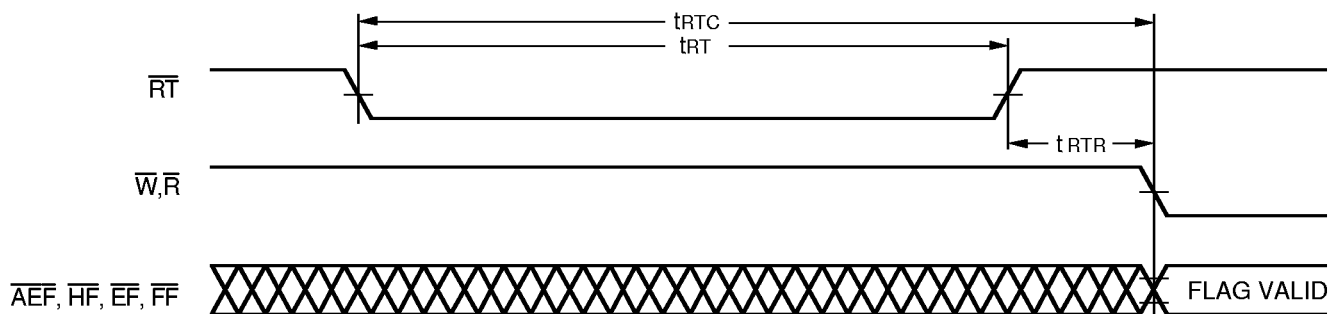


2677 drw 08

Figure 5. Empty Flag From Last Read to First Write

**NOTE:**

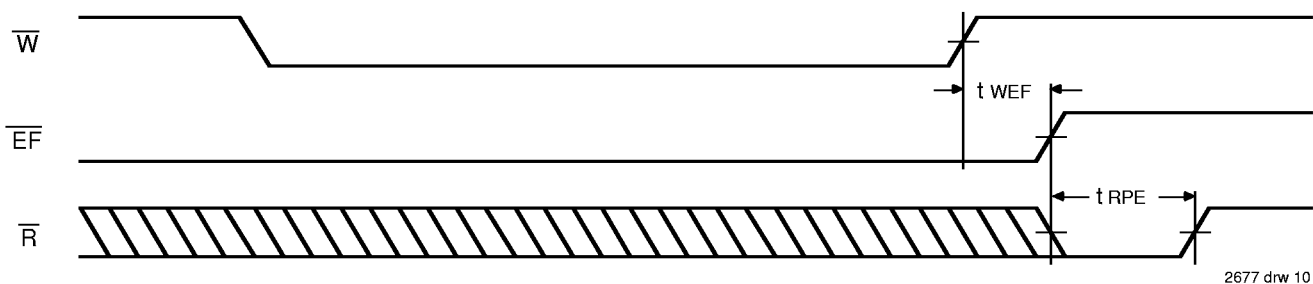
1. Assume  $\bar{OE}$  is asserted LOW.



2677 drw 09

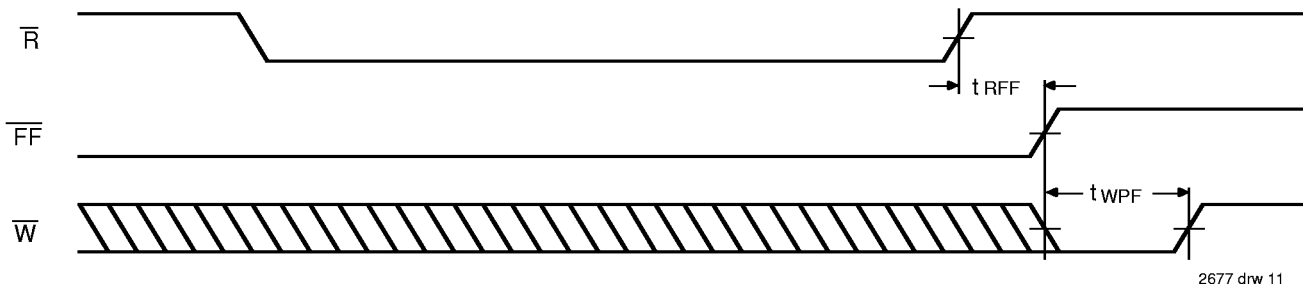
Figure 6. Retransmit





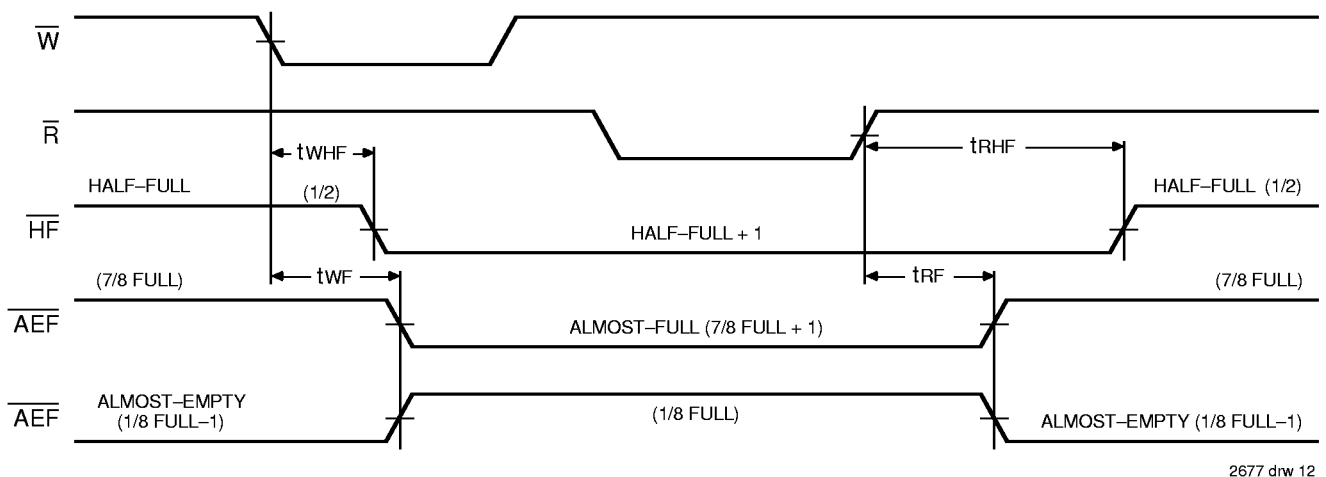
2677 drw 10

Figure 7. Empty Flag Timing  
 Figure 9. Almost-Empty/Almost-Full Flag and Half-Full Timings



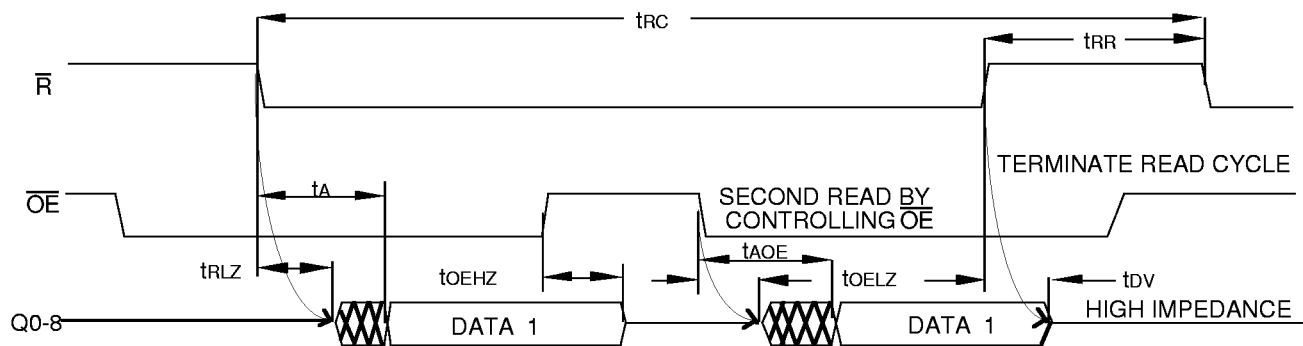
2677 drw 11

Figure 8. Full Flag Timing



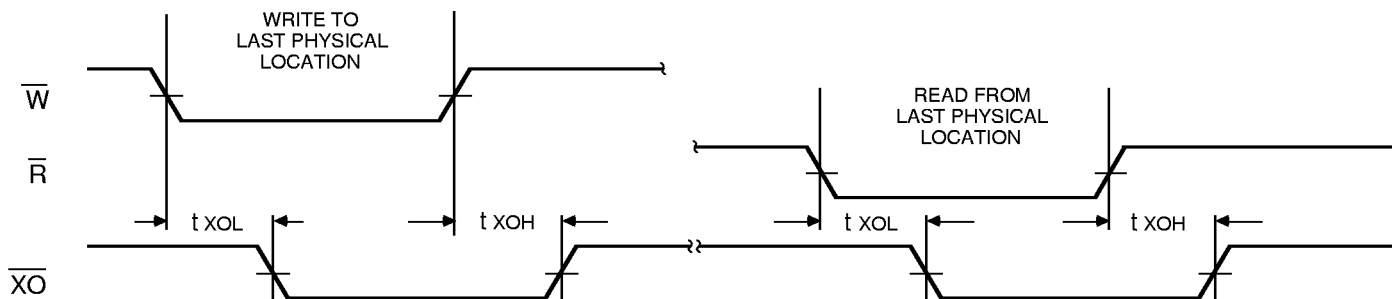
2677 drw 12

Figure 9. Almost-Empty/Almost-Full Flag and Half-Full Timings



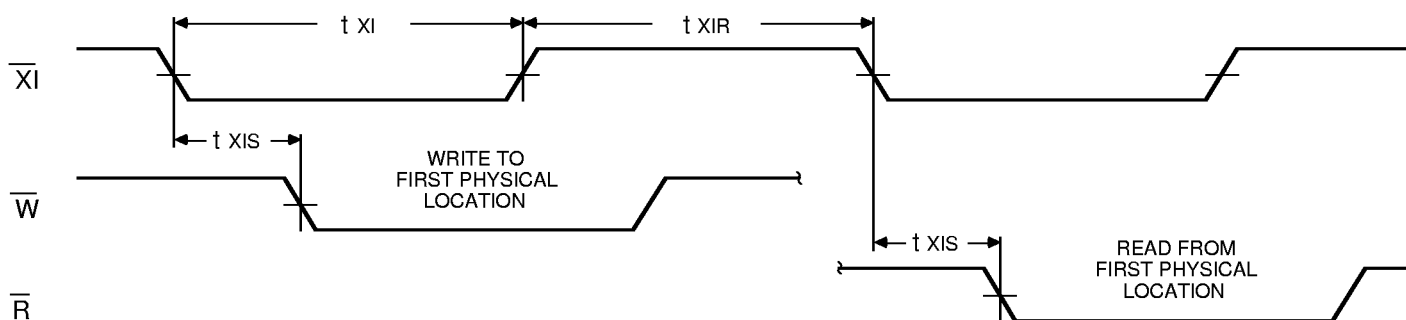
2677 drw 13

Figure 10. Output Enable and Read Operation Timings



2677 drw 14

Figure 11. Expansion Out



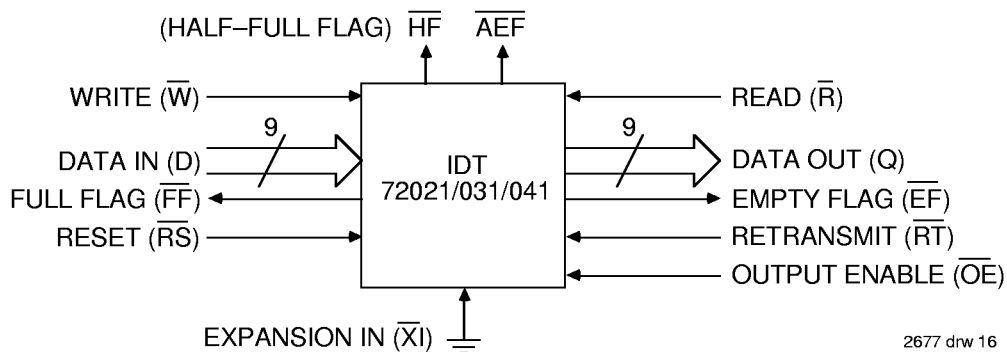
2677 drw 15

Figure 12. Expansion In

## OPERATING CONFIGURATIONS

### SINGLE DEVICE CONFIGURATION

The IDT72021/031/041 is in the Single Device Configuration when the Expansion In ( $\bar{X}I$ ) control input is grounded (see Figure 13).



2677 drw 16

Figure 13. Block Diagram of Single 1K/2K/4K x 9 FIFO

### WIDTH EXPANSION CONFIGURATION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ( $\overline{EF}$ ,  $\overline{FF}$ ,  $\overline{HF}$ , and  $\overline{AEF}$ ) can be detected from any one

device. Figure 14 demonstrates an 18-bit word width by using two IDT72021/031/041 devices. Any word width can be attained by adding additional IDT72021/031/041s.

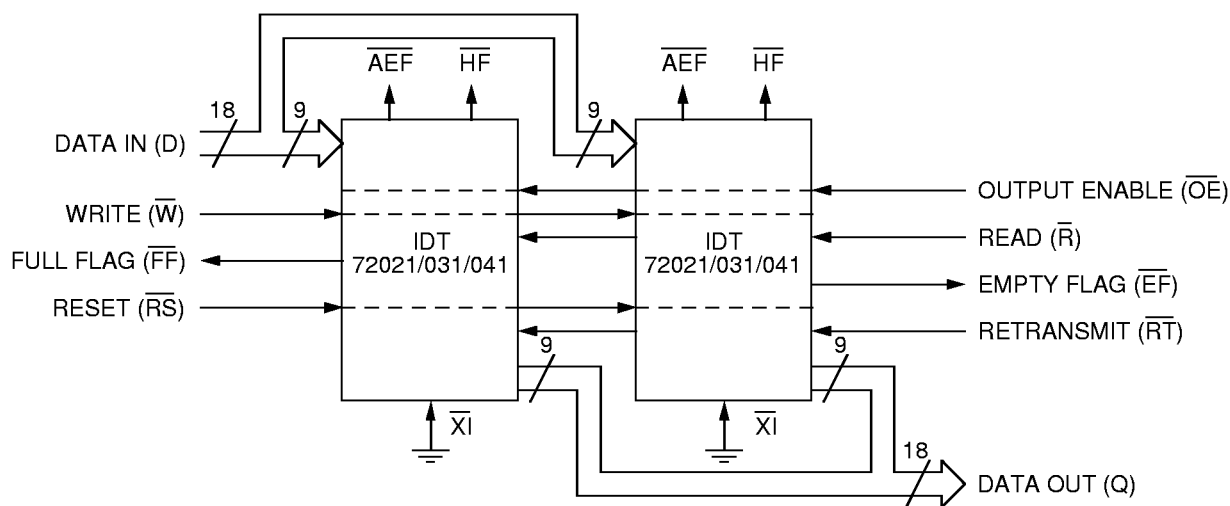


Figure 14. Block Diagram of 1K/2K/4K x 18 FIFO Memory Used in Width Expansion Configuration

#### NOTE:

1. Flag detection is accomplished by monitoring the  $\overline{FF}$ ,  $\overline{EF}$ ,  $\overline{HF}$  and  $\overline{AEF}$  signals on either (any) device used in the width expansion configuration. Do not connect any output signals together.

### DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT72021/031/041 can easily be adapted to applications when the requirements are for greater than 1K/2K/4K words. Figure 15 demonstrates Depth Expansion using three IDT72021/031/041s. Any depth can be attained by adding additional devices. The IDT72021/031/041 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the First Load ( $\overline{FL}$ ) control input.
2. All other devices must have  $\overline{FL}$  in the HIGH state.
3. The Expansion Out ( $\overline{XO}$ ) pin of each device must be tied to the Expansion In ( $\overline{XI}$ ) pin of the next device. See Figure 15.
4. External logic is needed to generate a composite Full Flag ( $\overline{FF}$ ) and Empty Flag ( $\overline{EF}$ ). This requires the ORing of all  $\overline{EF}$ s and ORing of all  $\overline{FF}$ s (i.e. all must be set to generate the correct composite  $\overline{FF}$  or  $\overline{EF}$ ). See Figure 15.
5. The Retransmit ( $\overline{RT}$ ) function and Half-Full Flag ( $\overline{HF}$ ) are not available in the Depth Expansion Mode. For additional information refer to Tech Note 9: "Cascading FIFOs or FIFO Modules".

### COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 16).

### BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT72021/031/041s as shown in Figure 17. Care must be taken to assure that the appropriate flag is monitored by each system (i.e.,  $\overline{FF}$  is monitored on the device where  $\overline{W}$  is used;  $\overline{EF}$  is monitored on the device where  $\overline{R}$  is used). Both Depth Expansion and Width Expansion may be used in this mode.

### DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted: a read flow-through and write flow-through mode. For the read flow-through mode (Figure 18), the FIFO permits the reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ( $t_{WEF} + t_A$ ) ns after the rising edge of  $\overline{W}$ , called the first write edge. It remains on the bus until the  $\overline{R}$  line is raised from LOW-to-HIGH, after which the bus would go into a three-state mode after  $t_{RHZ}$  ns. The  $\overline{EF}$  line would have a pulse showing temporary deassertion and then would be asserted. In the interval of time that  $\overline{R}$  was LOW, more words can be written to the FIFO (the subsequent writes after the first write edge will be deassert the Empty Flag); however, the same word (written on the first write edge), presented to the output bus as the read pointer, would not be incremented when  $\overline{R}$  was LOW. On toggling  $\overline{R}$ , the other words that are written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The  $\bar{R}$  line causes the  $\bar{FF}$  to be deasserted but the  $\bar{W}$  line, being LOW causes it to be asserted again in anticipation of a new data word. On the rising edge of  $\bar{W}$ , the new word is loaded in the FIFO. The  $\bar{W}$

line must be toggled when  $\bar{FF}$  is not asserted to write new data in the FIFO and to increment the write pointer.

For additional information refer to Tech Note 8: "Operating FIFOs on Full and Empty Boundary Conditions" and Tech Note 6: "Designing with FIFOs".

**TRUTH TABLES**

**TABLE I—RESET AND RETRANSMIT**

Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs			
	$\bar{RS}$	$\bar{RT}$	$\bar{XI}$	Read Pointer	Write Pointer	$\bar{EF}$	$\bar{FF}$	$\bar{HF}$	$\bar{AEF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1	0
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X	X
Read/Write	1	1	0	Increment <sup>(1)</sup>	Increment <sup>(1)</sup>	X	X	X	X

**NOTE:**

1. Pointer will increment if flag is HIGH.

2677 tbl 11

**TABLE II—RESET AND FIRST LOAD TRUTH TABLE**

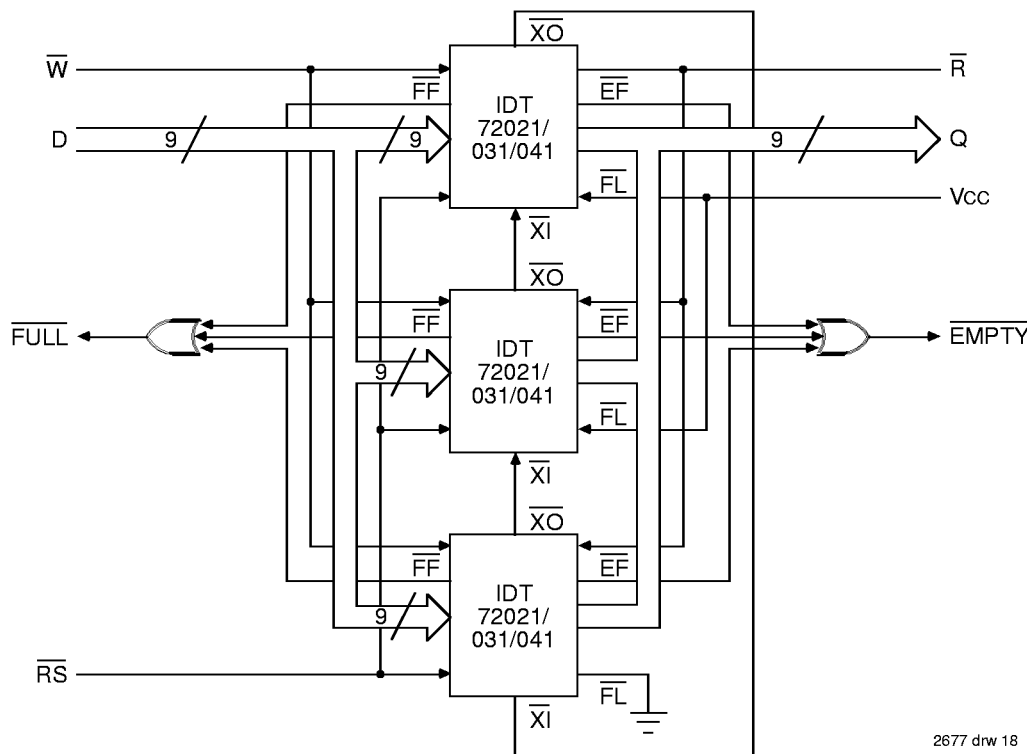
Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\bar{RS}$	$\bar{FL}$	$\bar{XI}$	Read Pointer	Write Pointer	$\bar{EF}$	$\bar{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

**NOTE:**

1.  $\bar{XI}$  is connected to  $\bar{XO}$  of previous device. See Figure 15.  $\bar{RS}$  = Reset Input  $\bar{FL}/\bar{RT}$  = First Load/Retransmit,  $\bar{EF}$  = Empty Flag Output,  $\bar{FF}$  = Flag Full Output,  $\bar{XI}$  = Expansion Input,  $\bar{HF}$  = Half-Full Flag Output,  $\bar{AEF}$  = Almost Empty/Almost Full Flag.

2677 tbl 12

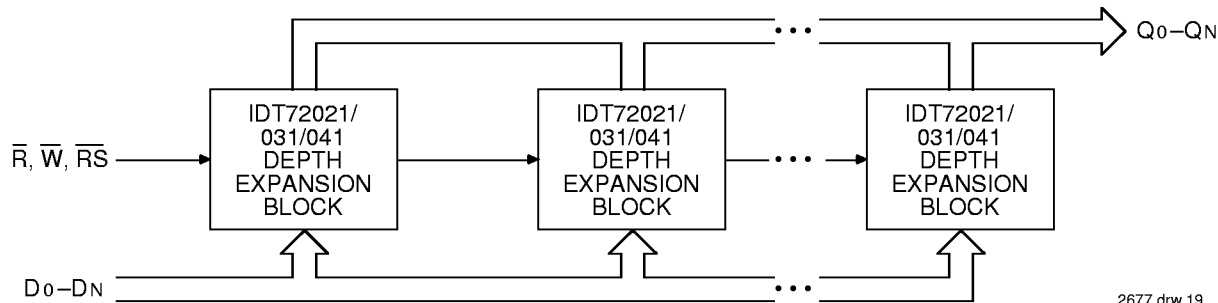


2677 drw 18

Figure 15. Block Diagram of 3K/6K/12K x 9 FIFO Memory (Depth Expansion)

**NOTE:**

1. IDT only guarantees depth expansion with identical IDT part numbers and speed.

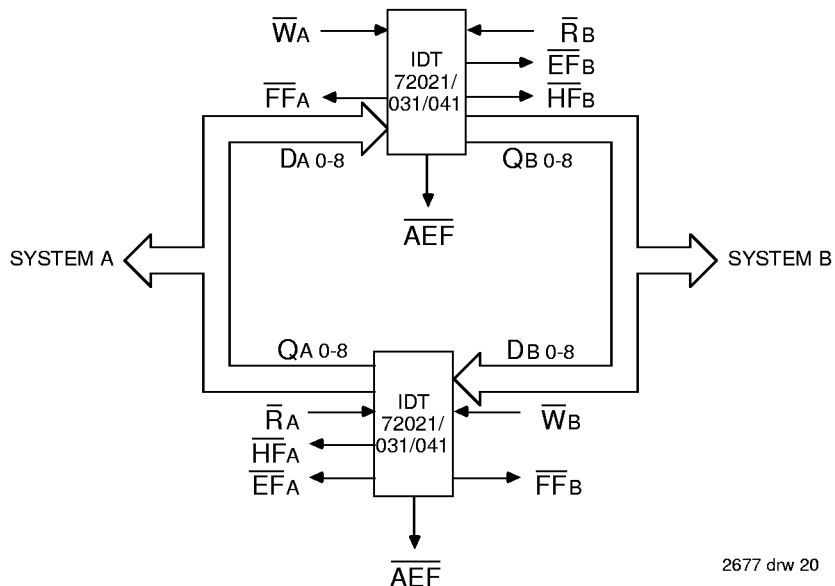


2677 drw 19

Figure 16. Compound FIFO Expansion

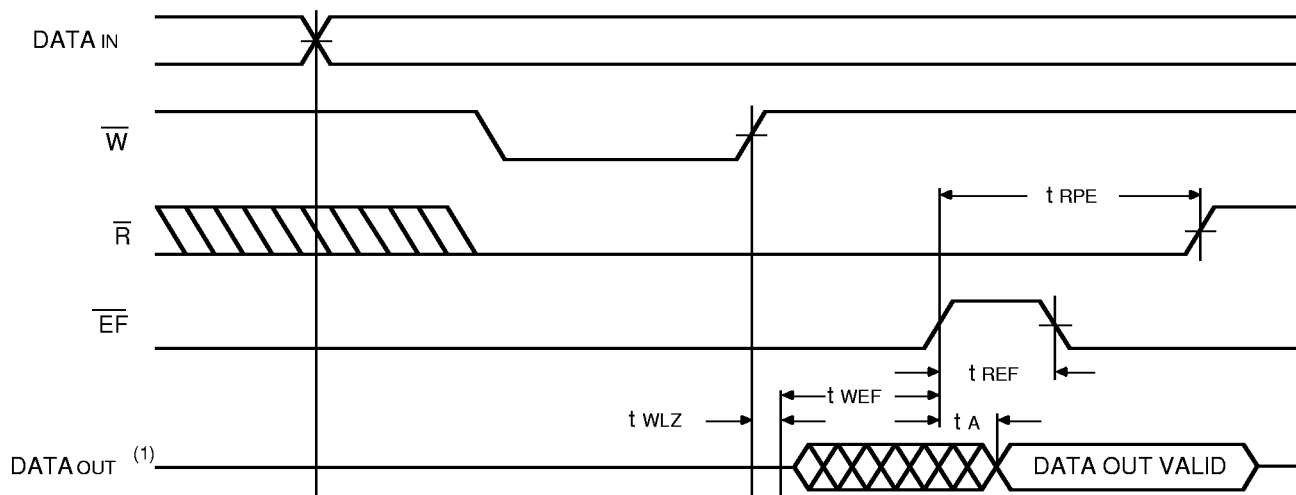
NOTES:

1. For depth expansion block see section of Depth Expansion and Figure 15.
2. For Flag detection see section on Width Expansion and Figure 14.



2677 drw 20

Figure 17. Bidirectional FIFO Mode



2677 drw 21

Figure 18. Read Data Flow-Through Mode

NOTE:

1. Assume OE-bar is asserted LOW.

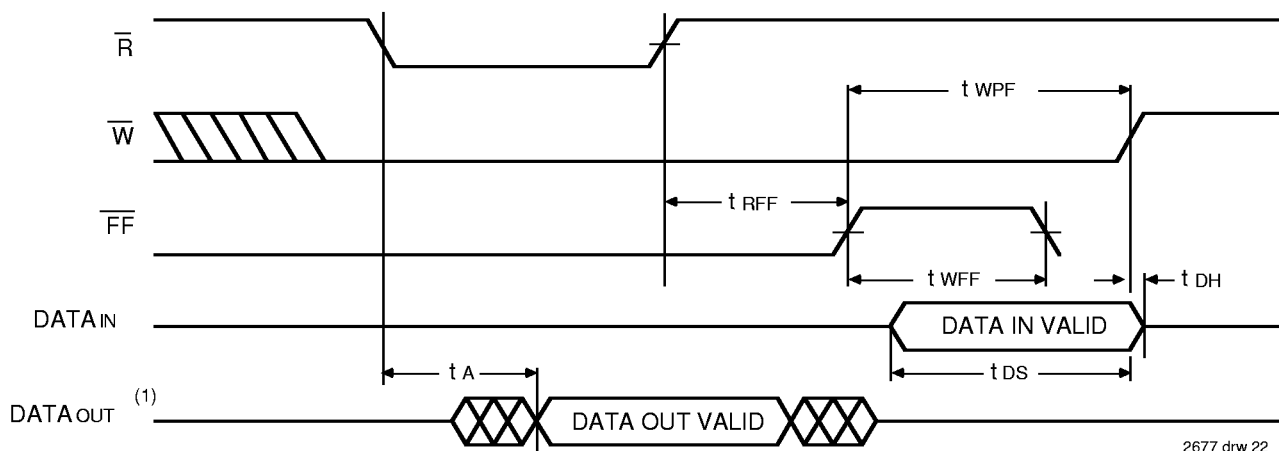


Figure 19. Write Data Flow-Through Mode

**NOTE:**

1. Assume  $\overline{OE}$  is asserted LOW.

**ORDERING INFORMATION**

IDT	XXXXX	X	X	X	X	
Device Type	Power	Speed	Package	Process/ Temperature Range		
					Blank	Commercial (0°C to +70°C)
					B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
					D	CERDIP (D32-1)
					J	Plastic Leaded Chip Carrier (PLCC, J32-1)
					25	72021—Commercial Only
					30	72021—Military Only
					35	72021/031/041—Commercial Only
					40	72021/031/041—Military Only
					50	72021/031/041—Commercial & Military
					L	Low Power
					72021	1,024 x 9-Bit FIFO
					72031	2,048 x 9-Bit FIFO
					72041	4,096 x 9-Bit FIFO

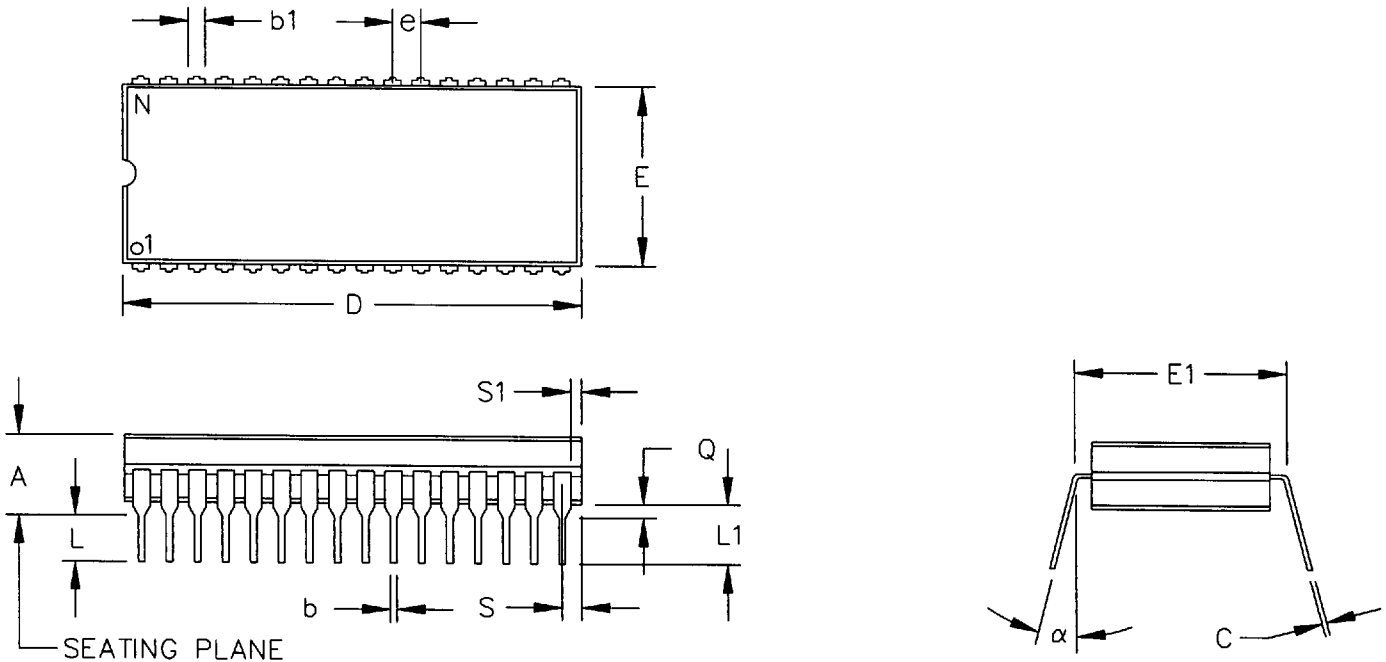
} Access Time (tA) Speed in Nanoseconds

2677 drw 23

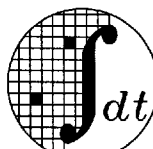
# PACKAGE DIAGRAM OUTLINES

## CERDIP (Continued)

REV	DCN	DESCRIPTION	DATE	APPROVED
01	17523	UPDATED TO STANDARDIZE DWG	6/20/90	<i>D Guilhamet</i>
02	22228	CHANGED b1 MIN DIMENSION		



- NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL DIMENSIONS ARE IN INCHES.
  2. BSC - BASIC LEAD SPACING BETWEEN CENTERS.
  3. SYMBOL "N" REPRESENTS THE NUMBER OF LEADS.

DWG #	D32-1				CONFIGURATION	EXCEPTIONS		
SYMBOL	MIN	MAX			NOT LISTED	NONE		
A	.120	.210	MIL-M-38510		NOT REGISTERED			
b	.014	.023	JEDEC					
b1	.045	.065	TOLERANCES UNLESS OTHERWISE SPECIFIED		 <b>Integrated Device Technology, Inc.</b> 3236 Scott Blvd., Santa Clara, CA 95051 (408) 727-6116 FAX: (408) 727-2328			
C	.008	.014	FRAC DEC ANGLES					
D	1.625	1.675	± - ± - ± -					
E	.570	.600	APPROVALS	DATE				
E1	.590	.620	DRAWN <i>AA</i>	03/90				
e	.100 BSC		CHECKED					
L	.125	.200						
L1	.150	-						
Q	.020	.060						
S	.030	.080						
S1	.005	-						
alpha	0°	15°						
N	32				SCALE	SIZE	DRAWING NO.	REV
				N/A	A	PSC-2054	02	
DO NOT SCALE DRAWING						SHEET	71	



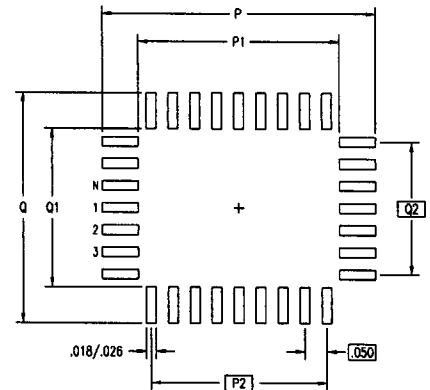


PACKAGE DIAGRAM OUTLINES  
PLCC (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27846	07	REDRAW TO JEDEC FORMAT	03/15/95	

SYMBOL	JEDEC VARIATION			NOTE
	AE			
	MIN	NOM	MAX	
A	.125	.132	.140	
A1	.075	.078	.095	
A2	.053	-	.068	
D	.485	.490	.495	
D1	.449	.451	.453	3,4
D2	.195	.205	.215	5
E	.585	.590	.595	
E1	.549	.551	.553	3,4
E2	.245	.255	.265	5
ND	7			
NE	9			
N	32			

LAND PATTERN DIMENSIONS



	MIN	MAX
P	.620	.628
P1	.454	.462
P2	.400 BSC	
Q	.520	.562
Q1	.354	.362
Q2	.300 BSC	
N	32	

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]
- DIMENSIONS D1 AND E1 ARE TO BE DETERMINED AT DATUM PLANE [-H-]
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .010 PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
- DIMENSIONS D2 AND E2 ARE TO BE DETERMINED AT SEATING PLANE [-C-] CONTACT POINT
- DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .007 TOTAL MAXIMUM PER LEAD
- EXACT SHAPE OF EACH CORNER IS OPTIONAL
- THESE DIMENSIONS DETERMINE THE MAXIMUM ANGLE OF THE LEAD FOR SOCKET APPLICATIONS
- ALL DIMENSIONS ARE IN INCHES
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-016, VARIATION AE

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc.	
DECIMAL	ANGULAR	2975 Slender Way, Santa Clara, CA 95054	
XX±	±	PHONE: (408) 727-8118	
XXXX±		FAX: (408) 492-8674 TWC: 910-338-2070	
XXXX±			
APPROVALS	DATE	TITLE PL PACKAGE OUTLINE	
DRAWN <i>Ad</i>	08/15/90	RECTANGULAR PLCC	
CHECKED		.050 PITCH	
		SIZE C	DRAWING No. PSC-4013
			REV 07
DO NOT SCALE DRAWING			

4825771 0021956 945

87