DESCRIPTION

The HY62U8400A/HY62U8400A-I is a high-speed, low power and 4M bits CMOS SRAM organized as 524,288 words by 8 bits. The HY62U8400A/HY62U8400A-I uses Hyundai's high performance twin tub CMOS process technology and was designed for high-speed and low power circuit technology. It is particulary well suited for used in high-density and low power system applications. This device has a data retention mode that guarantees data to remain valid at the minimum power supply voltage of 2.0V.

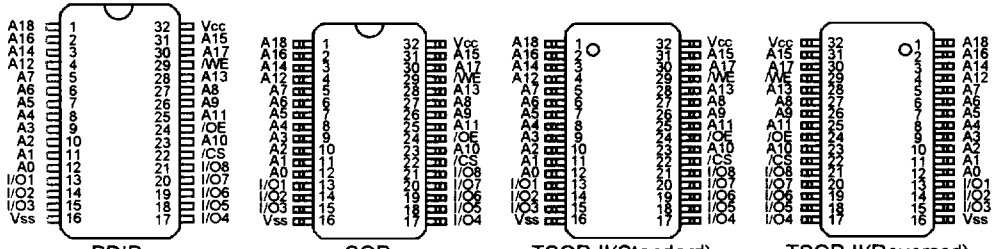
FEATURES

- Fully static operation and Tri-state outputs
- TTL compatible inputs and outputs
- Low power consumption
- Battery backup
  - 2.0V(min) data retention
- Standard pin configuration
  - 32pin 600mil PDIP
  - 32pin 525mil SOP
  - 32pin 400mil TSOP-II (Standard and Reversed)

Product No.	Voltage (V)	Speed (ns)	Operation Current(mA)	Standby Current(uA)	Temperature (℃)
HY62U8400A	3.0	55/70/85	5	50	0~70(Normal)
HY62U8400A-I	3.0	55/70/85	5	50	-40~85(E.T.)

Note 1. E.T. : Extended Temperature, Normal : Normal Temperature
2. Current value is max.

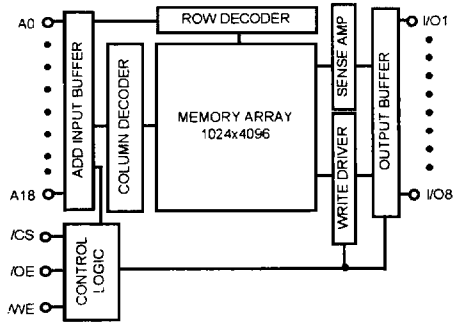
PIN CONNECTION



PIN DESCRIPTION

Pin Name	Pin Function
/CS	Chip Select
/WE	Write Enable
/OE	Output Enable
A0 ~ A18	Address Input
I/O1 ~ I/O16	Data Input/Output
Vcc	Power(3.0V)
Vss	Ground

BLOCK DIAGRAM



Low Power Dissipation SRAM(3.3V/3.0V)

ORDERING INFORMATION

Part No.	Speed	Temp.	Package
HY62U8400P	55/70/85		PDIP
HY62U8400G	55/70/85		SOP
HY62U8400T2	55/70/85		TSOP-II(Standard)
HY62U8400R2	55/70/85		TSOP-II(Reversed)
HY62U8400P-I	55/70/85	E.T.	PDIP
HY62U8400G-I	55/70/85	E.T.	SOP
HY62U8400T2-I	55/70/85	E.T.	TSOP-II(Standard)
HY62U8400R2-I	55/70/85	E.T.	TSOP-II(Reversed)

ABSOLUTE MAXIMUM RATING (1)

Symbol	Parameter	Rating	Unit	Remark
V_{CC}, V_{IN}, V_{OUT}	Power Supply, Input/Output Voltage	-0.3 to 4.6	V	
T_A	Operating Temperature	0 to 70	℃	HY62U8400
		-40 to 85	℃	HY62U8400-I
T_{STG}	Storage Temperature	-65 to 150	℃	
P_D	Power Dissipation	1.0	W	
I_{OUT}	Data Output Current	50	mA	
T_{SOLDER}	Lead Soldering Temperature & Time	260•10	℃• sec	

Note

1 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliablity.

RECOMMENDED DC OPERATING CONDITION

TA=0℃ to 70℃/-40℃ to 85℃

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	2.7	3.0	3.3	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	Vcc+0.3	V
V_{IL}	Input Low Voltage	-0.3(1)	-	0.4	V

Note :

1. V_{IL} = -3.0V for pulse width less than 30ns

TRUTH TABLE

/CS1	/WE	/OE	MODE	I/O OPERATION
H	X	X	Standby	High-Z
L	H	H	Output Disabled	High-Z
L	H	L	Read	Data Out
L	L	X	Write	Data In

Note :

1. H=V_{IH}, L=V_{IL}, X=don't care

DC ELECTRICAL CHARACTERISTICS

Vcc = 3.0V±10%, TA = 0℃ to 70℃/-40℃ to 85℃ unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ILI	Input Leakage Current	Vss ≤ VIN ≤ Vcc	-1	-	1	uA
ILO	Output Leakage Current	Vss ≤ VOUT ≤ Vcc, /CS = VIH or /OE = VIH or /WE = VIL	-1	-	1	uA
Icc	Operating Power Supply Current	/CS = VIL, VIN = VIH or VIL, II/O = 0mA	-	-	5	mA
ICC1	Average Operating Current	/CS = VIL Min Duty Cycle = 100%, II/O = 0mA	-	-	50	mA
ISB	TTL Standby Current (TTL Input)	/CS = VIH	-	-	0.5	mA
ISB1	CMOS Standby Current (CMOS Input)	/CS ≥ Vcc - 0.2V		-	50	uA
VOL	Output Low Voltage	IOL = 2.1mA	-	-	0.4	V
VOH	Output High Voltage	IOH = -1mA	2.2	-	-	V

Note : Typical values are at Vcc = 3.0V, TA = 25℃

AC CHARACTERISTICS

Vcc = 3.0V±10%, TA = 0℃ to 70℃/-40℃ to 85℃ unless otherwise specified

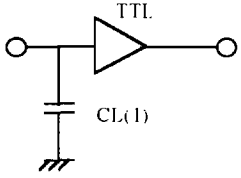
#	Symbol	Parameter	-55		-70		-85		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
	READ CYCLE								
1	tRC	Read Cycle Time	55	-	70	-	85	-	ns
2	tAA	Address Access Time	-	55	-	70	-	85	ns
3	tACS	Chip Select Access Time	-	55	-	70	-	85	ns
4	tOE	Output Enable to Output Valid	-	25	-	35	-	45	ns
5	tCLZ	Chip Select to Output in Low Z	10	-	10	-	10	-	ns
6	tOLZ	Output Enable to Output in Low Z	10	-	10	-	10	-	ns
7	tCHZ	Chip Deselection to Output in High Z	0	20	0	25	0	30	ns
8	tOHZ	Out Disable to Output in High Z	0	20	0	25	0	30	ns
9	tOH	Output Hold from Address Change	10	-	15	-	20	-	ns
	WRITE CYCLE								
10	tWC	Write Cycle Time	55	-	70	-	85	-	ns
11	tCW	Chip Selection to End of Write	45	-	60	-	70	-	ns
12	tAW	Address Valid to End of Write	45	-	60	-	70	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width	40	-	50	-	55	-	ns
15	tWR	Write Recovery Time	0	-	0	-	0	-	ns
16	tWHZ	Write to Output in High Z	0	20	0	25	0	30	ns
17	tDW	Data to Write Time Overlap	25	-	30	-	35	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
19	tOW	Output Active from End of Write	5	-	5	-	10	-	ns

AC TEST CONDITIONS

T_A = 0℃ to 70℃/-40℃ to 85℃ unless otherwise specified

PARAMETER	Value
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V
Output Load	CL = 100pF + 1TTL Load

AC TEST LOADS



Note : Including jig and scope capacitance

CAPACITANCE

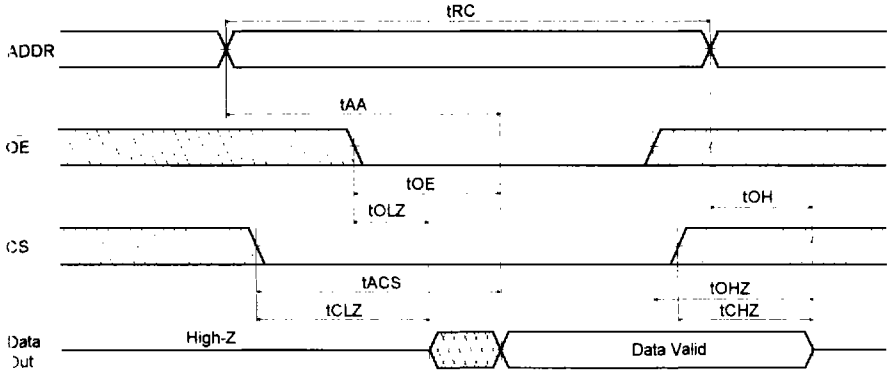
T_A = 25℃, f= 1.0Mhz

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	8	pF

Note : This parameter is sampled and not 100% tested

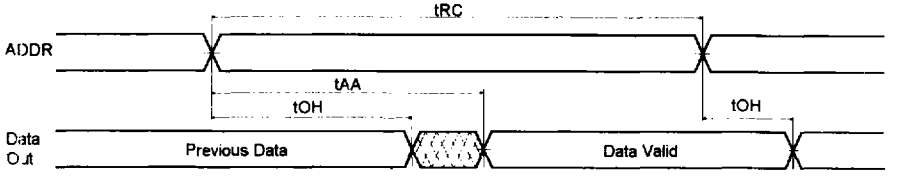
TIMING DIAGRAM

READ CYCLE 1



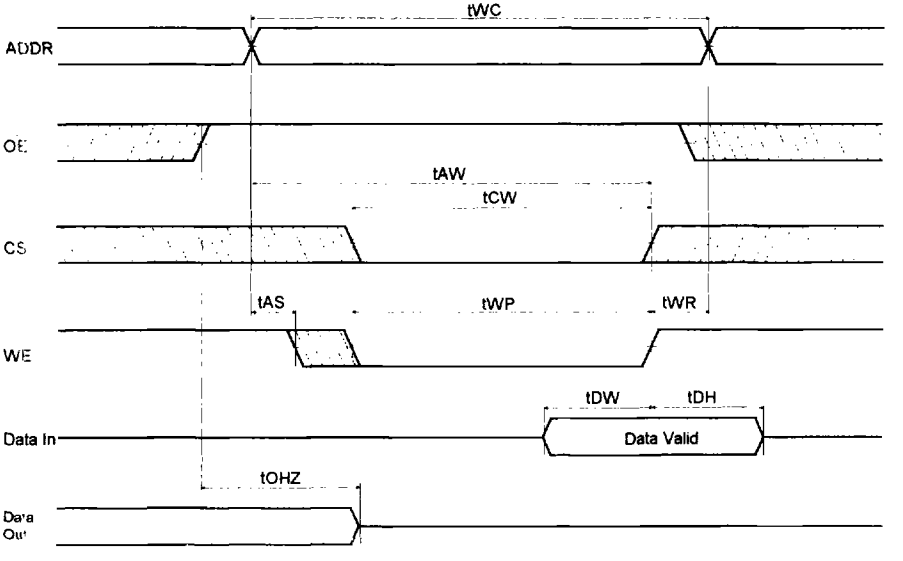
Note(READ CYCLE):
1. tCHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels
2. At any given temperature and voltage condition, tCHZ max. is less than tCLZ min. both for a given device and from device to device.
3. /WE is high for the read cycle.

READ CYCLE 2

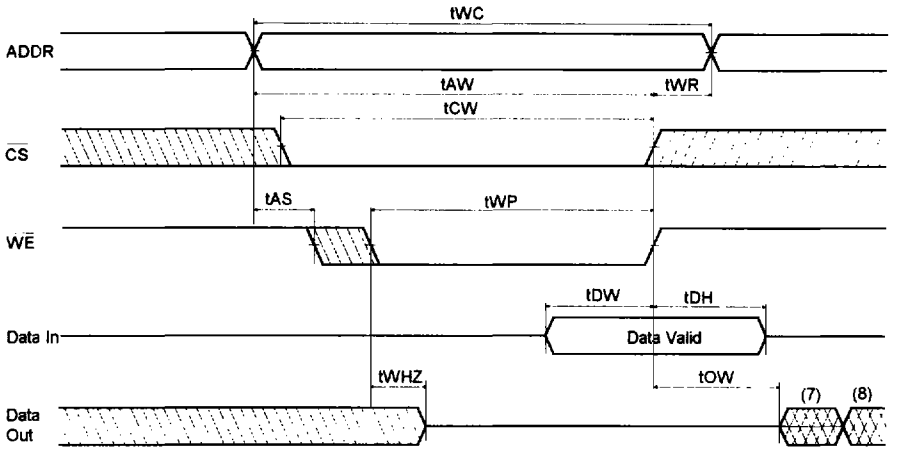


Note(READ CYCLE):
1. /WE is high for the read cycle.
2. Device is continuously selected /CS = V_{IL}
3. /OE =V_{IL}.

WRITE CYCLE 1(/OE Clocked)



WRITE CYCLE 2 (/OE Low Fixed)



Notes(WRITE CYCLE):

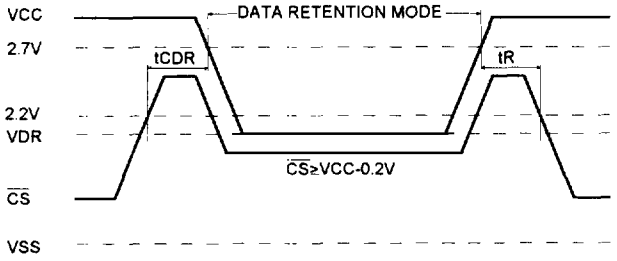
1. A write occurs during the overlap of a low /CS1, CS2 and low /WE. A write begins at the latest transition among /CS1 going now, CS2 going high and /WE going low: A write ends at the earliest transition among /CS1 going high, CS2 low and /WE going high. tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS1 going low or CS2 going high to the end of write
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tRW is applied in case a write ends as /CS1, or /WE going high, and tWR2 applied in case a write ends at CS2 going low.
5. If /OE, CS2 and /WE are in the read mode during this period, and the I/O pins are in the output low-Z state, input of opposite phase of the output must not be applied because bus contention can occur.
6. If /CS1 goes low simultaneously with /WE going low, the outputs remain in high impedance state.
7. Dout is the same phase of lasted written data in this write cycle.
8. Dout is the read data of the new address.

DATA RETENTION ELECTRIC CHARATERISTIC

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DR}	Vcc for Data Retention	/CS ≥ Vcc - 0.2V Vss ≤ V_{IN} ≤ Vcc	2.0	-	-	V
I_{CCDR}	Data Retention Current	Vcc = 0.3V, /CS ≥ Vcc -0.2V, Vss ≤ V_{IN} ≤ Vcc		-	20	uA
tCDR	Chip Disable to Data Retention Time	See Data Retention Timing Diagram	0	-	-	ns
tR	Operating Recovery Time		tRC(2)	-	-	ns

Notes:
1. Typical values are at the comdition of T_A = 25℃.
2. tRC is read cycle time.

DATA RETENTION TIMING DIAGRAM

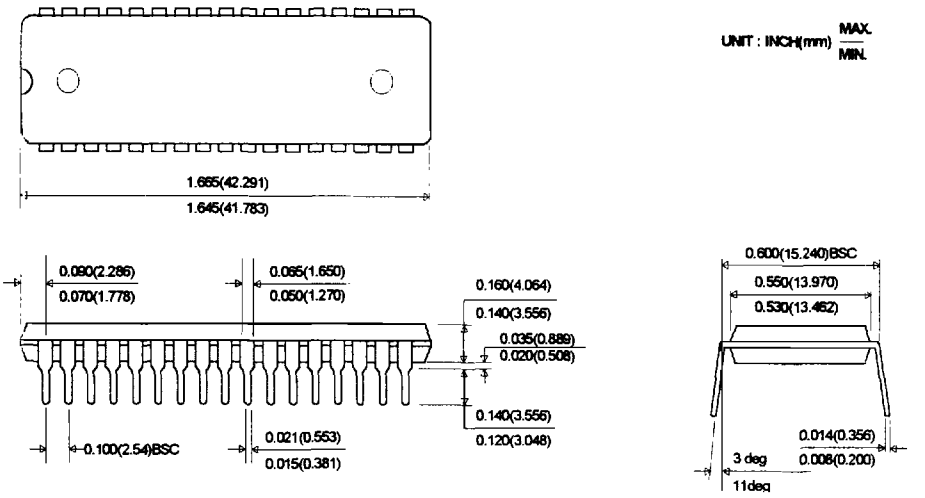


RELIABILITY SPEC.

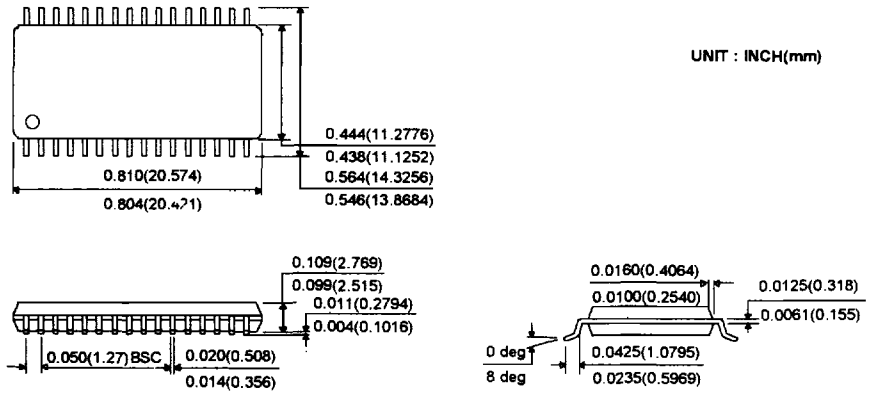
TEST MODE		TEST SPEC.
ESD	HBM	≥ 2000V
	MM	≥ 250V
LATCH - UP		≤ -100mA
		≥ 100mA

PACKAGE INFORMATION

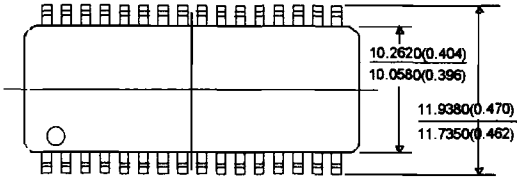
32pin 600mil Plastic Dual In Line Package(P)



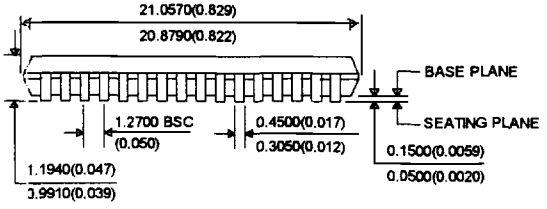
32pin 525mil Small Outline Package(G)

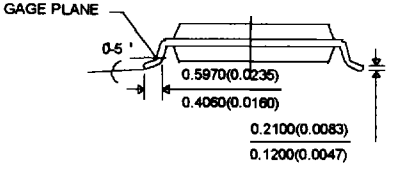


32pin 400mil Thin Small Outline Package Standard(T2)

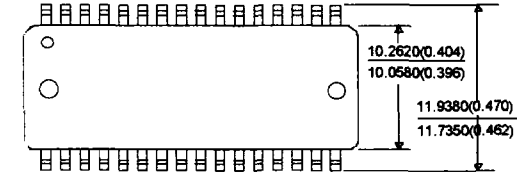


UNIT : INCH(mm) MAX. / MIN.





32pin 400mil Thin Small Outline Package Reversed(R2)



UNIT : INCH(mm) MAX. / MIN.