Quad Three-State Bus Transceiver With Interface Logic
2917

PRELIMINARY DATA

Features/Benefits
- **Quad high-speed LSI bus-transceiver**
- **Three-state bus driver**
- **D-type register on driver**
- **Bus driver output can sink 40mA at 0.5V max**
- **Internal odd 4-bit parity checker/generator**
- **Receiver has output latch for pipeline operation**
- **Three-state receiver outputs sink 12mA**
- **Advanced low-power Schottky processing**
- **100% reliability assurance testing in compliance with MIL-STD-883**
- **3.5V minimum output high voltage for direct interface to MOS microprocessors**

PART NUMBER	PACKAGE	TEMPERATURE RANGE
2917NC	N20	0°C to +70°C
2917JC	J20	0°C to +70°C
2917JM	J20	−55°C to +125°C
2917FM*	F20	−55°C to +125°C

*Available on special order

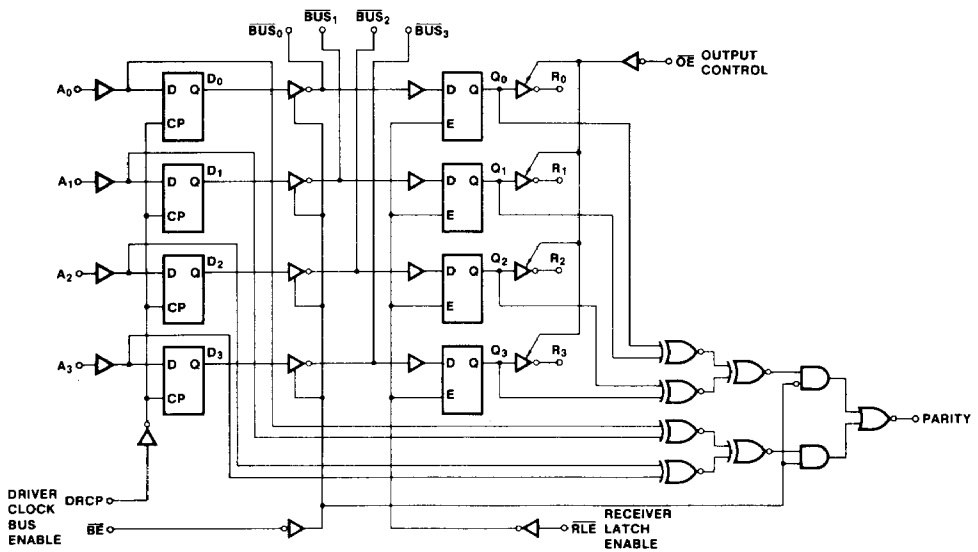
Description
The 2917 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches, that feature three-state outputs. The device also contains a four-bit odd parity checker/generator.

The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 40mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled.

The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_i data into this drive register on the LOW-to-HIGH transition.

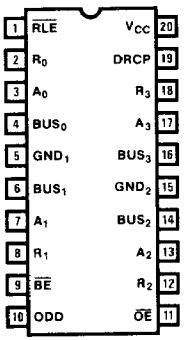
Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present

Logic Diagram

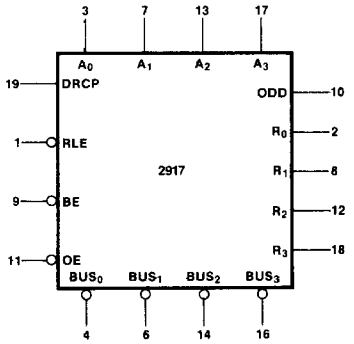


data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.
The 2917 features a built in 4-bit odd parity checker/generator. The bus enable input (BE) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

Pin Configuration



Logic Symbol



V_{CC} = Pin 20
GND_1 = Pin 5
GND_2 = Pin 15

Absolute Maximum Ratings

Storage temperature ..... −65°C to +150°C
Temperature (ambient) under bias ..... −55°C to +125°C
Supply voltage to ground potential ..... −0.5V to +7V
DC voltage applied to outputs for HIGH output state ..... −0.5V to +V_{CC} max.
DC input voltage ..... −0.5V to +5.5V
DC output current, into outputs (except bus) 30mA
DC output current, into bus 100mA
DC input current ..... −30mA to +5.0mA

Bus Input/Output Characteristics

Over Operating Temperature Range

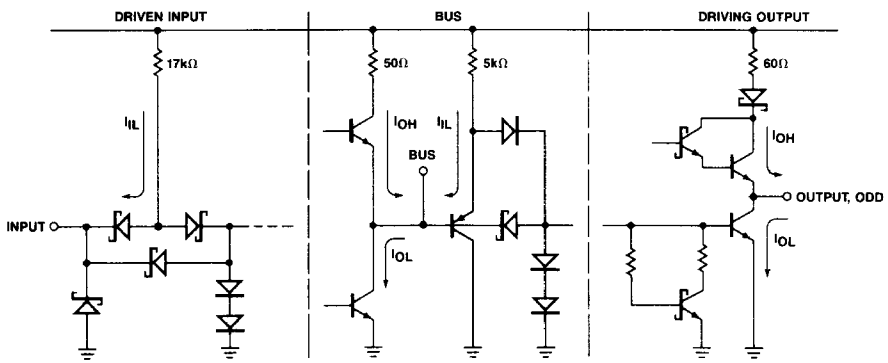
SYMBOL	PARAMETER	TEST CONDITIONS[1]		MILITARY T_A = −55°C to +125°C, V_{CC} MIN = 4.50V, V_{CC} MAX = 5.50V MIN	TYP	MAX	COMMERCIAL T_A = 0°C to +70°C, V_{CC} MIN = 4.75V, V_{CC} MAX = 5.25V MIN	TYP	MAX	UNIT
V_{OL}	Bus output LOW voltage	V_{CC} = MIN	I_{OL} = 24mA			0.4			0.4	V
			I_{OL} = 40mA			0.5			0.5	
V_{OH}	Bus output HIGH voltage	V_{CC} = MIN	I_{OH} = −20mA	2.4			2.4			V
I_O	Bus leakage current (high impedance)	V_{CC} = MAX, Bus enable = 2.4V	V_O = 0.4V			−200			−200	μA
			V_O = 2.4V			50			50	
			V_O = 4.5V			100			100	
I_{OFF}	Bus leakage current (power OFF)	V_O = 4.5V, V_{CC} = OV				100			100	μA
V_{IH}	Receiver input HIGH threshold	Bus enable = 2.4V		2.0			2.0			V
V_{IL}	Receiver input LOW threshold	Bus enable = 2.4V				0.8			0.8	V
I_{SC}	Bus output short Circuit current	V_{CC} = MAX, V_O = OV		−50	−85	−130	−50	−85	−130	mA

Electrical Characteristics

Over Recommended Operating Range

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MILITARY T_A = −55°C to +125°C, V_{CC} MIN = 4.50V, V_{CC} MAX = 5.50V MIN	MILITARY TYP[2]	MILITARY MAX	COMMERCIAL T_A = 0°C to +70°C, V_{CC} MIN = 4.75V, V_{CC} MAX = 5.25V MIN	COMMERCIAL TYP[2]	COMMERCIAL MAX	UNIT
V_{OH}	Receiver output HIGH voltage	V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH}	I_{OH} = −1.0mA	2.4	3.4					V
			I_{OH} = −2.6mA				2.4	3.4		
		V_{CC} = 5.0V, I_{OH} = −100μA		3.5			3.5			V
V_{OH}	Parity output HIGH voltage	V_{CC} = MIN, I_{OH} = −660μA, V_{IN} = V_{IH} or V_{IL}		2.5	3.4		2.7	3.4		V
V_{OL}	Output LOW voltage (except bus)	V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH}	I_{OL} = 4mA		0.27	0.4		0.27	0.4	V
			I_{OL} = 8mA		0.32	0.45		0.32	0.5	
			I_{OL} = 12mA		0.37	0.5		0.37	0.5	
V_{IH}	Input HIGH level (except bus)	Guaranteed input logical HIGH for all inputs		2.0			2.0			V
V_{IL}	Input LOW level (except bus)	Guaranteed input logical LOW for all inputs							0.8	V
V_I	Input clamp voltage (except bus)	V_{CC} = MIN, I_{IN} = −18mA				−1.2			−1.2	V
I_{IL}	Input LOW current (except bus)	V_{CC} = MAX, V_{IN} = 0.4V	$\overline{BE}$, $\overline{RLE}$			−0.72			−0.72	mA
			All other inputs			−0.36			−0.36	
I_{IH}	Input HIGH current (except bus)	V_{CC} = MAX, V_{IN} = 2.7V				20			20	μA
I_I	Input HIGH current (except bus)	V_{CC} = MAX, V_{IN} = 7.0V				100			100	μA
I_{SC}	Output short circuit current (except bus)	V_{CC} = MAX		−30		−85	−30		−85	mA
I_{CC}	Power supply currents	V_{CC} = MAX, all inputs = GND			63	95		63	95	mA
I_O	Off-state output current (receiver outputs)	V_{CC} = MAX.	V_O = 2.4V			20			20	μA
			V_O = 0.4V			−20			−20	

Input/Output Current Interface Conditions



Note: Actual current flow direction shown.

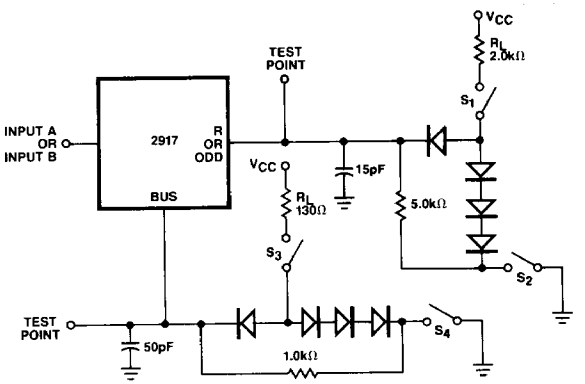
Switching Characteristics

Over Recommended Operating Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY T_A = −55°C to +125°C V_{CC} MIN = 4.50V V_{CC} MAX = 5.50V MIN	TYP[2]	MAX	COMMERCIAL T_A = 0°C to +70°C V_{CC} MIN = 4.75V V_{CC} MAX = 5.25V MIN	TYP[2]	MAX	UNIT
t_{PHL}	Driver clock (DRCP) to bus	C_L(bus) = 50pF, R_L(bus) = 50Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus enable ($\overline{BE}$) to bus			13	26		13	23	ns
t_{HZ}, t_{LZ}				13	26		13	23	
t_s	A data inputs	C_L = 15pF, R_L = 2.0kΩ	23			20			ns
t_h			8.0			6.0			
t_{PW}	Clock pulse width (HIGH)		20			17			ns
t_{PLH}	Bus to receiver output (latch enabled)			18	30		18	27	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch enable to receiver output			21	30		21	27	ns
t_{PHL}				21	30		21	27	
t_s	Bus to latch enable ($\overline{RLE}$)		17			14			ns
t_h			6.0			4.0			
t_{PLH}	A data to odd parity out (driver enabled)			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{PLH}	Bus to odd parity out (driver inhibit)			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{PLH}	Latch enable ($\overline{RLE}$) to odd parity output			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{ZH}, t_{ZL}	Output control to output			14	26		14	23	ns
t_{HZ}, t_{LZ}				14	26		14	23	

Notes: 1. For conditions shown as MIN, or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Standard Test Load Circuit



Function Table

INPUTS					INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
A_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	BUS_i	R_i	
X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	H	L	L	X	H	H	L	
X	X	X	H	X	X	NC	X	X	Latch received data
L	↑	X	X	X	L	X	X	X	Load driver register
H	↑	X	X	X	H	X	X	X	
X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	H	X	X	X	NC	X	X	X	
X	X	L	X	X	L	X	H	X	Drive Bus
X	X	L	X	X	H	X	L	X	

H = HIGH Z = High Impedance X = Don't Care i = 0, 1, 2, 3
L = LOW NC = No Change ↑ = LOW-to-HIGH Transition

Definition of Functional Terms

Driver clock pulse, DRCP
Clock pulse for the driver register.

Bus enable, $\overline{BE}$
When the bus enable is LOW, the four drivers are in the high impedance state.

Driver outputs and receiver inputs, BUS_0, BUS_1, BUS_2, BUS_3
Four driver outputs and receiver inputs (data is inverted).

Receiver outputs, R_0, R_1, R_2, R_3
The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

Receiver latch enable, $\overline{RLE}$
When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

Odd parity output, ODD
Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

Output enable, $\overline{OE}$
When the $\overline{OE}$ input is HIGH, the four three-state receiver outputs are in the high-impedance state.

Parity Output Function Table

$\overline{BE}$	ODD PARITY OUTPUT
L	$ODD = A_0 \oplus A_1 \oplus A_2 \oplus A_3$
H	$ODD = Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$