Spread Spectrum 3 DIMM Desktop Clock

Features

- Maximized EMI Suppression using IC WORKS'Spread Spectrum Technology
- Outputs
  - 4 CPU Clock (2.5V or 3.3V, 60 to 100MHz)
  - 7 PCI (3.3V)
  - 1 48MHz for USB (3.3V)
  - 1 24MHz for Super I/O (3.3V)
  - 2 REF (3.3V)
  - 1 IOAPIC (2.5V or 3.3V)
  - 12 SDRAM (3.3V)
- Serial data interface provides additional frequency selection, individual clock output disable, and other functions
- Smooth transition supports dynamic frequency assignment
- Spread Spectrum enabled after power-up
- Frequency selection not affected during power down/up cycle
- Supports a variety of power saving options
- Available in 48-pin SSOP (300 mils)

Key Specifications

Spread Spectrum Modulation:	±0.5%
Jitter (cycle-to-cycle):	250ps
Duty Cycle:	45-55%
Output Skew (PCI-PCI or CPU-CPU)	250ps

Figure 1 Block Diagram

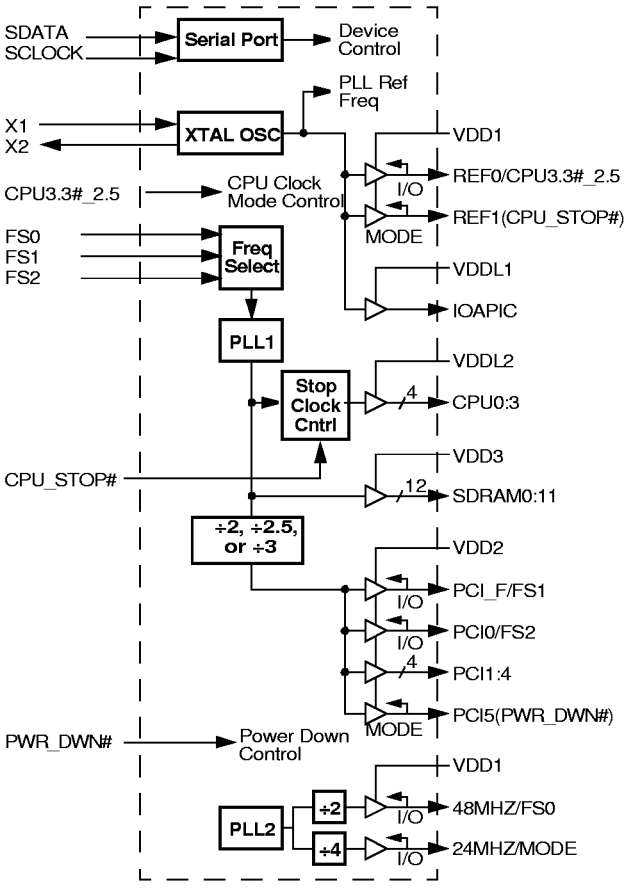


Table 1 Order Information

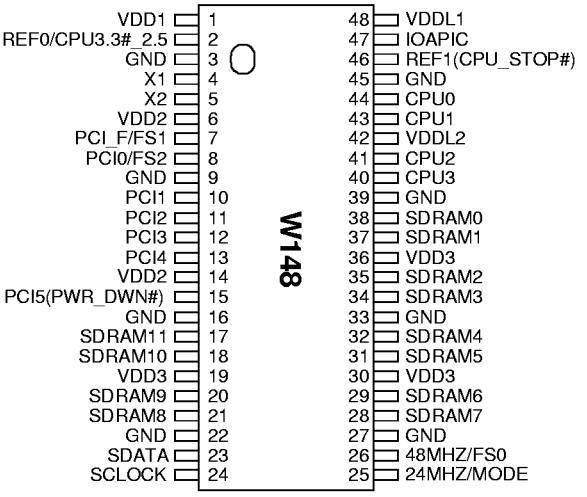
Part Number	Package
W148	H = SSOP (300 mils)

Table 2 Pin Selectable Frequency (Note)

Input Address			CPU, SDRAM Clocks (MHz)	PCI Clocks (MHz)
FS2	FS1	FS0		
0	0	0	95.25	31.75
0	0	1	75.0	30.0
0	1	0	80.0	32.0
0	1	1	100.0	33.3
1	0	0	83.3	33.3
1	0	1	75.0	37.5
1	1	0	70.0	35.0
1	1	1	66.8	33.4

Note: Additional frequency selections provided by serial data interface; refer to Table 6 on page 8.

Figure 2 Pin Diagram



Note: Signal names in parenthesis denotes function is selectable through mode pin resistor strapping.

Overview

The W148, a motherboard clock synthesizer, can provide either a 2.5V or 3.3V CPU clock swing making it suitable for a variety of CPU options. Twelve SDRAM clocks are provided in phase with the CPU clock outputs. This provides clock support for up to three SDRAM DIMMs. Fixed output frequency clocks are provided for other system functions.

Functional Description

I/O Pin Operation

Pins 2, 7, 8, 25 and 26 are dual purpose I/O pins. Upon power up these pins act as logic inputs, allowing the determination of assigned device functions. A short time after power up, the logic state of these pins is latched and the pins then become clock outputs. This feature reduces device pin count by combining clock outputs with input select pins.

An external 10 kohm "strapping" resistor is connected between each I/O pin and ground or VDD3. Connection to ground sets a latch to "0", connection to VDD3 sets a latch to "1". Figure 3 and Figure 4 show two suggested methods for strapping resistor connection.

Upon W148 power up, the first 2ms of operation is used for input logic selection. During this period, these dual purpose I/O pins are tristated, allowing the output strapping resistor on each I/O pin to pull the pin and its associated capacitive clock load to either a logic high or low state. At the end of the 2ms period, the established logic 0 or 1 condition of each I/O is pin is then latched. Next the output buffers are enabled converting the I/O pins into operating clock outputs. The 2ms timer starts when VDD reaches 2.0V. The input bits can only be reset by turning VDD off and then back on again.

It should be noted that the strapping resistors have no significant effect on clock output signal integrity. The drive impedance of the clock outputs is <40 ohms (nominal) which is minimally affected by the 10 kohm strap to ground or VDD. As with the series termination resistor, the output strapping resistor should be placed as close to the I/O pin as possible in order to keep the interconnecting trace short. The trace from the resistor to ground or VDD should be kept less than two inches in length to prevent system noise coupling during input logic sampling.

When the clock outputs are enabled following the 2ms input period, target (normal) output frequency is delivered assuming that VDD has stabilized. If VDD has not yet reached full value, output frequency initially may be below target but will increase to target once VDD voltage has stabilized. In either case, a short output clock cycle may be produced from the CPU clock outputs when the outputs are enabled.

Figure 3 Input Logic Selection Through Resistor Load Option

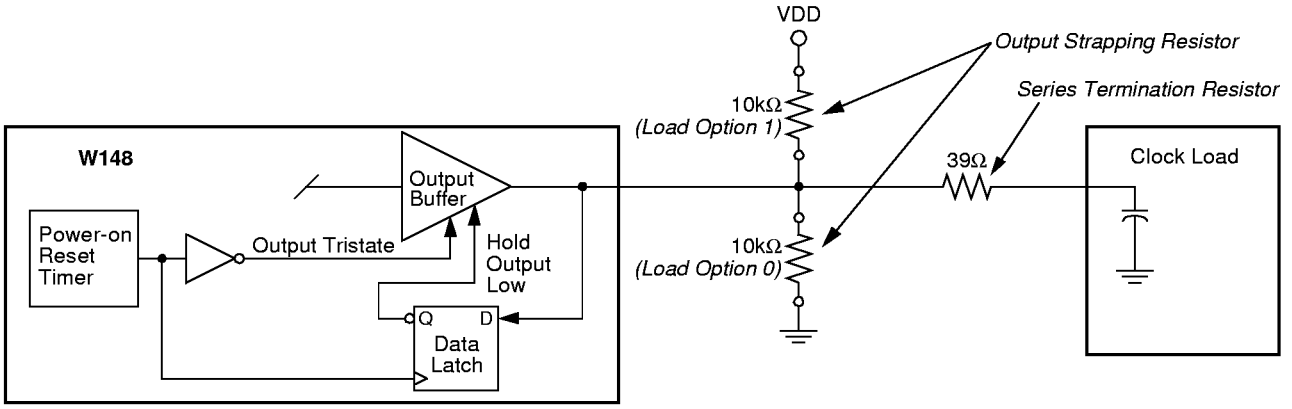
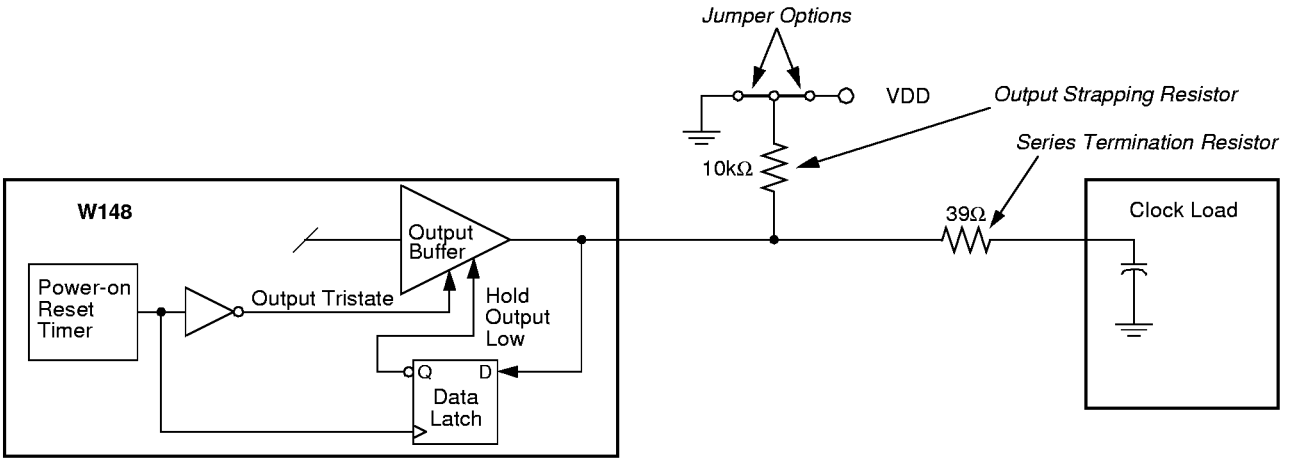


Figure 4 Input Logic Selection Through Jumper Option



CPU/PCI Frequency Selection

CPU frequency is selected with I/O pins 26, 7, and 8 (48MHz/FS0, PCI_F/FS1, and PCI0/FS2, respectively). Refer to Table 2 for CPU/PCI frequency programming information. Additional frequency selections are available through the serial data interface. Refer to Table 6, Additional Frequency Selections through Serial Data Interface Data Bytes on page 8.

Output Buffer Configuration

Clock Outputs

All clock outputs are designed to drive serial terminated clock lines. The W148 outputs are CMOS-type which provide rail-to-rail output swing. To accommodate the limited voltage swing required by some processors, the output buffers of CPU0:3 use a special VDDL2 power supply pin that may be tied to 2.5V nominal.

Crystal Oscillator

The W148 requires one input reference clock to synthesize all output frequencies. The reference clock can be either an externally generated clock signal or the clock generated by the internal crystal oscillator. When using an external clock signal, pin X1 is used as the clock input and pin X2 is left open. The input threshold voltage of pin X1 is VDD/2.

The internal crystal oscillator is used in conjunction with a quartz crystal connected to device pins X1 and X2. This forms a parallel resonant crystal oscillator circuit. The W148 incorporates the necessary feedback resistor and crystal load capacitors. Including typical stray circuit capacitance, the total load presented to the crystal is approximately 20pF. For optimum frequency accuracy without the addition of external capacitors, a parallel-resonant mode crystal specifying a load of 20pF should be used. This will typically yield reference frequency accuracies within ±100 ppm.

Dual Supply Voltage Operation

The W148 is designed for dual power supply operation. Supply pins VDD1, VDD2, and VDD3 are connected to a 3.3V supply and supply power to the internal core circuit and to the clock output buffers, except for outputs CPU0:3 and IOAPIC. Supply pins VDDL1 and VDDL2 may be connected to either a 2.5V or 3.3V supply.

Spread Spectrum Feature

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in Figure 5.

As shown in Figure 5, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is

$$dB = 6.5 + 9*\log_{10}(P) + 9*\log_{10}(F)$$

Where *P* is the percentage of deviation and*F* is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in Figure 6. This waveform, as discussed in "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions" by Bush, Fessler, and Hardin produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is± 0.5% of the center frequency. Figure 6 details the IC WORKS spreading pattern. IC WORKS does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

Figure 5 Clock Harmonic with and without SSCG Modulation Frequency Domain Representation

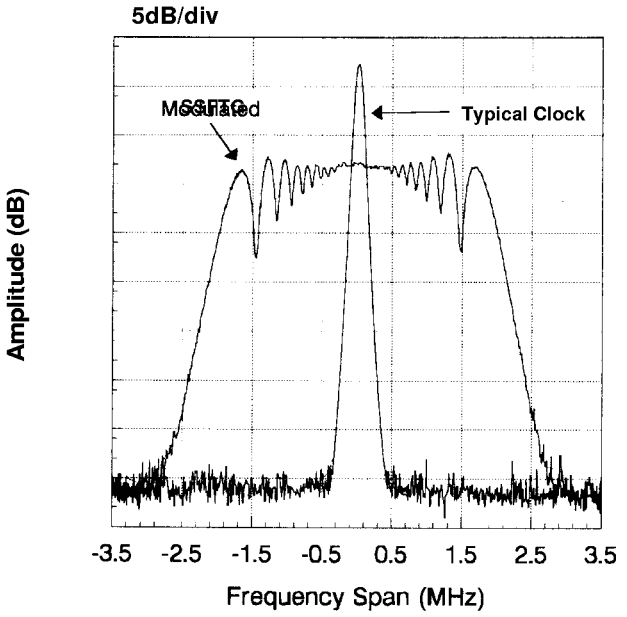
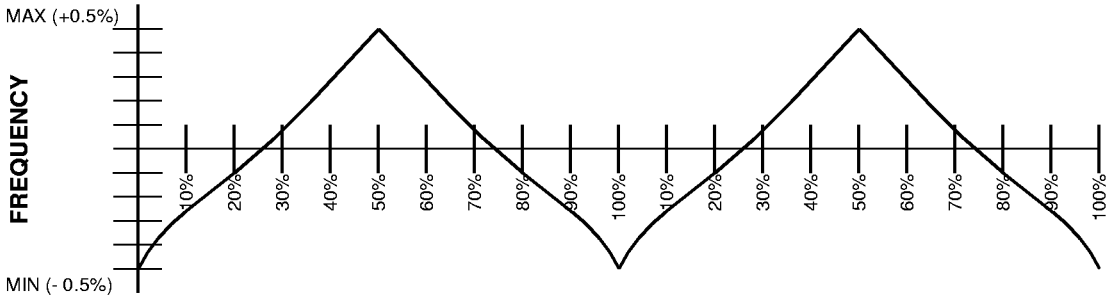


Figure 6 Typical Modulation Profile



Serial Data Interface

The W148 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the W148 initializes with default register settings, therefore the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDATA and SCLOCK. In motherboard applications, SDATA and SCLOCK are typically driven by two logic outputs of the chipset. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions. Table 3 summarizes the control functions of the serial data interface.

Table 3 Serial Data Interface Control Functions Summary

Control Function	Description	Common Application
Clock Output Disable	Any individual clock output(s) can be disabled. Disabled outputs are actively held low.	Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused SDRAM DIMM socket or PCI slot.
CPU Clock Frequency Selection	Provides CPU/PCI frequency selections. Frequency is changed in a smooth and controlled fashion.	For alternate CPU devices, and power management options. Smooth frequency transition allows CPU frequency change under normal system operation.
Output Tristate	Puts all clock outputs into a high impedance state.	Production PCB testing.
Test Mode	All clock outputs toggle in relation with X1 input, internal PLL is bypassed. Refer to Table 5.	Production PCB testing.
(Reserved)	Reserved function for future device revision or production device testing.	No user application. Register bit must be written as 0.

Operation

Data is written to the W148 in ten bytes of eight bits each. Bytes are written in the order shown in Table 4.

Table 4 Byte Writing Sequence

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the W148 to accept the bits in Data Bytes 0-6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the W148 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Dont' Care	Unused by the W148, therefore bit values are ignored (dont' care). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	Dont' Care	Unused by the W148, therefore bit values are ignored (dont' care). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.

Table 4 Byte Writing Sequence (cont.)

Byte Sequence	Byte Name	Bit Sequence	Byte Description
4	Data Byte 0	Refer to Table 5	The data bits in these bytes set internal W148 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to Table 5, Data Byte Serial Configuration Map.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3		
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6		

Writing Data Bytes

Each bit in the data bytes control a particular device function except for the "reserved" bits which must be written as a logic 0. Bits are written MSB (most significant bit) first, which is bit 7. Table 5 gives the bit formats for registers located in Data Bytes 0-6. Table 6 details additional frequency selections that are available through the serial data interface. Table 7 details the select functions for Byte 0, bits 1 and 0.

Table 5 Data Bytes 0-6 Serial Configuration Map

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 0						
7	--	--	(Reserved)	--	--	0
6	--	--	BYT0_SEL2	Refer to Table 6		0
5	--	--	BYT0_SEL1	Refer to Table 6		0
4	--	--	BYT0_SEL0	Refer to Table 6		0
3	--	--	BYT0 /FS#	Frequency Controlled by FS (2:0)	Frequency Controlled by BYT0_SEL (2:0)	0
2	--	--	(Reserved)	--	--	0
1-0	--	--	Bit 1 Bit 0 Function (See Table 7 for function details) 0 0 Normal Operation 0 1 Test Mode 1 0 Reserved 1 1 All Outputs Tristated			00
Data Byte 1						
7	26	48MHZ	Clock Output Disable	Low	Active	1
6	25	24MHZ	Clock Output Disable	Low	Active	1
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	40	CPU3	Clock Output Disable	Low	Active	1
2	41	CPU2	Clock Output Disable	Low	Active	1
1	43	CPU1	Clock Output Disable	Low	Active	1
0	44	CPU0	Clock Output Disable	Low	Active	1
Data Byte 2						
7	--	--	(Reserved)	--	--	0
6	7	PCI_F	Clock Output Disable	Low	Active	1
5	15	PCI5	Clock Output Disable	Low	Active	1

Table 5 Data Bytes 0-6 Serial Configuration Map (cont.)

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
4	13	PCI4	Clock Output Disable	Low	Active	1
3	12	PCI3	Clock Output Disable	Low	Active	1
2	11	PCI2	Clock Output Disable	Low	Active	1
1	10	PCI1	Clock Output Disable	Low	Active	1
0	8	PCI0	Clock Output Disable	Low	Active	1
Data Byte 3						
7	28	SDRAM7	Clock Output Disable	Low	Active	1
6	29	SDRAM6	Clock Output Disable	Low	Active	1
5	31	SDRAM5	Clock Output Disable	Low	Active	1
4	32	SDRAM4	Clock Output Disable	Low	Active	1
3	34	SDRAM3	Clock Output Disable	Low	Active	1
2	35	SDRAM2	Clock Output Disable	Low	Active	1
1	37	SDRAM1	Clock Output Disable	Low	Active	1
0	38	SDRAM0	Clock Output Disable	Low	Active	1
Data Byte 4						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	17	SDRAM11	Clock Output Disable	Low	Active	1
2	18	SDRAM10	Clock Output Disable	Low	Active	1
1	20	SDRAM9	Clock Output Disable	Low	Active	1
0	21	SDRAM8	Clock Output Disable	Low	Active	1
Data Byte 5						
7	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	47	IOAPIC	Clock Output Disable	Low	Active	1
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	46	REF1	Clock Output Disable	Low	Active	1
0	2	REF0	Clock Output Disable	Low	Active	1
Data Byte 6						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	--	--	(Reserved)	--	--	0
0	--	--	(Reserved)	--	--	0

Table 6 Additional Frequency Selections through Serial Data Interface Data Bytes

Input Conditions			Output Frequency	
Data Byte 0, Bit 3 = 1				
Bit 6 BYT0_SEL2	Bit 5 BYT0_SEL1	Bit 4 BYT0_SEL0	CPU, SDRAM Clocks (MHz)	PCI Clocks (MHz)
0	0	0	95.25	31.75
0	0	1	75.0	30.0
0	1	0	80.0	32.0
0	1	1	100.0	33.3
1	0	0	83.3	33.3
1	0	1	75.0	37.5
1	1	0	70.0	35.0
1	1	1	66.8	33.4

Table 7 Select Function for Data Byte 0, Bits 0:1

Function	Input Conditions		Output Conditions			
	Data Byte 0		CPU0:3, SDRAM0:11	PCI_F, PCI0:5	REF0:1, IOAPIC	48/24MHZ
	Bit 1	Bit 0				
Normal Operation	0	0	Note 1	Note 1	14.318MHz	48/24MHz
Test Mode	0	1	X1/2	X1/4	X1	Note 2
Reserved	1	0	reserved	reserved	reserved	reserved
Tristate	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Notes: 1. CPU, SDRAM and PCI frequency selections are listed in Table 2 and Table 6.

2. In Test Mode, the 48/24MHz clock outputs are:
   - X1/2 for 48MHz output
   - X1/4 for 24MHz output

How To Use the Serial Data Interface

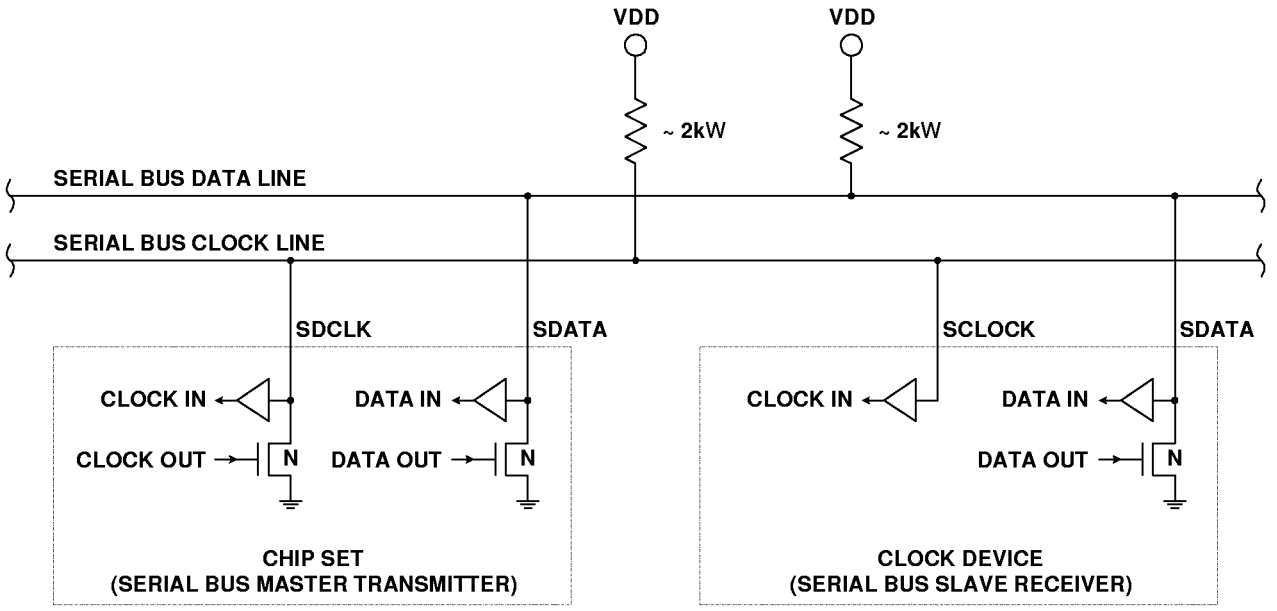
Electrical Requirements

Figure 7 illustrates electrical characteristics for the serial interface bus used with the W148. Devices send data over the bus with an open drain logic output that can (a) pull the bus line low, or (b) let the bus default to logic 1. The pull-up resistors on the bus (both clock and data lines) establish a default logic 1. All bus devices generally have logic inputs to receive data.

Although the W148 is a receive-only device (no data write-back capability), it does transmit an "acknowledge" data pulse after each byte is received. Thus, the SDATA line can both transmit and receive data.

The pull-up resistor should be sized to meet the rise and fall times specified in AC parameters, taking into consideration total bus line capacitance.

Figure 7 Serial Interface Bus Electrical Characteristics



Signaling Requirements

As shown in Figure 8, valid data bits are defined as stable logic 0 or 1 condition on the data line during a clock high (logic 1) pulse. A transitioning data line during a clock high pulse may be interpreted as a start or stop pulse (it will be interpreted as a start or stop pulse if the start/stop timing parameters are met).

A write sequence is initiated by a "start bit" as shown in Figure 9. A "stop bit" signifies that a transmission has ended.

As stated previously, the W148 sends an "acknowledge" pulse after receiving eight data bits in each byte as shown in Figure 10.

Sending Data to the W148

The device accepts data once it has detected a valid start bit and address byte sequence. Device functionality is changed upon the receipt of each data bit (registers are not double buffered). Partial transmission is allowed meaning that a transmission can be truncated as soon as the desired data bits are transmitted (remaining registers will be unmodified). Transmission is truncated with either a stop bit or new start bit (restart condition).

Figure 8 Serial Data Bus Valid Data Bit

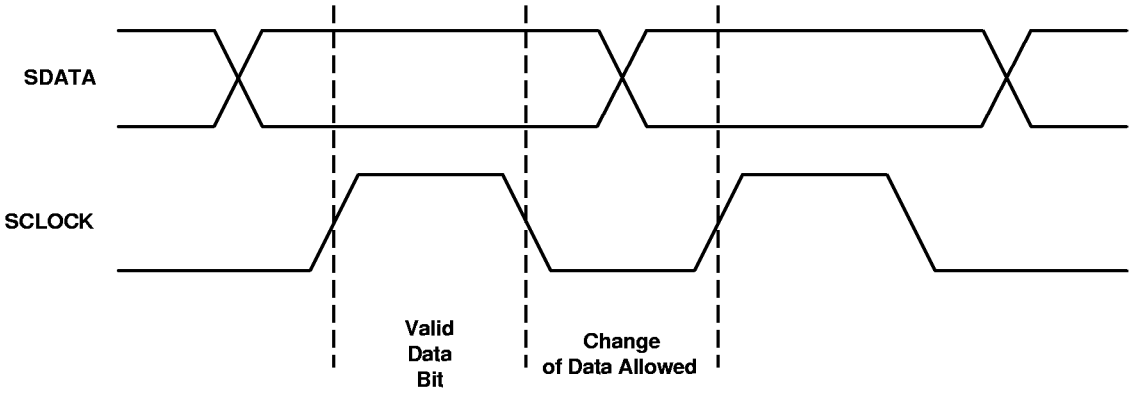


Figure 9 Serial Data Bus Start and Stop Bit

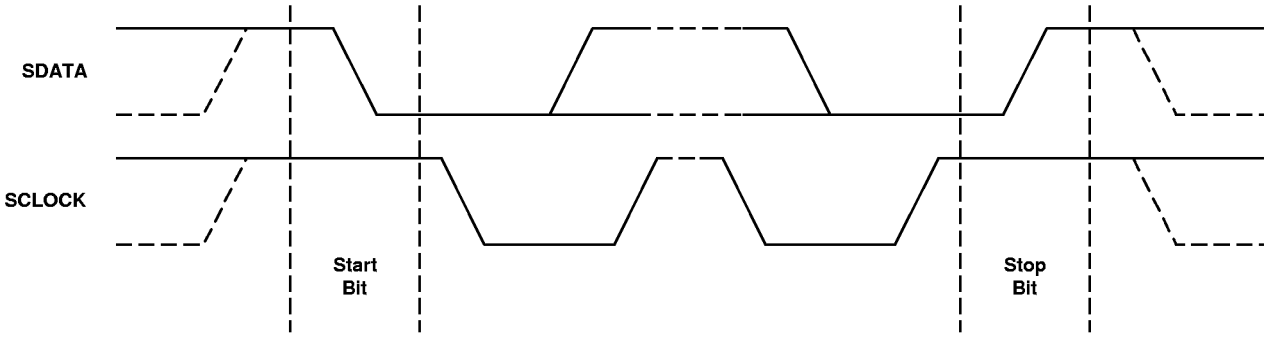


Figure 10 Serial Data Bus Write Sequence

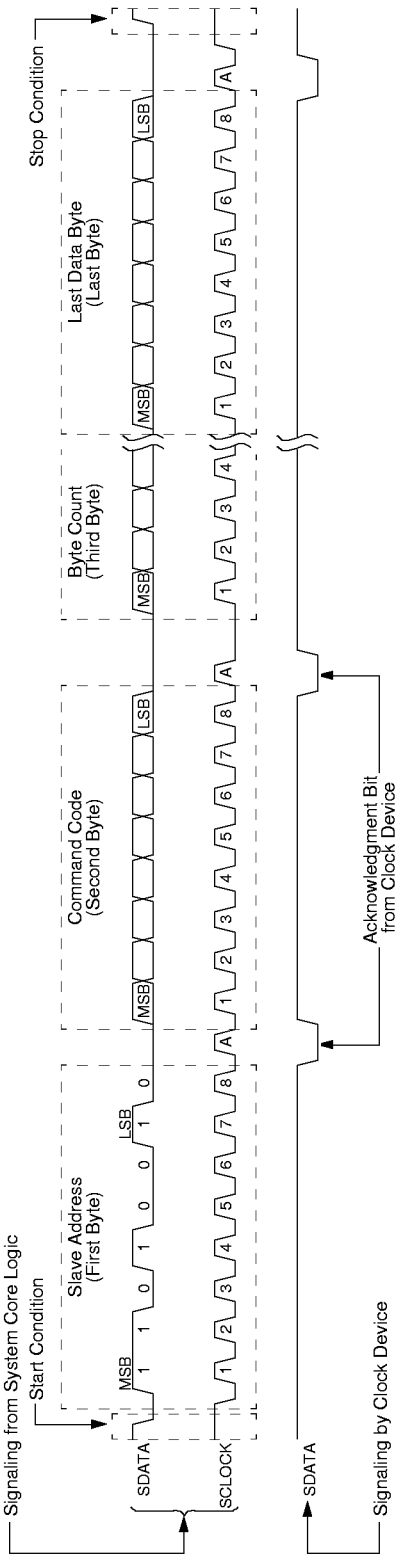
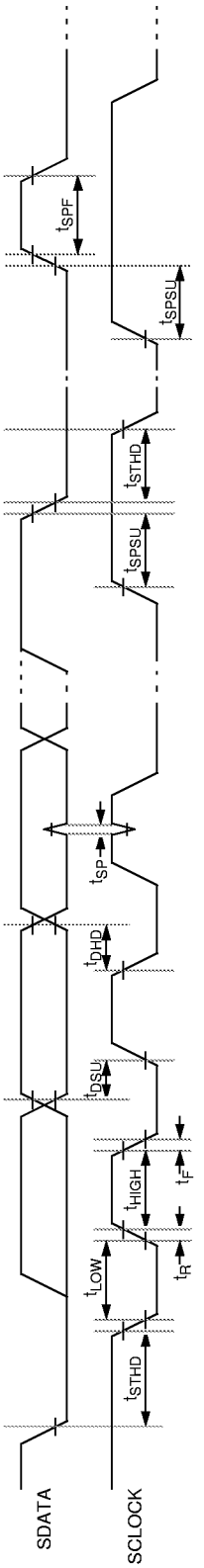


Figure 11 Serial Data Bus Timing Diagram



Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CPU0:3	44, 43, 41, 40	O	***CPU Clock Outputs 0 through 3:*** These four CPU clock outputs are controlled by the CPU_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDL2 and output characteristics are adjusted by input CPU3.3#_2.5.
PCI_F/FS1	7	I/O	***Fixed PCI Clock Output and Frequency Selection Bit 1:*** As an output, this pin works in conjunction with PCI0:5. Output voltage swing is controlled by voltage applied to VDD2. When an input, this pin functions as part of the frequency selection address. The value of FS0:2 determines the power-up default frequency of device output clocks as per the Table 2, "Pin Selectable Frequency" on page 1.
PCI0/FS2	8	I/O	***PCI Bus Clock Output 0 and Frequency Selection Bit 2:*** As an output, this pin works in conjunction with PCI1:5 and PCI_F. Output voltage swing is controlled by voltage applied to VDD2. When an input, this pin functions as part of the frequency selection address. The value of FS0:2 determines the power-up default frequency of device output clocks as per the Table 2, "Pin Selectable Frequency" on page 1.
PCI1:4	10, 11, 12, 13	O	***PCI Bus Clock Outputs 1 through 4:*** Output voltage swing is controlled by voltage applied to VDD2.
PCI5(PWR_DWN#)	15	I/O	***PCI Bus Clock Output 5 or Power Down Control:*** As an output, this pin works in conjunction with PCI0:4 and PCI_F. Output voltage swing is controlled by voltage applied to VDD2. If programmed as an input (refer to MODE pin description), this pin is used for power down control. When low, the device goes into a low power standby condition. All outputs are actively held low while in power down. CPU, SDRAM and PCI clock outputs are stopped low after completing a full clock cycle (2-4 CPU clock cycle latency). When brought high, CPU, SDRAM and PCI outputs start with a full clock cycle at full operating frequency (3ms maximum latency).
SDRAM0:11	38, 37, 35, 34, 32, 31, 29, 28, 21, 20, 18, 17	O	***SDRAM Clock Outputs 0 through 11:*** These twelve SDRAM clock outputs run synchronous to the CPU clock outputs. Output voltage swing is controlled by voltage applied to VDD3.
IOAPIC	47	O	***I/O APIC Clock Output:*** Provides 14.318MHz fixed frequency. The output voltage swing is controlled by VDDL1.
48MHZ/FS0	26	I/O	***48MHz Output and Frequency Selection Bit 0:*** Fixed clock output that defaults to 48MHz following device power-up. Output voltage swing is controlled by voltage applied to VDD1. When an input, this pin functions as part of the frequency selection address. The value of FS0:2 determines the power-up default frequency of device output clocks as per the Table 2, "Pin Selectable Frequency" on page 1.

Pin Definitions (cont.)

Pin Name	Pin No.	Pin Type	Pin Description
24MHZ/MODE	25	I/O	***24MHz Output and Mode Control Input:*** Fixed clock output that defaults to 24MHz following device power-up. Output voltage swing is controlled by voltage applied to VDD1. When an input, this pin is used for pin programming selection. It determines the functions for pins 15 and 46: **MODE** **Pin 15** **Pin 46** 0 PWR_DWN# (input) CPU_STOP# (input) 1 PCI5 (output) REF1 (output)
REF0/CPU3.3#_2.5	2	I/O	***Fixed 14.318MHz Output 0 and CPU Output Voltage Swing Selection Input:*** As an output, this pin is used for various system applications. Output voltage swing is controlled by voltage applied to VDD1. REF0 is stronger than REF1 and should be used for driving ISA slots. When an input, this pin selects the CPU clock output buffer characteristics that are optimized for either 3.3V or 2.5V operation. **CPU3.3#_2.5** **VDDQ2 Voltage (CPU0:3 Swing)** 0 3.3V 1 2.5V This input adjusts CPU clock output impedance so that a nominal 20 ohm output impedance is maintained. This eliminates or reduces the need to adjust external clock tuning components when changing VDDL2 voltage. CPU clock phase is also adjusted so that both CPU and SDRAM and CPU-to-PCI clock skew is maintained over the two VDDL2 voltage options. This input does not adjust IOAPIC clock output characteristics.
REF1(CPU_STOP#)	46	I/O	***Fixed 14.318MHz Output or CPU Clock Output Stop Control:*** Used for various system applications. Output voltage swing is controlled by voltage applied to VDD1. REF0 is stronger than REF1 and should be used for driving ISA slots. If programmed as an input (refer to MODE pin description), this pin is used for stopping the CPU clock outputs. When brought low, clock outputs CPU0:3 are stopped low after completing a full clock cycle (2-3 CPU clock latency). When brought high, clock outputs CPU0:3 are started beginning with a full clock cycle (2-3 CPU clock latency).
X1	4	I	***Crystal Connection or External Reference Frequency Input:*** This pin has dual functions. It can be used as an external 14.318MHz crystal connection or as an external reference frequency input.
X2	5	I	***Crystal Connection:*** An input connection for an external 14.318MHz crystal. If using an external reference, this pin must be left unconnected.
SDATA	23	I	***Serial Data Input:*** Data input for Serial Data Interface. Refer to Serial Data Interface section that follows.
SCLOCK	24	I	***Serial Clock Input:*** Clock input for Serial Data Interface. Refer to Serial Data Interface section that follows.
VDD1	1	P	***Power Connection:*** Power supply for crystal oscillator and REF0:1 output buffers. Connected to 3.3V supply.
VDD2	6,14	P	***Power Connection:*** Power supply for PCI clock output buffers. Connected to 3.3V supply.
VDDL1	48	P	***Power Connection:*** Power supply for IOAPIC output buffer. Connected to 2.5V or 3.3V supply.

Pin Definitions (cont.)

Pin Name	Pin No.	Pin Type	Pin Description
VDDL2	42	P	***Power Connection:*** Power supply for CPU clock output buffers. Connected to 2.5V or 3.3V supply.
VDD3	19, 30, 36	P	***Power Connection:*** Power supply for SDRAM clock output buffers. Connected to 3.3V supply.
GND	3, 9, 16, 22, 27, 33, 39, 45	G	***Ground Connection:*** Connect all ground pins to the common system ground plane.

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
T_A	Operating Temperature	0 to +70	°C
ESD_{PROT}	Input ESD Protection	2 (min)	kV

Crystal Oscillator

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{TH}	X1 Input threshold Voltage (Note 3)		1.65		V	VDD1:3 = 3.3V
C_{LOAD}	Load Capacitance, Seen By external crystal (Note 4)		20		pF	
$C_{IN,X1}$	X1 Input Capacitance (Note 5)		40		pF	Pin X2 unconnected

3.3V DC Electrical Characteristics (CPU3.3#_2.5 Input = 0)

T_A = 0°C to +70°C, VDD1:3 = VDD1:2 = 3.3V±5% (3.135-3.465V)

Symbol	Parameter		Min	Typ	Max	Unit	Test Condition
Supply Current							
I_{DD}	Combined 3.3V Supply Current				365	mA	CPU0:3 = 66.8MHz Outputs Loaded (Note 1)
Logic Inputs							
V_{IL}	Input Low Voltage				0.8	V	
V_{IH}	Input High Voltage		2.0			V	
I_{IL}	Input Low Current (Note 2)				10	µA	
I_{IH}	Input High Current (Note 2)				10	µA	
Clock Outputs							
V_{OL}	Output Low Voltage				50	mV	I_{OL} = 1mA
V_{OH}	Output High Voltage		3.1			V	I_{OH} = –1mA
I_{OL}	Output Low Current:	CPU0:3	55	75	105	mA	V_{OL} = 1.5V
		SDRAM0:11	80	110	155		
		PCI_F, PCI0:5	55	75	105		
		IOAPIC	100	135	190		
		REF0	60	75	90		
		REF1	45	60	75		
		48/24MHZ	55	75	105		

3.3V DC Electrical Characteristics (CPU3.3#_2.5 Input = 0) (cont.)

T_A = 0°C to +70°C, VDD1:3 = VDD1.1:2 = 3.3V±5% (3.135-3.465V)

Symbol	Parameter		Min	Typ	Max	Unit	Test Condition
I_{OH}	Output High Current:	CPU0:3	55	85	125	mA	V_{OH} = 1.5V
		SDRAM0:11	80	120	175		
		PCI_F, PCI0:5	55	85	125		
		IOAPIC	100	150	220		
		REF0	60	85	110		
		REF1	45	65	90		
		48/24MHZ	55	85	125		
Pin Capacitance/Inductance							
C_{IN}	Input Pin Capacitance				5	pF	Except X1 and X2
C_{OUT}	Output Pin Capacitance				6	pF	
L_{IN}	Input Pin Inductance				7	nH	
Serial Input Port							
V_{IL}	Input Low Voltage				$0.3V_{DD}$	V	V_{DD} = 3.3V
V_{IH}	Input High Voltage		$0.7V_{DD}$			V	V_{DD} = 3.3V
I_{IL}	Input Low Current				10	µA	No internal pull-up/down on SCLOCK
I_{IH}	Input High Current				10	µA	No internal pull-up/down on SCLOCK
I_{OL}	Sink Current into SDATA, Open Drain N-Channel Device On		6			mA	$I_{OL} = 0.3V_{DD}$
C_{IN}	Input Capacitance of SDATA and SCLOCK				10	pF	
C_{SDATA}	Total Capacitance of SDATA Bus				400	pF	
C_{SCLOCK}	Total Capacitance of SCLOCK Bus				400	pF	

Notes:
1. All clock outputs loaded with maximum lump capacitance test load specified in AC Electrical Characteristics section.
2. W148 logic inputs have internal pull-up devices (pull-ups not CMOS level).
3. X1 input threshold voltage (typical) is VDD1/2.
4. The W148 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load seen by crystal is 20pF; this includes typical stray capacitance of short PCB traces to crystal.
5. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).
6. CPU0:3 loaded by 60Ω, 6-inch long transmission lines ending with 20pF capacitors.

2.5V DC Electrical Characteristics (CPU3.3#_2.5 Input = 1)

T_A = 0°C to +70°C, VDD1:3 = 3.3V±5% (3.135-3.456V), VDD1:2 = 2.5V±5% (2.375-2.625V)

Symbol	Parameter		Min	Typ	Max	Unit	Test Condition
Supply Current							
$I_{DD-3.3V}$	3.3V Supply Current				300	mA	CPU0:3 = 66.8MHz Outputs Loaded (Note 1)
$I_{DD-2.5}$	2.5V Supply Current				50	mA	CPU0:3= 66.8MHz Outputs Loaded (Note 1)
Logic Inputs							
V_{IL}	Input Low Voltage				0.8	V	
V_{IH}	Input High Voltage		2.0			V	
I_{IL}	Input Low Current (Note 2)				10	µA	
I_{IH}	Input High Current (Note 2)				10	µA	
Clock Outputs							
V_{OL}	Output Low Voltage				50	mV	I_{OL} = 1mA
V_{OH}	Output High Voltage		2.2			V	I_{OH} = –1mA
I_{OL}	Output Low Current:	CPU0:3	45	70	105	mA	V_{OL} = 1.25V
		IOAPIC	55	85	130		V_{OL} = 1.25V
I_{OH}	Output High Current:	CPU0:3	40	65	95	mA	V_{OH} = 1.25V
		IOAPIC	50	80	120		V_{OH} = 1.25V
Pin Capacitance/Inductance							
C_{IN}	Input Pin Capacitance				5	pF	Except X1 and X2
C_{OUT}	Output Pin Capacitance				6	pF	
L_{IN}	Input Pin Inductance				7	nH	
Serial Input Port							
V_{IL}	Input Low Voltage				$0.3V_{DD}$	V	V_{DD} = 2.5V
V_{IH}	Input High Voltage		$0.7V_{DD}$			V	V_{DD} = 2.5V

Notes:
1. All clock outputs loaded with maximum lump capacitance test load specified in AC Electrical Characteristics section.
2. W148 logic inputs have internal pull-up devices (pull-ups not CMOS level).
3. X1 input threshold voltage (typical) is VDD1/2.
4. The W148 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load as seen by crystal is 20pF; this includes typical stray capacitance of short PCB traces to crystal.
5. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).
6. CPU0:3 loaded by 60Ω, 6-inch long transmission lines ending with 20pF capacitors.

3.3V AC Electrical Characteristics (CPU3.3#_2.5 Input = 0)

T_A = 0°C to +70°C, VDD3:3 = VDD1:3 = 3.3V±5% (3.135-3.465V), f_{XTL} = 14.31818MHz

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.

CPU Clock Outputs, CPU0:3 (Lump Capacitance Test Load = 20pF)

Symbol	Parameter	CPU = 66.8MHz			Unit	Test Condition/Comments
		Min	Typ	Max		
t_P	Period	15			ns	Measured on rising edge at 1.5V.
f	Frequency, Actual		66.8		MHz	Determined by PLL divider ratio.
t_H	High Time	5.2			ns	Duration of clock cycle above 2.4V.
t_L	Low Time	5			ns	Duration of clock cycle below 0.4V.
t_R	Output Rise Edge Rate	1		4	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	1		4	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	45		55	%	Measured on rising and falling edge at 1.5V.
t_{JC}	Jitter, Cycle-to-Cycle			250	ps	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.
t_{SK}	Output Skew			250	ps	Measured on rising edge at 1.5V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance	15	20	30	ohm	Average value during switching transition. Used for determining series termination value.

SDRAM Clock Outputs, SDRAM0:11 (Lump Capacitance Test Load = 30pF)

Symbol	Parameter	CPU = 66.8MHz			Unit	Test Condition/Comments
		Min	Typ	Max		
t_P	Period	15			ns	Measured on rising edge at 1.5V.
f	Frequency, Actual		66.8		MHz	Determined by PLL divider ratio.
t_R	Output Rise Edge Rate	1		4	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	1		4	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	45		55	%	Measured on rising and falling edge at 1.5V.
t_{JC}	Jitter, Cycle-to-Cycle			250	ps	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.
t_{SK}	Output Skew		100		ps	Measured on rising edge at 1.5V.
t_{SK}	CPU to SDRAM Clock Skew			500	ps	Covers all CPU/SDRAM outputs. Measured on rising edge at 1.5V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance	10	15	20	ohm	Average value during switching transition. Used for determining series termination value.

3.3V AC Electrical Characteristics (CPU3.3#_2.5 Input = 0) (cont.)

PCI Clock Outputs, PCI_F and PCI0:5 (Lump Capacitance Test Load = 30pF)

Symbol	Parameter	CPU = 66.8MHz			Unit	Test Condition/Comments
		Min	Typ	Max		
t_P	Period	30			ns	Measured on rising edge at 1.5V.
f	Frequency, Actual		33.4		MHz	Determined by PLL divider ratio.
t_H	High Time	12			ns	Duration of clock cycle above 2.4V.
t_L	Low Time	12			ns	Duration of clock cycle below 0.4V.
t_R	Output Rise Edge Rate	1		4	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	1		4	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	45		55	%	Measured on rising and falling edge at 1.5V.
t_{JC}	Jitter, Cycle-to-Cycle			250	ps	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.
t_{SK}	Output Skew			250	ps	Measured on rising edge at 1.5V.
t_O	CPU to PCI Clock Skew	1		4	ns	Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	ms	Assumes full supply voltage reached within 1ms from po up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance	15	20	30	ohm	Average value during switching transition. Used for dete ing series termination value.

IOAPIC Clock Output (Lump Capacitance Test Load = 20pF)

Symbol	Parameter	CPU = 66.8MHz			Unit	Test Condition/Comments
		Min	Typ	Max		
f	Frequency, Actual		14.31818		MHz	Frequency generated by crystal oscillator.
t_R	Output Rise Edge Rate	1		4	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	1		4	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	45		55	%	Measured on rising and falling edge at 1.5V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			1.5	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance	8	12	15	ohm	Average value during switching transition. Used for determining series termination value.

3.3V AC Electrical Characteristics (CPU3.3#_2.5 Input = 0) (cont.)

REF0 Clock Output (Lump Capacitance Test Load = 45pF)

Symbol	Parameter	CPU = 66.8MHz			Unit	Test Condition/Comments
		Min	Typ	Max		
f	Frequency, Actual		14.31818		MHz	Frequency generated by crystal oscillator.
t_R	Output Rise Edge Rate	1		4	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	1		4	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	40		60	%	Measured on rising and falling edge at 1.5V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			1.5	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance	17	20	25	ohm	Average value during switching transition. Used for determining series termination value.

REF1 Clock Output (Lump Capacitance Test Load = 20pF)

Symbol	Parameter	CPU = 66.8MHz			Unit	Test Condition/Comments
		Min	Typ	Max		
f	Frequency, Actual		14.31818		MHz	Frequency generated by crystal oscillator.
t_R	Output Rise Edge Rate	1		4	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	1		4	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	40		55	%	Measured on rising and falling edge at 1.5V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			1.5	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance	20	25	35	ohm	Average value during switching transition. Used for determining series termination value.

3.3V AC Electrical Characteristics (CPU3.3#_2.5 Input = 0) (cont.)

48/24MHZ Clock Outputs (Lump Capacitance Test Load = 20pF)

Symbol	Parameter	CPU = 66.8MHz			Unit	Test Condition/Comments
		Min	Typ	Max		
f	Frequency, Actual		48.008/24.004		MHz	Determined by PLL divider ratio (see n/m below).
f_D	Deviation from 48MHz		+167		ppm	(48.008 – 48)/48
m/n	PLL Ratio		57/17, 57/34			(14.31818MHz x 57/17 = 48.008MHz)
t_R	Output Rise Edge Rate	1		4	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	1		4	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	40		55	%	Measured on rising and falling edge at 1.5V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance	15	20	30	ohm	Average value during switching transition. Used for determining series termination value.

Serial Input Port

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
f_{SCLOCK}	SCLOCK Frequency	0		100	kHz	Normal Mode
t_{STHD}	Start Hold Time	4.0			µs	
t_{LOW}	SCLOCK Low Time	4.7			µs	
t_{HIGH}	SCLOCK High Time	4.0			µs	
t_{DSU}	Data Setup Time	250			ns	
t_{DHD}	Data Hold Time	0			ns	(Transmitter should provide a 300ns hold time to ensure proper timing at the receiver.)
t_R	Rise Time, SDATA and SCLOCK			1000	ns	From $0.3V_{DD}$ to $0.7V_{DD}$
t_F	Fall Time, SDATA and SCLOCK			300	ns	From $0.7V_{DD}$ to $0.3V_{DD}$
t_{STSU}	Stop Setup Time	4.0			µs	
t_{SPF}	Bus Free Time between Stop and Start Condition	4.7			µs	
t_{SP}	Allowable Noise Spike Pulse Width			50	ns	

2.5V AC Electrical Characteristics (CPU3.3#_2.5 Input = 1)

T_A = 0°C to +70°C, VDD1:3 = 3.3V±5% (3.135-3.465V), VDD1:2 = 2.5V±5% (2.375-2.625V), f_{XTL} = 14.31818MHz

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.

CPU Clock Outputs, CPU0:3 (Lump Capacitance Test Load = 20pF)

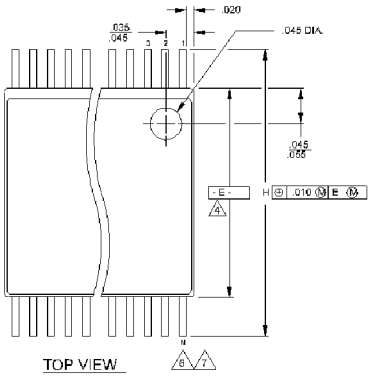
Symbol	Parameter	CPU = 66.8MHz			Unit	Test Condition/Comments
		Min	Typ	Max		
t_P	Period	15			ns	Measured on rising edge at 1.25V.
f	Frequency, Actual		66.8		MHz	Determined by PLL divider ratio.
t_H	High Time	5.2			ns	Duration of clock cycle above 2.0V.
t_L	Low Time	5			ns	Duration of clock cycle below 0.4V.
t_R	Output Rise Edge Rate	0.8		3	V/ns	Measured from 0.4V to 2.0V.
t_F	Output Fall Edge Rate	0.8		3	V/ns	Measured from 2.0V to 0.4V.
t_D	Duty Cycle	45		55	%	Measured on rising and falling edge at 1.25V.
t_{JC}	Jitter, Cycle-to-Cycle			250	ps	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.
t_{SK}	Output Skew			250	ps	Measured on rising edge at 1.25V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance	12	20	30	ohm	Average value during switching transition. Used for determining series termination value.

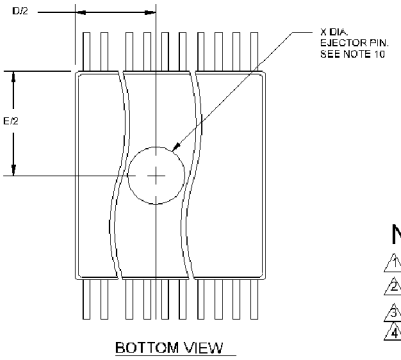
IOAPIC Clock Output (Lump Capacitance Test Load = 20pF)

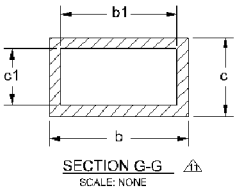
Symbol	Parameter	CPU = 66.8MHz			Unit	Test Condition/Comments
		Min	Typ	Max		
f	Frequency, Actual		14.31818		MHz	Frequency generated by crystal oscillator.
t_R	Output Rise Edge Rate	1		4	V/ns	Measured from 0.4V to 2.0V.
t_F	Output Fall Edge Rate	1		4	V/ns	Measured from 2.0V to 0.4V.
t_D	Duty Cycle	45		55	%	Measured on rising and falling edge at 1.25V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			1.5	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance	10	15	25	ohm	Average value during switching transition. Used for determining series termination value.

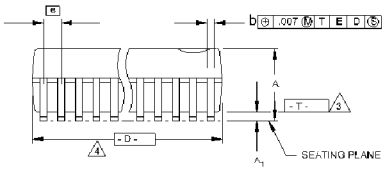
Mechanical Package Outline

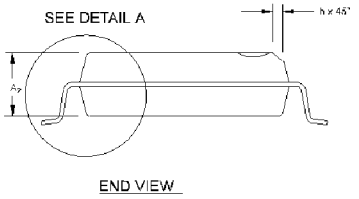
Figure 12 48-Pin Small Shrink Outline Package (SSOP, 300 mils)

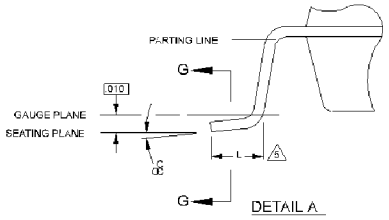












NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
2. DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. CONTROLLING DIMENSION: INCHES.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION.
11. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 INCHES AND .010 INCHES FROM THE LEAD TIPS.
12. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-118, VARIATIONS AA, AB, EXCEPT CHAMFER DIMENSION h. JEDEC SPECIFICATION FOR h IS .015"/.025".

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE 4			6
	MIN.	NOM.	MAX.	VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	.095	.102	.110	AA	.620	.625	.630	48
A_1	.008	.012	.016	AB	.720	.725	.730	56
A_2	.088	.090	.092					
b	.008	.010	.0135					
b_1	.008	.010	.012					
c	.005	-	.010					
c_1	.005	.006	.0085					
D	SEE VARIATIONS			4				
E	.292	.296	.299					
e	.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	SEE VARIATIONS			6				
X	.085	.093	.100	10				
α	0°	5°	8°					

THIS TABLE IN INCHES

Summary of nominal dimensions in inches:

Body Width: .296
Lead Pitch: .025
Body Length: .625
Body Height: .102

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE 4			6
	MIN.	NOM.	MAX.	VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	2.41	2.59	2.79	AA	15.75	15.88	16.00	48
A_1	0.20	0.31	0.41	AB	18.29	18.42	18.54	56
A_2	2.24	2.29	2.34					
b	0.203	0.254	0.343					
b_1	0.203	0.254	0.305					
c	0.127	-	0.254					
c_1	0.127	0.152	0.216					
D	SEE VARIATIONS			4				
E	7.42	7.52	7.59					
e	0.635 BSC							
H	10.16	10.31	10.41					
h	0.25	0.33	0.41					
L	0.61	0.81	1.02					
N	SEE VARIATIONS			6				
X	2.16	2.36	2.54	10				
α	0°	5°	8°					

THIS TABLE IN MILLIMETERS