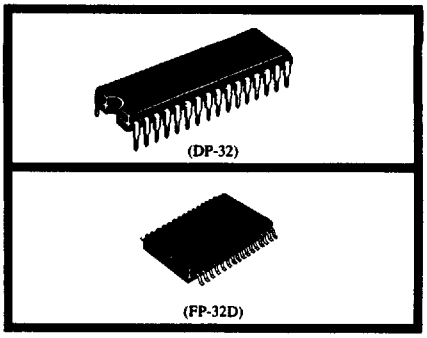
HM658512 Series

T-46-23-25

524,288-Word × 8-Bit High Speed Pseudo Static RAM

Features

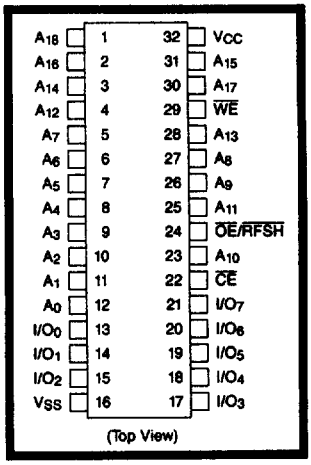
- Single 5 V (± 10%)
- High speed
  - Access time
    - $\overline{CE}$ access time ..... 80/100/120 ns
  - Cycle time
    - Random read/write cycle time ..... 130/160/190 ns
- Low power
  - Active: 250 mW (typ.)
  - Standby: 200 μW (typ.)
- All inputs and outputs TTL compatible
- Package
  - 32-pin dual-in-line plastic package
  - 32-pin SOP package
- Non multiplexed address
- 2048 refresh cycles (32 ms)
- Refresh functions
  - L/LL/LV-version ..... Address refresh
    Automatic refresh
    Self refresh
  - D-version ..... Address refresh
    Automatic refresh



■ ORDERING INFORMATION

Type No.	Access Time	Package
HM658512LP-8	80 ns	600 mil 32 pin Plastic DIP (DP-32)
HM658512LP-10	100 ns	
HM658512LP-12	120 ns	
HM658512DP-8	80 ns	
HM658512DP-10	100 ns	
HM658512DP-12	120 ns	
HM658512LP-8L	80 ns	
HM658512LP-10L	100 ns	
HM658512LP-12L	120 ns	
HM658512LP-8LV	80 ns	
HM658512LP-10LV	100 ns	
HM658512LP-12LV	120 ns	
HM658512LFP-8	80 ns	32 pin Plastic SOP (FP-32D)
HM658512LFP-10	100 ns	
HM658512LFP-12	120 ns	
HM658512DFP-8	80 ns	
HM658512DFP-10	100 ns	
HM658512DFP-12	120 ns	
HM658512LFP-8L	80 ns	
HM658512LFP-10L	100 ns	
HM658512LFP-12L	120 ns	
HM658512LFP-8LV	80 ns	
HM658512LFP-10LV	100 ns	
HM658512LFP-12LV	120 ns	

■ PIN ARRANGEMENT



■ PIN DESCRIPTION

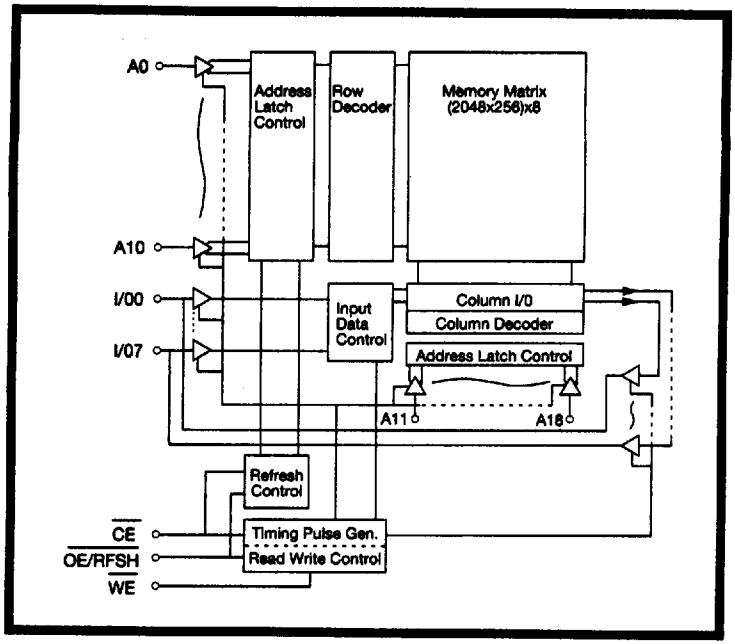
Pin Name	Function
A_0–A_{18}	Address
I/O_0–I/O_7	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}/\overline{RFSH}$	Output Enable/Refresh
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

4

NOTICE

SEE ORDER OF DATA FOR ERRATA INFORMATION

■ BLOCK DIAGRAM



Pin Functions

$\overline{CE}$: Chip Enable (Input)

$\overline{CE}$ is a basic clock. RAM is active when $\overline{CE}$ is low, and is on standby when $\overline{CE}$ is high.

A_0-A_{18}: Address Inputs (Input)

A_0-A_{10} is a row address and A_{11}-A_{18} is a column address. The entire address A_0-A_{18} is fetched into RAM by the falling edge of $\overline{CE}$.

$\overline{WE}$: Write Enable (Input)

RAM is in write mode when $\overline{WE}$ is low, and is in read mode when $\overline{WE}$ is high. I/O data is fetched into RAM by the rising edge of $\overline{WE}$ or $\overline{CE}$ (earlier timing) and the data is written into memory cells.

$\overline{OE}$/$\overline{RFSH}$: Output Enable/Refresh (Input)

This pin has two functions. Basically it works as $\overline{OE}$ when $\overline{CE}$ is low, and as $\overline{RFSH}$ when $\overline{CE}$ is high (in standby mode). After a read or write cycle finishes, refresh does not start if $\overline{CE}$ goes high while $\overline{OE}$/$\overline{RFSH}$ is held low. In order to start a refresh in standby mode, $\overline{OE}$/$\overline{RFSH}$ must go high to reset the refresh circuits of the RAM. After the refresh circuits are reset, the refresh starts when $\overline{OE}$/$\overline{RFSH}$ goes low.

I/O_0-I/O_7: Input/Output (Inputs and Outputs)

These pins are data I/O pins.

Refresh

There are three refresh modes: address refresh, automatic refresh, and self refresh.

(1) Address refresh

Data is refreshed by accessing all 2048 row addresses every 32 ms. A read is one method of accessing those addresses. Each row address (2048 addresses of A_0-A_{10}) must be read at least once every 32 ms. In address refresh mode, $\overline{OE}$/$\overline{RFSH}$ can remain high. In this case, the I/O pins remain at high impedance, but the refresh is done within RAM.

(2) Automatic refresh

Instead of address refresh, automatic refresh can be used. RAM goes to automatic refresh mode if $\overline{OE}$/$\overline{RFSH}$ falls while $\overline{CE}$ is high and it remains low for at least t_{FAP}. One automatic refresh cycle is executed by one low pulse of $\overline{OE}$/$\overline{RFSH}$. It is not necessary to input the refresh address from outside since it is generated internally by an on-chip address counter. 2048 automatic refresh cycles must be done every 32 ms.

(3) Self refresh

Self refresh mode is suitable for data retention by battery. In standby mode, a self refresh starts automatically when $\overline{OE}$/$\overline{RFSH}$ stays low for more than 8 μs. Refresh addresses are automatically specified by the on-chip address counter, and the refresh period is determined by the on-chip timer.

Automatic refresh and self refresh are distinguished from each other by the width of the $\overline{OE}/\overline{RFSH}$ low pulse in standby mode. If the $\overline{OE}/\overline{RFSH}$ low pulse is wider than 8 μs, RAM changes into self refresh mode; if the $\overline{OE}/\overline{RFSH}$ low pulse is less than 8 μs, it is recognized as an automatic refresh instruction.

Notes on Using the HM658512

Since pseudo static RAM consists of dynamic circuits like DRAM, it is more noise-sensitive than conventional SRAM.

(1) If a short $\overline{CE}$ pulse of a width less than t_{CE} min. is applied to RAM, an incomplete read occurs and stored data may be destroyed. Make sure that $\overline{CE}$ low pulses of less than t_{CE} min. are inhibited. Note that a 10 ns $\overline{CE}$ low pulse may sometimes occur owing to the gate delay on the board if the CE signal is generated by the decoding of higher address signals on the board. Avoid these short pulses.

(2) $\overline{OE}/\overline{RFSH}$ works as refresh control in standby mode. A short $\overline{OE}/\overline{RFSH}$ low pulse may cause an incomplete refresh that will destroy data. Make sure that $\overline{OE}/\overline{RFSH}$ low pulses of less than t_{FAP} min. are also inhibited.

T-46-23-25

(3) t_{OHC} and t_{OCD} are the timing specs which distinguish the $\overline{OE}$ function of $\overline{OE}/\overline{RFSH}$ from the $\overline{RFSH}$ function. The t_{OHC} and t_{OCD} specs must be strictly maintained.

(4) Start the HM658512 operating by executing at least eight initial cycles (dummy cycles) at least 100 μs after the power voltage reaches 4.5V–5.5V after power-on.

■ FUNCTION TABLE

$\overline{CE}$	$\overline{OE}/\overline{RFSH}$	$\overline{WE}$	I/O Pin	Mode
L	L	H	Low-Z	Read
L	X	L	High-Z	Write
L	H	H	High-Z	—
H	L	X	High-Z	Refresh
H	H	X	High-Z	Standby

NOTE: 1. X means don't care.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to V_{SS}	V_T	−1.0 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C

■ RECOMMENDED DC OPERATING CONDITIONS (T_A = 0°C to +70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.4	—	6.0	V
	V_{IL}	−1.0*1	—	0.8	V

NOTES: 1. V_{IL} min. = −3.0V for pulse width 30 ns.

4

■ DC CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Operating Power Supply Current	I_{CC1}	—	—	75	mA	$I_{I/O}$ = 0, t_{cyc} = min.
Standby Power Supply Current	I_{SB1}	—	1	2	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}/\overline{RFSH}$ = V_{IH}, V_{IN} ≥ 0V
	I_{SB2}	—	20	200 100*2	μA	$\overline{CE}$ ≥ V_{CC} -0.2V $\overline{OE}/\overline{RFSH}$ ≥ V_{CC} -0.2V V_{IN} ≥ 0V
Operating Power Supply Current in Self Refresh Mode	I_{CC2}	—	1	2	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}/\overline{RFSH}$ = V_{IL}, V_{IN} ≥ 0V
	I_{CC3}	—	70*1 40*2	200*1 100*2	μA	$\overline{CE}$ ≥ V_{CC} -0.2V $\overline{OE}/\overline{RFSH}$ ≤ 0.2V V_{IH}, V_{IN} ≥ 0V
Input Leakage Current	I_{LI}	-10	—	10	μA	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	I_{LO}	-10	—	10	μA	$\overline{OE}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}
Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	—	—	V	I_{OH} = -1 mA

NOTES: 1. Only for L-Version.
2. Only for LL/LV-Version.

■ CAPACITANCE

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Input Capacitance	C_{in}	—	8	pF	V_{in} = 0V
Input/Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0V

NOTE: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Test Conditions

Input pulse levels: 2.4V, 0.4V
Input rise and fall times: 5 ns
Timing measurement level: 2.2V, 0.8V
Reference level: V_{OH} = 2.0V, V_{OL} = 0.8V
Output load: 1 TTL and 100 pF

T-46-23-25

■ AC CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Item	Symbol	HM658512-8		HM658512-10		HM658512-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	130	—	160	—	190	—	ns	
Chip Enable Access Time	t_{CEA}	—	80	—	100	—	120	ns	
Read-Modify-Write Cycle Time	t_{RWC}	180	—	220	—	260	—	ns	
Output Enable Access Time	t_{OEA}	—	30	—	40	—	50	ns	
Chip Disable to Output in High-Z	t_{CHZ}	0	25	0	25	0	30	ns	1
Chip Enable to Output in Low-Z	t_{CLZ}	20	—	20	—	20	—	ns	2
Output Disable to Output in High-Z	t_{OHZ}	—	25	—	25	—	30	ns	1
Output Enable to Output in Low-Z	t_{OLZ}	0	—	0	—	0	—	ns	2
Chip Enable Pulse Width	t_{CE}	80 ns	10 μs	100 ns	10 μs	120 ns	10 μs		
Chip Enable Pre-Charge Time	t_P	40	—	50	—	60	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	
Address Hold Time	t_{AH}	20	—	25	—	30	—	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	
Write Command Pulse Width	t_{WP}	25	—	30	—	35	—	ns	
Chip Enable to End of Write	t_{CW}	80	—	100	—	120	—	ns	
Chip Enable to Output Enable Delay Time	t_{OCD}	0	—	0	—	0	—	ns	
Output Enaole Hold Time	t_{OHC}	15	—	15	—	15	—	ns	
Data in to End of Write	t_{DW}	20	—	25	—	30	—	ns	
Data in Hold Time for Write	t_{DH}	0	—	0	—	0	—	ns	
Output Active From End of Write	t_{OW}	5	—	5	—	5	—	ns	2
Write to Output in High-Z	t_{WHZ}	—	20	—	25	—	30	ns	1
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
Refresh Command Delay Time	t_{RFD}	40	—	50	—	60	—	ns	
Refresh Precharge Time	t_{FP}	40	—	40	—	40	—	ns	
Refresh Command Pulse Width for Automatic Refresh	t_{FAP}	80 ns	8 μs	80 ns	8 μs	80 ns	8 μs		
Automatic Refresh Cycle Time	t_{FC}	130	—	160	—	190	—	ns	
Refresh Command Pulse Width for Self Refresh	t_{FAS}	8	—	8	—	8	—	μs	
Refresh Reset Time From Self Refresh	t_{RFS}	600	—	600	—	600	—	ns	
Refresh Period	t_{REF}	—	32	—	32	—	32	ms	2048 cycle

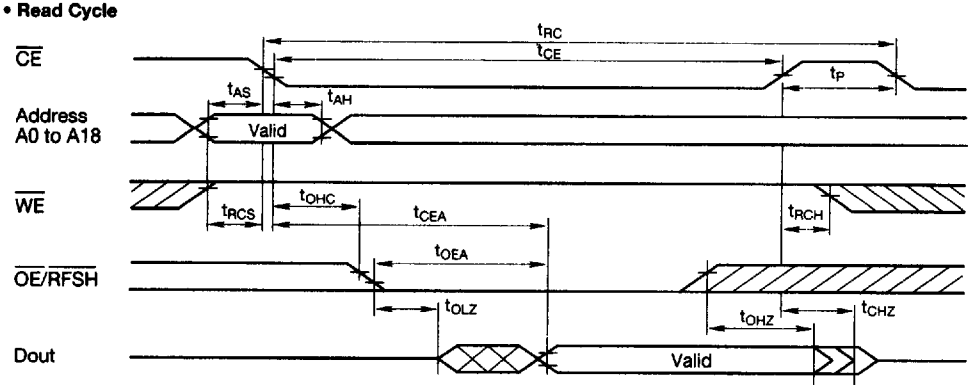
NOTES:
1. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit condition.
2. t_{CLZ}, t_{OLZ} and t_{OW} are sampled under the condition of t_T = 5 ns and not 100% tested.
3. A write occurs during the overlap of low $\overline{CE}$ and low $\overline{WE}$.
4. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition, the output buffers remain in high impedance state.
5. In write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and at the end of write cycle data inputs must be floated prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.
6. Transition time t_T is measured between V_{IH} (min.) and V_{IL} (max.).
7. After power-up, pause for more than 100 μs and execute at least 8 initialization cycles, preferably as 8 refresh cycles.
8. 2048 cycles of burst refresh or distributed automatic refresh must be executed within 15 μs after self refresh, in order to meet the refresh specification of 32 ms and 2048 cycle.

SEE ORDER OF DATA **NOTICE** FOR ERRATA INFORMATION

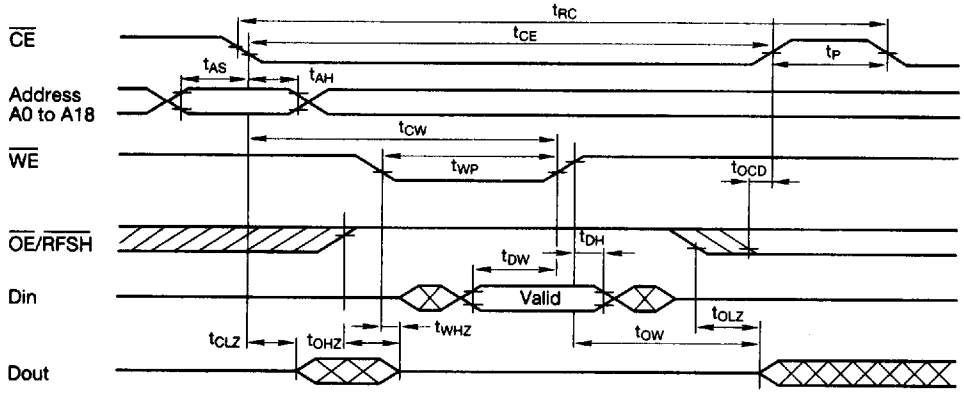
4

■ TIMING WAVEFORMS

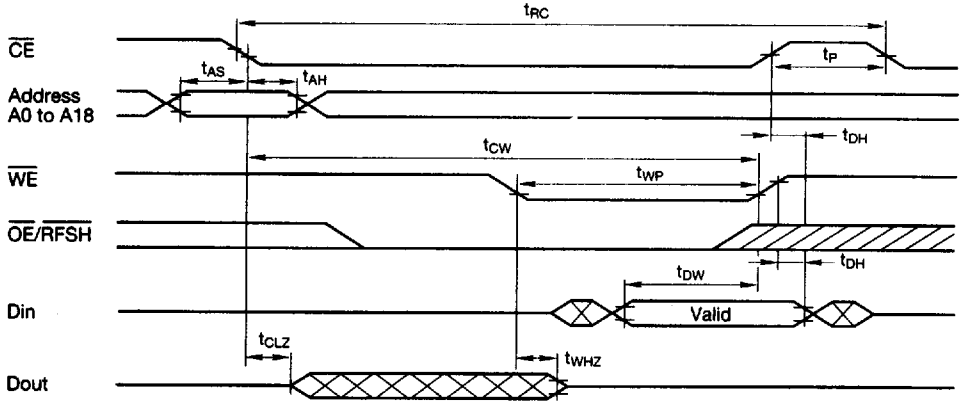
• Read Cycle



• Write Cycle (1) ($\overline{OE}$ High)



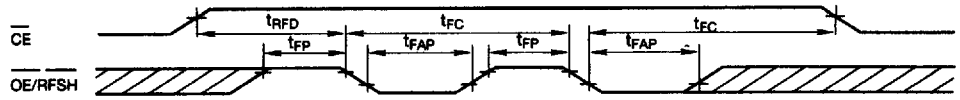
• Write Cycle (2) ($\overline{OE}$ Low)



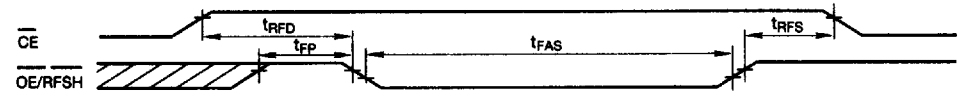
Not Valid

T-46-23-25

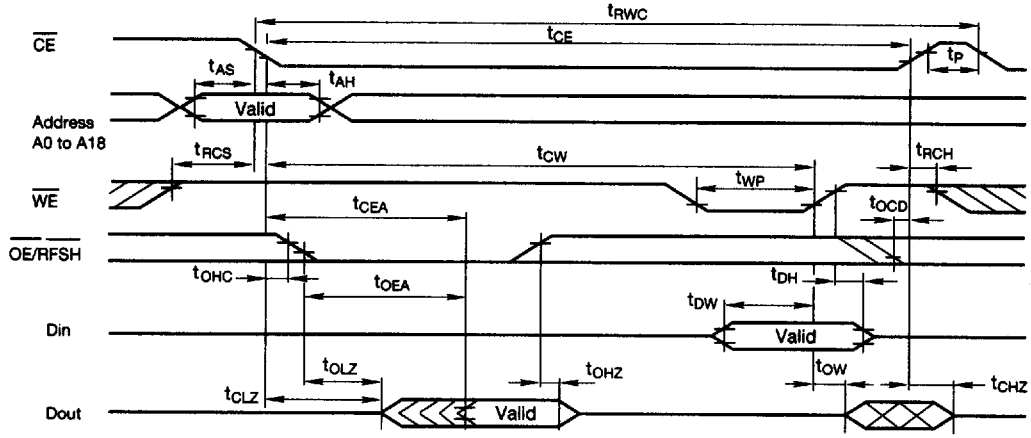
• **Automatic Refresh Cycle**



• **Self Refresh Cycle**



• **Read-Modify-Write Cycle**

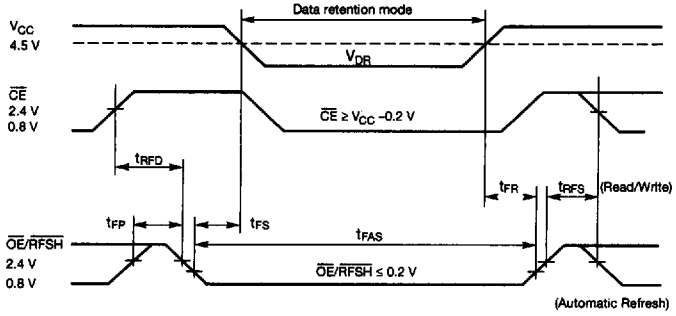


• **Low V_{CC} Data Retention Characteristics** Ta = 0 to 70°C. This characteristic is guaranteed only for LV-version.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
V_{CC} for data retention	V_{DR}	4.0	—	5.5	V	
Self refresh current	I_{CCDR}			50	μA	V_{CC}=4.0 V $\overline{CE} \geq V_{CC}$ -0.2 V $\overline{OE/RFSH} \leq 0.2$ V $V_{in} \geq 0$ V
				100	μA	V_{CC} = 5.5 V $\overline{CE} \geq V_{CC}$ -0.2 V $\overline{OE/RFSH} \leq 0.2$ V $V_{in} \geq 0$ V
Refresh setup time	t_{FS}	0			ns	
Operation recovery time	t_{FR}	5			ms	

4

• **Low V_{CC} Data Retention Timing Waveform**



Notes: 1. t_R (rise time), t_F (fall time) of power supply voltage must be smaller than 0.05 V/ms.
2. Keep $\overline{CE} \geq V_{CC}$ -0.2 V during data retention mode.
3. Regarding t_{RFD}, t_{FP}, t_{FAS} and t_{RFS}, refer to AC characteristics.