# 54F/74F378

## Parallel D Register With Enable

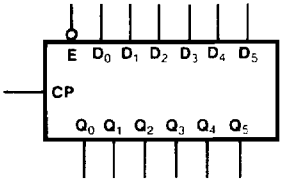
### Description

The 'F378 is a 6-bit register with a buffered common Enable. This device is similar to the 'F174, but with common Enable rather than common Master Reset.

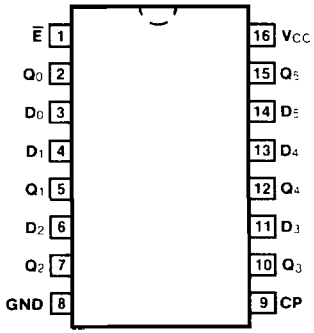
- **6-Bit High-Speed Parallel Register**
- **Positive Edge-Triggered D-Type Inputs**
- **Fully Buffered Common Clock and Enable Inputs**
- **Input Clamp Diodes Limit High-Speed Termination Effects**
- **Full TTL and CMOS Compatible**

**Ordering Code:** See Section 5

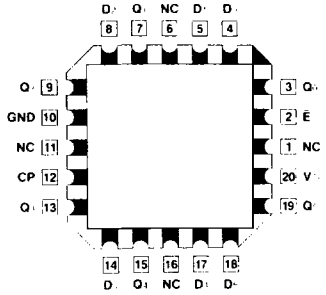
### Logic Symbol




### Connection Diagrams




**Pin Assignment for DIP and SOIC**




**Pin Assignment for LCC and PCC**

**Input Loading/Fan-Out:** See Section 3 for U.L. definitions

| Pin Names | Description | 54F/74F(U.L.) HIGH/LOW |
|---|---|---|
| $\overline{E}$ | Enable Input (Active LOW) | 0.5/0.375 |
| $D_0$-$D_5$ | Data Inputs | 0.5/0.375 |
| CP | Clock Pulse Input (Active Rising Edge) | 0.5/0.375 |
| $Q_0$-$Q_5$ | Outputs | 25/12.5 |

## Functional Description

The 'F378 consists of six edge-triggered D-type flip-flops with individual D inputs and Q inputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops.

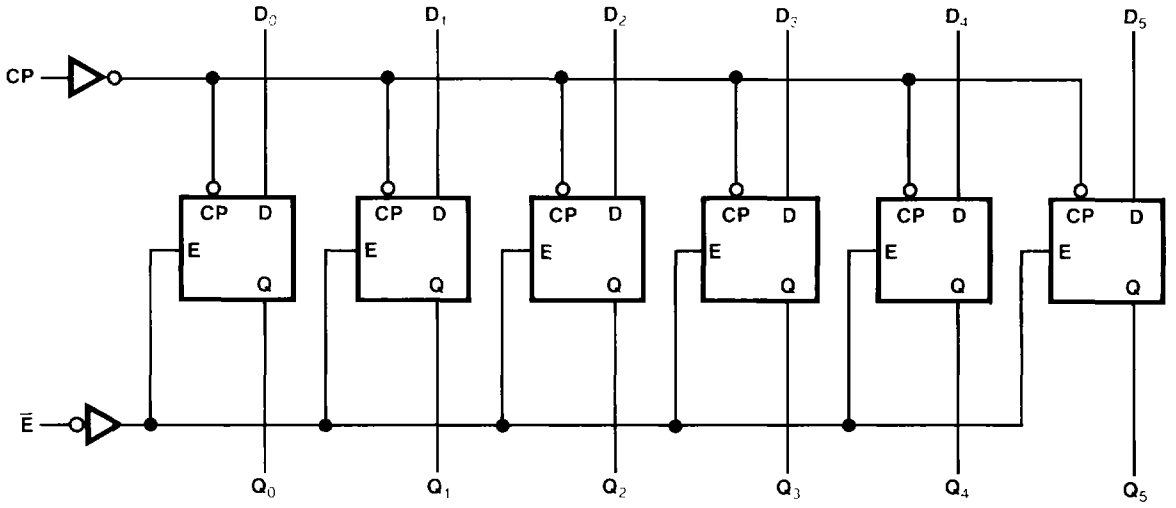
When the $\overline{E}$ input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the $\overline{E}$ input is HIGH the register will retain the present data independent of the CP input.

## Truth Table

| Inputs | | | Output |
|---|---|---|---|
| $\overline{E}$ | CP | $D_n$ | $Q_n$ |
| H | ⎍ | X | No Change |
| L | ⎍ | H | H |
| L | ⎍ | L | L |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

## Logic Diagram




Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## DC Characteristics over Operating Temperature Range (unless otherwise specified)

| Symbol | Parameter | 54F/74F | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| $I_{CC}$ | Power Supply Current | | 30 | 45 | mA | $V_{CC}$ = Max, $V_{CP}$ = 0 |

**AC Characteristics:** See Section 3 for waveforms and load configurations

| Symbol | Parameter | 54F/74F | | | 54F | | 74F | | Units | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $T_A = +25°C$, $V_{CC} = +5.0\ V$, $C_L = 50\ pF$ | | | $T_A$, $V_{CC}$ = Mil, $C_L = 50\ pF$ | | $T_A$, $V_{CC}$ = Com, $C_L = 50\ pF$ | | | |
| | | Min | Typ | Max | Min | Max | Min | Max | | |
| $f_{max}$ | Maximum Input Frequency | 80 | 100 | | 70 | | 80 | | MHz | 3-1 |
| $t_{PLH}$ | Propagation Delay | 3.0 | 5.5 | 7.5 | 3.0 | 10.0 | 3.0 | 8.5 | ns | 3-1 |
| $t_{PHL}$ | CP to $Q_n$ | 3.5 | 6.0 | 8.5 | 3.5 | 10.5 | 3.5 | 9.5 | | 3-7 |

**AC Operating Requirements:** See Section 3 for waveforms

| Symbol | Parameter | 54F/74F | | | 54F | | 74F | | Units | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $T_A = +25°C$, $V_{CC} = +5.0\ V$ | | | $T_A$, $V_{CC}$ = Mil | | $T_A$, $V_{CC}$ = Com | | | |
| | | Min | Typ | Max | Min | Max | Min | Max | | |
| $t_s(H)$ | Setup Time, HIGH or LOW | 4.0 | | | 5.0 | | 4.0 | | ns | 3-5 |
| $t_s(L)$ | $D_n$ to CP | 4.0 | | | 5.0 | | 4.0 | | | |
| $t_h(H)$ | Hold Time, HIGH or LOW | 0 | | | 2.0 | | 0 | | ns | 3-5 |
| $t_h(L)$ | $D_n$ to CP | 0 | | | 2.0 | | 0 | | | |
| $t_s(H)$ | Setup Time, HIGH or LOW | 4.0 | | | 4.5 | | 4.0 | | ns | 3-5 |
| $t_s(L)$ | $\overline{E}$ to CP | 10.0 | | | 13.0 | | 10.0 | | | |
| $t_h(H)$ | Hold Time, HIGH or LOW | 0 | | | 0 | | 0 | | ns | 3-5 |
| $t_h(L)$ | $\overline{E}$ to CP | 0 | | | 0 | | 0 | | | |
| $t_w(H)$ | CP Pulse Width | 4.0 | | | 5.0 | | 4.0 | | ns | 3-7 |
| $t_w(L)$ | HIGH or LOW | 6.0 | | | 7.5 | | 6.0 | | | |