

# SONY CXK584000TM/YM/M/P -55L/70L/85L/10L -55LL/70LL/85LL/10LL

524288-word × 8-bit High Speed CMOS Static RAM

*Preliminary*

## Description

CXK584000TM/YM/M/P is a 4,194,304 bits high speed CMOS static RAM organized as 524,288 words by 8-bits. Polysilicon TFT cell technology realized extremely low stand-by current and higher data retention stability. Operating on a single 2.7 to 5.5V supply, this asynchronous IC is suitable for high speed and low power consumption applications where battery back up for nonvolatility is required.

## Features

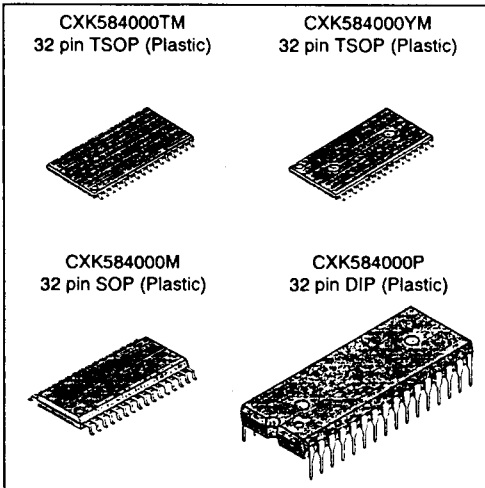
- Wide supply voltage range: 2.7 to 5.5V
- Fast access time: 5V operation/3V operation
 

-55L/55LL	55ns/110ns (Max.)
-70L/70LL	70ns/140ns (Max.)
-85L/85LL	85ns/170ns (Max.)
-10L/10LL	100ns/200ns (Max.)
- Low stand-by current:
 

-55L/70L/85L/10L	100 μA (Max.)
-55LL/70LL/85LL/10LL	50 μA (Max.)
- Low data retention current:
 

-55L/70L/85L/10L	15 μA (Max.) Ta=0 to +40 °C
-55LL/70LL/85LL/10LL	3 μA (Max.) Ta=0 to +40 °C
- Low voltage data retention: 2.0V (Min.)
- Package line-up
 

CXK584000TM/YM	400mil 32 pin TSOP (Type II)
CXK584000M	525mil 32 pin SOP
CXK584000P	600mil 32 pin DIP



## Function

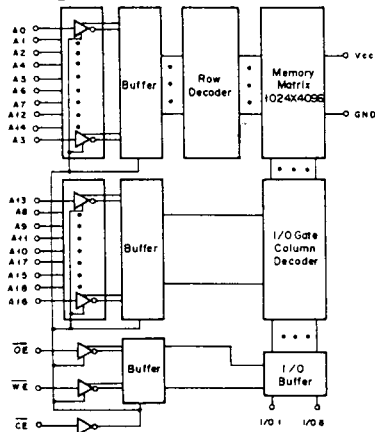
524288-word × 8-bit static RAM

## Structure

Silicon gate CMOS IC

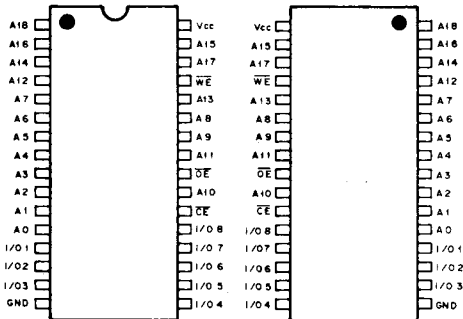
**5**

## Block Diagram



**Pin Configuration**

(Top View)



CXK584000TM  
CXK584000M  
CXK584000P

CXK584000YM

**Pin Description**

Symbol	Description
A0 to A18	Address input
I/O1 to I/O8	Data input/output
CE	Chip enable input
WE	Write enable input
OE	Output enable input
Vcc	Power supply
GND	Ground

**Absolute Maximum Ratings**

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	-0.5 to +7.0	V
Input voltage	V <sub>IN</sub>	-0.5 * to Vcc+0.5	V
Input and output voltage	V <sub>I/O</sub>	-0.5 * to Vcc+0.5	V
Allowable power dissipation	P <sub>d</sub>	CXK584000TM/YM/M	0.7
		CXK584000P	1.0
Operating temperature	T <sub>opr</sub>	0 to +70	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C
Soldering temperature • time	T <sub>solder</sub>	CXK584000TM/YM	235 • 10
		CXK584000M/P	260 • 10

\* V<sub>IN</sub>, V<sub>I/O</sub>=-3.0V Min. for pulse width less than 50ns.

**Truth Table**

CE	OE	WE	Mode	I/O pin	Vcc current
H	x	x	Not selected	High Z	I <sub>SB1</sub> , I <sub>SB2</sub>
L	H	H	Output disable	High Z	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC3</sub>
L	L	H	Read	Data out	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC3</sub>
L	x	L	Write	Data in	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC3</sub>

x : "H" or "L"

**DC Recommended Operating Conditions**

(Ta=0 to +70 °C, GND=0V)

Item	Symbol	Vcc=5V ± 10%			Vcc=2.7 to 5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply voltage	Vcc	4.5	—	5.5	2.7	—	5.5	V
Input high voltage	V <sub>IH</sub>	2.2	—	Vcc+0.3	2.2	—	Vcc+0.3	V
Input low voltage	V <sub>IL</sub>	-0.3*	—	0.8	-0.3*	—	0.4	V

\* V<sub>IL</sub>=-3.0V Min. for pulse width less than 50ns.

**Electrical Characteristics**

**• DC characteristics**

(GND=0V, Ta=0 to +70 °C)

Item	Symbol	Test conditions	Vcc=5V ± 10%			Vcc=3V ± 10%			Unit		
			Min.	Typ. *1	Max.	Min.	Typ. *2	Max.			
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =GND to Vcc	-1	—	1	-1	—	1	μA		
Output leakage current	I <sub>LO</sub>	CE=V <sub>IH</sub> or OE=V <sub>IH</sub> or WE=V <sub>IL</sub> V <sub>IO</sub> =GND to Vcc	-1	—	1	-1	—	1	μA		
Operating power supply current	I <sub>CC1</sub>	CE=V <sub>IL</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>OUT</sub> =0mA	—	6	15	—	0.4	0.8	mA		
Average operating current	I <sub>CC2</sub>	Min. cycle Duty=100% I <sub>OUT</sub> =0mA	—	60	100	—	20	35	mA		
	I <sub>CC3</sub>	Cycle time 1 μs Duty=100% I <sub>OUT</sub> =0mA CE ≤ 0.2V, V <sub>IL</sub> ≤ 0.2V, V <sub>IH</sub> ≥ Vcc-0.2V	—	10	20	—	5	10	mA		
Standby current	I <sub>SB1</sub>	CE ≥ Vcc-0.2V	L*3	0 to +70 °C	—	—	100	—	—	74	μA
				0 to +40 °C	—	—	35	—	—	24	
				+25 °C	—	2	—	—	1	—	
			LL*4	0 to +70 °C	—	—	50	—	—	22	
				0 to +40 °C	—	—	18	—	—	4.5	
				+25 °C	—	2	—	—	0.5	—	
I <sub>SB2</sub>	CE=V <sub>IH</sub>	—	0.3	3	—	0.06	0.3	mA			
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA	2.4	—	—	2.2	—	—	V		
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	—	—	0.4	—	—	0.4	V		

\*1 Vcc=5V, Ta=25 °C

\*2 Vcc=3V, Ta=25 °C

\*3 Guaranteed for L-version (-55L/70L/85L/10L)

\*4 Guaranteed for LL-version (-55LL/70LL/85LL/10LL)

5

**I/O Capacitance**

(Ta=25°C, f=1MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	—	—	7	pF
I/O capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> =0V	—	—	8	pF

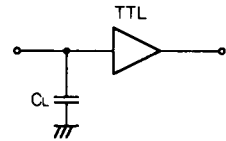
**Note)** This parameter is sampled and is not 100% tested.

**AC Characteristics**

● **AC test conditions**

(V<sub>CC</sub>=2.7 to 5.5V, Ta=0 to +70°C)

Item	Conditions		
	V <sub>CC</sub> =5V	V <sub>CC</sub> =3V	
Input pulse high level	V <sub>IH</sub> =2.2V	V <sub>IH</sub> =2.2V	
Input pulse low level	V <sub>IL</sub> =0.8V	V <sub>IL</sub> =0.4V	
Input rise time	t <sub>r</sub> =5ns	t <sub>r</sub> =5ns	
Input fall time	t <sub>f</sub> =5ns	t <sub>f</sub> =5ns	
Input and output reference level	1.5V	1.5V	
Output load conditions	-70L/70LL -85L/85LL -10L/10LL	C <sub>L</sub> * =100pF, 1TTL	C <sub>L</sub> * =100pF, 1TTL
	-55L/55LL	C <sub>L</sub> * =30pF, 1TTL	C <sub>L</sub> * =30pF, 1TTL



\* C<sub>L</sub> includes scope and jig capacitances.

## • Read cycle

(V<sub>CC</sub>=5V ± 10%, GND=0V, Ta=0 to +70 °C)

Item	Symbol	- 55L/55LL		- 70L/70LL		- 85L/85LL		- 10L/10LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t <sub>RC</sub>	55	—	70	—	85	—	100	—	ns
Address access time	t <sub>AA</sub>	—	55	—	70	—	85	—	100	ns
Chip enable access time	t <sub>CO</sub>	—	55	—	70	—	85	—	100	ns
Output enable to output valid	t <sub>OE</sub>	—	30	—	40	—	45	—	50	ns
Output hold from address change	t <sub>OH</sub>	10	—	10	—	10	—	10	—	ns
Chip enable to output in low Z ( $\overline{CE}$ )	t <sub>LZ</sub>	10	—	10	—	10	—	10	—	ns
Output enable to output in low Z ( $\overline{OE}$ )	t <sub>OLZ</sub>	5	—	5	—	5	—	5	—	ns
Chip disable to output in high Z ( $\overline{CE}$ )	t <sub>HZ</sub> *	0	20	0	25	0	30	0	35	ns
Output disable to output in high Z ( $\overline{OE}$ )	t <sub>OZH</sub> *	0	20	0	25	0	30	0	35	ns

\* t<sub>HZ</sub> and t<sub>OZH</sub> are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

## • Write cycle

(V<sub>CC</sub>=5V ± 10%, GND=0V, Ta=0 to +70 °C)

Item	Symbol	- 55L/55LL		- 70L/70LL		- 85L/85LL		- 10L/10LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t <sub>WC</sub>	55	—	70	—	85	—	100	—	ns
Address valid to end of write	t <sub>AW</sub>	50	—	60	—	70	—	80	—	ns
Chip enable to end of write	t <sub>CW</sub>	50	—	60	—	70	—	80	—	ns
Data to write time overlap	t <sub>DW</sub>	25	—	30	—	35	—	40	—	ns
Data hold from write time	t <sub>DH</sub>	0	—	0	—	0	—	0	—	ns
Write-pulse width	t <sub>WP</sub>	40	—	50	—	60	—	70	—	ns
Address setup time	t <sub>AS</sub>	0	—	0	—	0	—	0	—	ns
Write recovery time ( $\overline{WE}$ )	t <sub>WR</sub>	0	—	0	—	0	—	0	—	ns
Write recovery time (CE)	t <sub>WR1</sub>	0	—	0	—	0	—	0	—	ns
Output active from end of write	t <sub>OW</sub>	5	—	5	—	5	—	5	—	ns
Write to output in high Z	t <sub>WHZ</sub> *	0	20	0	25	0	30	0	30	ns

\* t<sub>WHZ</sub> is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

## • Read cycle

(V<sub>CC</sub>=3V ± 10%, GND=0V, T<sub>a</sub>=0 to +70 °C)

Item	Symbol	- 55L/55LL		- 70L/70LL		- 85L/85LL		- 10L/10LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t <sub>RC</sub>	110	—	140	—	170	—	200	—	ns
Address access time	t <sub>AA</sub>	—	110	—	140	—	170	—	200	ns
Chip enable access time	t <sub>CO</sub>	—	110	—	140	—	170	—	200	ns
Output enable to output valid	t <sub>OE</sub>	—	60	—	80	—	90	—	100	ns
Output hold from address change	t <sub>OH</sub>	20	—	20	—	20	—	20	—	ns
Chip enable to output in low Z ( $\overline{CE}$ )	t <sub>LZ</sub>	20	—	20	—	20	—	20	—	ns
Output enable to output in low Z ( $\overline{OE}$ )	t <sub>OLZ</sub>	10	—	10	—	10	—	10	—	ns
Chip disable to output in high Z ( $\overline{CE}$ )	t <sub>HZ</sub> *	0	40	0	50	0	60	0	70	ns
Output disable to output in high Z ( $\overline{OE}$ )	t <sub>OHZ</sub> *	0	40	0	50	0	60	0	70	ns

\* t<sub>HZ</sub> and t<sub>OHZ</sub> are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

## • Write cycle

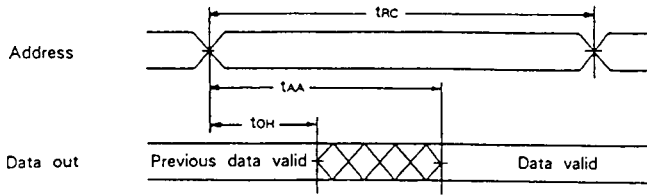
(V<sub>CC</sub>=3V ± 10%, GND=0V, T<sub>a</sub>=0 to +70 °C)

Item	Symbol	- 55L/55LL		- 70L/70LL		- 85L/85LL		- 10L/10LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t <sub>WC</sub>	110	—	140	—	170	—	200	—	ns
Address valid to end of write	t <sub>AW</sub>	100	—	120	—	140	—	160	—	ns
Chip enable to end of write	t <sub>CW</sub>	100	—	120	—	140	—	160	—	ns
Data to write time overlap	t <sub>DW</sub>	50	—	60	—	70	—	80	—	ns
Data hold from write time	t <sub>DH</sub>	0	—	0	—	0	—	0	—	ns
Write pulse width	t <sub>WP</sub>	80	—	100	—	120	—	140	—	ns
Address setup time	t <sub>AS</sub>	0	—	0	—	0	—	0	—	ns
Write recovery time (WE)	t <sub>WR</sub>	0	—	0	—	0	—	0	—	ns
Write recovery time ( $\overline{CE}$ )	t <sub>WR1</sub>	0	—	0	—	0	—	0	—	ns
Output active from end of write	t <sub>OW</sub>	10	—	10	—	10	—	10	—	ns
Write to output in high Z	t <sub>WHZ</sub> *	0	40	0	50	0	60	0	60	ns

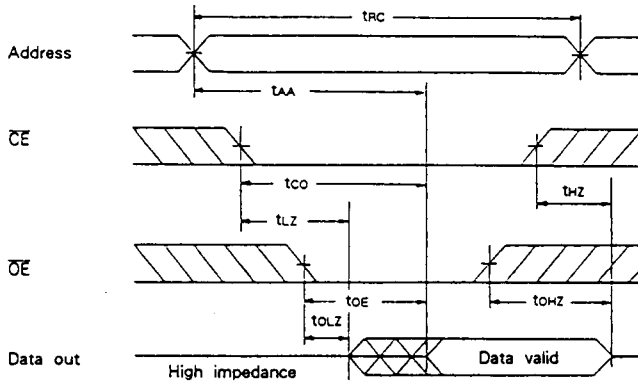
\* t<sub>WHZ</sub> is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

**Timing Waveform**

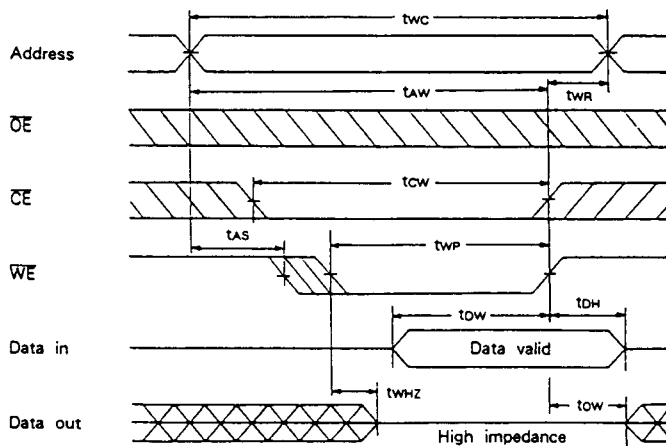
- Read cycle (1) :  $\overline{CE}=\overline{OE}=V_{IL}, \overline{WE}=V_{IH}$



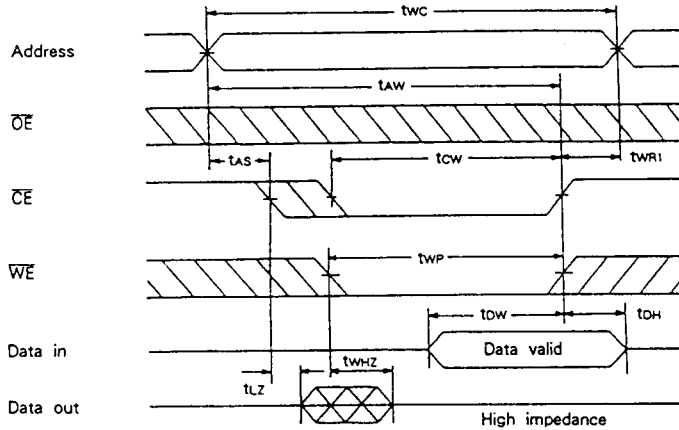
- Read cycle (2) :  $\overline{WE}=V_{IH}$



- Write cycle (1) :  $\overline{WE}$  control



• Write cycle (2) :  $\overline{CE}$  control



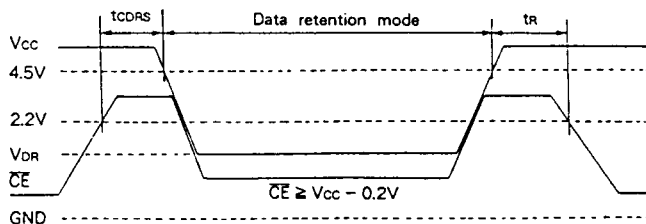
During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

**Data Retention Characteristics**

(Ta=0 to 70°C)

Item	Symbol	Test conditions	- 55L/70L/85L/10L			- 55LL/70LL/85LL/10LL			Unit	
			Min.	Typ.	Max.	Min.	Typ.	Max.		
Data retention voltage	V <sub>DR</sub>	$\overline{CE} \geq V_{CC} - 0.2V$	2.0	—	5.5	2.0	—	5.5	V	
Data retention current	I <sub>CCDR1</sub>	V <sub>CC</sub> =3.0V $\overline{CE} \geq 2.8V$	0 to 70°C	—	—	50	—	—	15	μA
			0 to 40°C	—	—	15	—	—	3	
			25°C	—	1	—	—	0.5	—	
	I <sub>CCDR2</sub>	V <sub>CC</sub> =2.0 to 5.5V $\overline{CE} \geq V_{CC} - 0.2V$	—	2	100	—	2	50	μA	
Data retention setup time	t <sub>CDRS</sub>	Chip disable to data retention mode	0	—	—	0	—	—	ns	
Recovery time	t <sub>R</sub>		5	—	—	5	—	—	ms	

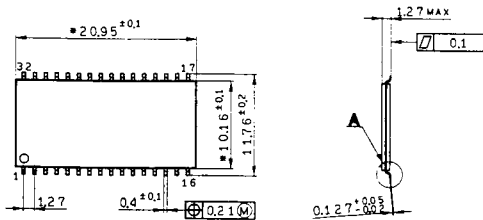
**Data retention waveform**





Package Outline Unit : mm

CXK584000TM 32pin TSOP (Plastic) 400mil

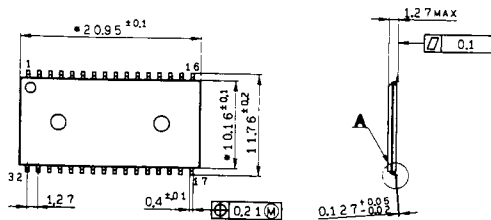


Note) Dimensions marked with \* does not include resin residue.

Detailed diagram of A.

SONY NAME	TSOP(I)-32P-L01
EIAJ NAME	TSOP(T)032-P-0400-A
JEDEC CODE	

CXK584000YM 32pin TSOP (Plastic) 400mil



Note) Dimensions marked with \* does not include resin residue.

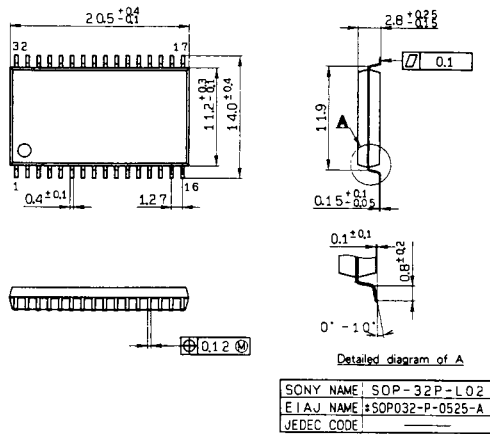
Detailed diagram of A.

SONY NAME	TSOP(I)-32P-L01P
EIAJ NAME	TSOP(I)032-P-0400-B
JEDEC CODE	

5

CXK584000M

32pin SOP (Plastic) 525mil



CXK584000P

32pin DIP (Plastic) 600mil 4.5g

