FCT PRODUCTS FOR BACKPLANE-INTERFACE APPLICATIONS

RCA FCT products are being developed to provide a reliable interface with modern high-speed backplanes. The FCT types vastly reduce power consumption, avoid bus contention difficulties, minimize switching noise, and provide outputs that are specifically tailored to interface with VME buses or their equivalent.

The speed of the FCT family is comparable to that of bipolar FAST types. Sink current ranges from 48 milliamperes to 64 milliamperes depending on product type. Fully populated buses, such as the 21-slot VME can be reliably interfaced. Products are most economically packaged in plastic DIP and gull-wing surface-mount pinouts. As with GE's AC/ACT family of logic devices, simultaneous switching transients are controlled to levels comparable to similar bipolar logic functions (1 volt peak area for octal ground bounce).

FCT products, the modern standard for backplane-interface applications, meet or exceed planned JEDEC industry-standard No. 18 specifications. FCT products clearly are the low-power backplane interface needed in the rapidly growing down-sized computer world, where low operating power and virtually zero standby power are essential requirements.

The two competitive bipolar families, FAST and the proposed BCT line as described in the technical press, compared with FCT products are 300 to 1000 times higher in quiescent power consumption and 400 to 850 times higher in operating power consumption at a continuous five megahertz operation. This comparison is illustrated in Fig. 79.

The ratio of sink-to-source current and the absence of diodes clamped to the supply rail at the I/O ports eliminate or minimize bus contention and permit low power-down mode operation.

Table XVIII lists types and type numbers now in planning.

FCT Features

Speed	Competitive with similar bipolar F/AS TTL functions. Typical delay is 3.5 nanoseconds.
Sink/Source Current	All types have sink and source currents meeting VME, multibus, etc standards. Output edges are monotonic through the TTL switch point with fully populated backplanes.
Simultaneous Switching Transients	(Ground bounce) Competitive with similar bipolar TTL and CMOS products. Output swing is 3.5 volts. Output edges are slewed.
Operating and Standby Power	Ultra-low pure CMOS operating power and standby power of almost zero.
Pinout	Standard.

FCT Benefits

Swift delay requirements dictated by modern control-system backplane-interface logic present no problems.

Optimized output drives minimize backplane reflections in worst-case situations.

EMI and RFI emissions minimized. Good signal-pulse integrity.

Meets low-power needs of down-sized computers without fans, etc. Low battery drain.

Provided in minimum and most economically sized DIP and SOP.

Minimum CAD/CAM, burn-in board, and PC-board real-estate costs. With no performance sacrifice.

Table XVIII - Planned FCT Types

Buffers			
CD54/74FCT240	CD54/74FCT241	CD54/74FCT244	CD54/74FCT540
CD54/74FCT541	CD54/74FCT827	CD54/74FCT828	
Transceivers			
CD54/74FCT245	CD54/74FCT623	CD54/74FCT646	CD54/74FCT648
CD54/74FCT651	CD54/74FCT652	CD54/74FCT861	CD54/74FCT862
CD54/74FCT863	CD54/74FCT864	CD54/74FCT7623	
Latches			
CD54/74FCT373	CD54/74FCT533	CD54/74FCT563	CD54/74FCT573
CD54/74FCT841	CD54/74FCT842	CD54/74FCT843	CD54/74FCT844
Registers			
CD54/74FCT821	CD54/74FCT822	CD54/74FCT823	CD54/74FCT824
Flip-Flops			
CD54/74FCT273	CD54/74FCT374	CD54/74FCT534	CD54/74FCT564
CD54/74FCT574			

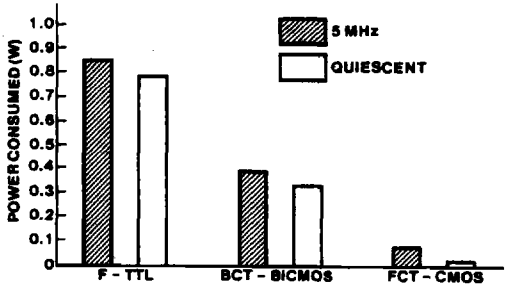


Fig. 79 - Comparison of power consumption for an octal transceiver type.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V) ..... -20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V) ..... -50 mA
DC OUTPUT SINK CURRENT per Output Pin, I_O ..... +70 mA
DC OUTPUT SOURCE CURRENT per Output Pin, I_O ..... -30 mA
DC V_{CC} CURRENT (I_{CC}) ..... 140 mA
DC GROUND CURRENT (I_{GND}) ..... N (I_{OL}) + M (ΔI_{CC})
where N = No. of outputs
M = No. of inputs

POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE E, M ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*:			
T_A = 0 to 70°C	4.75	5.25	V
T_A = -55 to + 125°C	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

STATIC ELECTRICAL CHARACTERISTICS
FCT Series:

74FCT Commercial Temperature Range, 0 to 70°C. V_{CC} max = 5.25 V, V_{CC} min = 4.75 V

54FCT Extended Industrial Temperature Range, -55 to +125°C. V_{CC} max = 5.5 V, V_{CC} min = 4.5 V

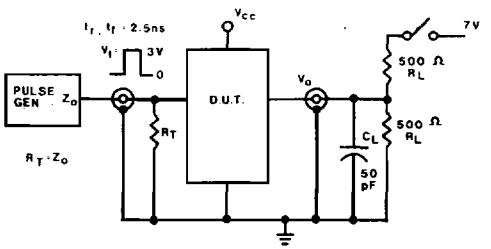
CHARACTERISTICS		TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C: +25 MIN.	+25 MAX.	0 to +70 MIN.	0 to +70 MAX.	-55 to +125 MIN.	-55 to +125 MAX.	UNITS
High-Level Input Voltage	V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15#	MIN.	2.4	—	2.4	—	—	—	V
			-12#		2.4	—	—	—	2.4	—	
Low-Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	64#	MIN.	—	0.55	—	0.55	—	—	
			48#		—	0.55	—	—	—	0.55	
High-Level Input Current	I_{IH}	V_{CC}		MAX.	—	0.1	—	1	—	1	μA
Low-Level Input Current	I_{IL}	GND		MAX.	—	-0.1	—	-1	—	-1	μA
3-State Leakage Current	I_{OZH}	V_{CC}		MAX.	—	0.5	—	10	—	10	μA
	I_{OZL}	GND		MAX.	—	-0.5	—	-10	—	-10	
Short-Circuit Output Current*	I_{OS}	V_{CC} or GND V_O = 0		MAX.	-60#	—	-60#	—	-60#	—	mA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	MIN.	—	-1.2	—	-1.2	—	-1.2	V
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	MAX.	—	8	—	80	—	500	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI_{CC}	3.4 V†		MAX.	—	1.6	—	1.6	—	2	mA

*Not more than one output should be shorted at one time. Test duration should not exceed 100 ms.
†Inputs that are not measured are at V_{CC} or Gnd.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6 mA max. @ 70°C.
#Values are for FCT240 types (see "Output Capabilities" and Table XIX for I_{OS}, I_{OL}, and I_{OH} for other types.)

SWITCHING WAVEFORMS FOR 54/74FCTXXX

Shown below is the FCT test circuit. A Thevenin equivalent may be used for output loading.



TEST	SWITCH POSITION
t_{PLZ} t_{PZL} OPEN DRAIN	CLOSED
t_{PHZ} t_{PZH} t_{PLH} t_{PHL}	OPEN

Definitions:

C_L = Load capacitance includes jig and probe capacitance.
R_T = Termination should be equal to Z_{OUT} of the pulse generator. (Typically 50 Ω).
V_{IN} = 0 V to 3 V
Input: $t_r = t_f$ = 2.5 ns (10% to 90%) unless otherwise specified.

Fig. 80 - Test circuit.

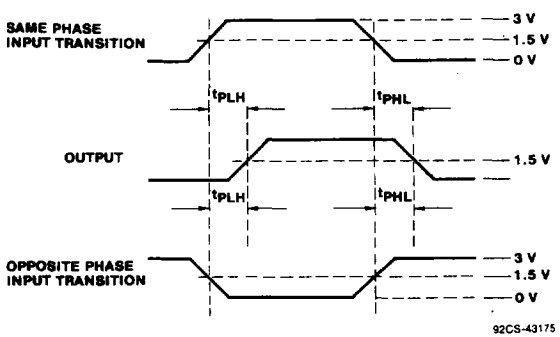
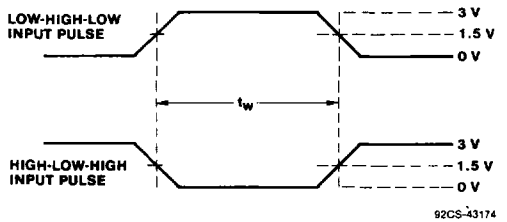


Fig. 81 - Propagation delay times.



Output Requirement:

Device must follow truth table.
$V_{OL} \leq 0.55$ V
$V_{OH} \geq 2.4$ V

Input Condition:

$t_r = t_f \leq 2.5$ ns (as fast as required)

Standard Output Loading:

R_L = 500 Ω
C_L = 50 pF

Fig. 82 - Input pulse width.

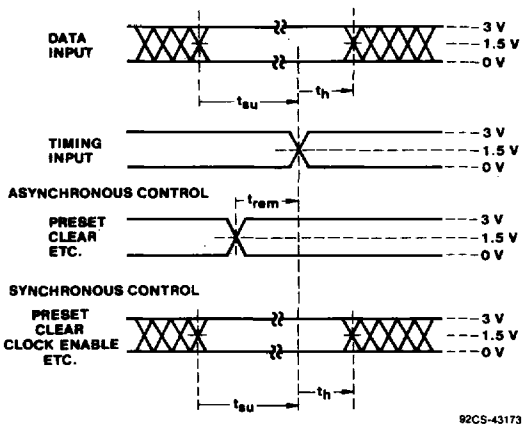


Fig. 83 - Setup, hold, and removal times.

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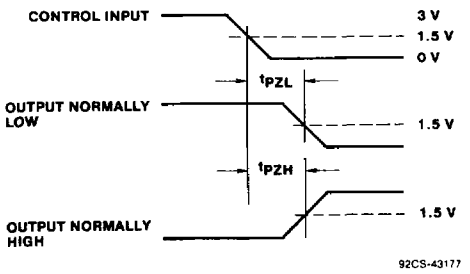
SWITCHING WAVEFORMS FOR 54/74FCTXXX (CONT'D)

ENABLE TIMES



DISABLE TIMES

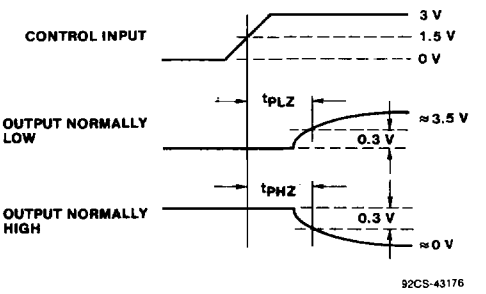


Fig. 84 - Output enable and disable times.

OUTPUT CAPABILITIES

Because of the numerous applications for 54/74FCT types, the output specifications are derived from the LOW drive and HIGH drive tables below. Any I_{OL} type category may be combined with any I_{OH} and I_{OS} type category to specify the output drive. Refer to Table XIX for device type categories.

Minimum Output at Low Drive (I_{OL}); V_{CC} = min

Type Category	Low-Level Output Voltage V_{OL} (V)	Minimum Low-Level Output Current I_{OL} (mA)	
		COM'L	MIL
3	0.55	48	32
4	0.55	64	48

Minimum Output at High Drive (I_{OH}); V_{CC} = min

Type Category	High-Level Output Voltage V_{OH} (V)	Minimum High-Level Output Current I_{OH} (mA)	
		COM'L	MIL
1	2.4	-15	-12
2	2.4	-24	-20

Minimum Output at Short Circuit (I_{OS}); V_{CC} = max

Type Category	Output Voltage V_O (V)	Minimum Short-Circuit Output Current I_{OS} (mA)	
		COM'L	MIL
1	0.0	-60	-60
2	0.0	-75	-75

Table XIX - Output Drive for 54/74FCTXXX

Device Number	I_{OH} Output Type	I_{OL} Output Type
54/74FCT240	1	4
54/74FCT241	1	4
54/74FCT244	1	4
54/74FCT245	1	4
54/74FCT273	1	3
54/74FCT373	1	3
54/74FCT374	1	3
54/74FCT533	1	3
54/74FCT534	1	3
54/74FCT540	1	4
54/74FCT541	1	4
54/74FCT563	1	3
54/74FCT564	1	3
54/74FCT573	1	3
54/74FCT574	1	3
54/74FCT623/7623	1	4
54/74FCT646	1	4
54/74FCT648	1	4
54/74FCT651	1	4
54/74FCT652	1	4
54/74FCT821	2	3
54/74FCT822	2	3
54/74FCT823	2	3
54/74FCT824	2	3
54/74FCT827	2	3
54/74FCT828	2	3
54/74FCT842	2	3
54/74FCT843	2	3
54/74FCT844	2	3
54/74FCT861	2	3
54/74FCT862	2	3
54/74FCT863	2	3
54/74FCT864	2	3

PRELIMINARY SWITCHING-SPEED LIMITS

This section gives the preliminary switching-speed parameter limits for the FCT types. The limits are given for each type grouped by generic function. Table XX covers bus drivers, buffers, and transceivers. Table XXI covers flip-flops and registers. Table XXII covers latches, and Table XXIII covers all types that additionally have three-state operation capability.

In the tables, individual parameter limits are given for each device type along with descriptive symbols for each parameter. All limit values are in nanoseconds. Generic pin names are used and no distinctions are made for inverting or non-inverting outputs unless noted.

For each entry two limit values are shown separated by a slash, e.g. a/b. Limit a applies to the commercial temperature range 0 to 70°C with V_{CC} = 5.0 ± 0.25 volts. Limit b applies to the MIL temperature range of -55°C to +125°C with V_{CC} = 5.0 ± 0.5 volts. Plastic DIP and SOP packaged parts (74 series) are applicable for both temperature ranges. The 54 series devices will apply only to the MIL ceramic packaged parts when available. A dash (—) indicates that the parameter is not specified or does not exist for a given device.

It should be noted that these preliminary speed limits are design objectives and are subject to possible minor changes.

Table XX - Switching Parameters for Bus Drivers, Buffers, and Transceivers.

Type Number	Descriptive Symbol	COM'L/MIL Limits (ns)
CD54/74FCT240	t_{PLH}, t_{PHL} $A_n \rightarrow Y_n$	8.0/9.0
CD54/74FCT241	t_{PLH}, t_{PHL} $A_n \rightarrow Y_n$	6.5/7.0
CD54/74FCT244	t_{PLH}, t_{PHL} $A_n \rightarrow Y_n$	6.5/7.0
CD54/74FCT245	t_{PLH}, t_{PHL} $A_n \rightarrow Y_n$	7.0/7.5
CD54/74FCT540	t_{PLH}, t_{PHL} $A_n \rightarrow Y_n$	8.0/9.0
CD54/74FCT541	t_{PLH}, t_{PHL} $A_n \rightarrow Y_n$	6.5/7.0
CD54/74FCT623	t_{PLH}, t_{PHL} $A_n/B_n \rightarrow Y_n$	7.0/7.5
	t_{PZH}, t_{PZL} $G, \overline{G} \rightarrow O$	9.5/10.0
	t_{PHZ}, t_{PLZ} $G, \overline{G} \rightarrow O$	7.5/10.0
CD54/74FCT646	t_{PLH}, t_{PHL} BUS→Bus	9.0/11.0
	t_{PLH}, t_{PHL} CL→Bus	9.0/10.0
	t_{PLH}, t_{PHL} Sel→Bus	11.0/12.0
	t_{PZH}, t_{PZL} $\overline{G}$/DIR→Bus	14.0/15.0
	t_{PHZ}, t_{PLZ} $\overline{G}$/DIR→Bus	9.0/11.0
	t_{su}	4.0/4.5
	t_h	2.0/2.0
	t_{pw}	6.0/6.0
CD54/74FCT648	t_{PLH}, t_{PHL} BUS→Bus	8.0/9.0
	t_{PLH}, t_{PHL} CL→Bus	9.0/10.0
	t_{PLH}, t_{PHL} Sel→Bus	11.0/12.0
CD54/74FCT648 (cont'd)	t_{PZH}, t_{PZL} $\overline{G}$/DIR→Bus	15.0/18.0
	t_{PHZ}, t_{PLZ} $\overline{G}$/DIR→Bus	9.0/11.0
	t_{su}	4.0/4.5
	t_h	2.0/2.0
	t_{pw}	6.0/6.0
CD54/74FCT651	t_{PLH}, t_{PHL} BUS→Bus	9.0/10.0
	t_{PLH}, t_{PHL} CL→Bus	9.0/11.0
	t_{PLH}, t_{PHL} Sel→Bus	11.0/12.0
	t_{PZH}, t_{PZL} $\overline{G}$/DIR→Bus	14.0/13.0
	t_{PHZ}, t_{PLZ} $\overline{G}$/DIR→Bus	9.0/11.0
	t_{su}	4.0/4.5
	t_h	2.0/2.0
	t_{pw}	6.0/6.0
CD54/74FCT652	t_{PLH}, t_{PHL} BUS→Bus	9.0/10.0
	t_{PLH}, t_{PHL} CL→Bus	9.0/11.0
	t_{PLH}, t_{PHL} Sel→Bus	11.0/12.0
	t_{PZH}, t_{PZL} $\overline{G}$/DIR→Bus	14.0/13.0
	t_{PHZ}, t_{PLZ} $\overline{G}$/DIR→Bus	9.0/11.0
	t_{su}	4.0/4.5
	t_h	2.0/2.0
	t_{pw}	6.0/6.0
CD54/74FCT827	t_{PLH}, t_{PHL} $A_n \rightarrow Y_n$	10.0/12.0

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Table XX - Switching Parameters for Bus Drivers, Buffers, and Transceivers (Cont'd)

Type Number	Descriptive Symbol	COM'L/MIL Limits (ns)
CD54/74FCT827 (cont'd)	t_{PLZ},t_{PHZ} G→O	13.0/15.0
	t_{PZL},t_{PZH} G→O	13.0/15.0
CD54/74FCT828	t_{PLH},t_{PHL} A_n→Y_n	10.0/12.0
	t_{PLZ},t_{PHZ} G→O	13.0/15.0
	t_{PZL},t_{PZH} G→O	13.0/15.0
CD54/74FCT861	t_{PLH},t_{PHL} A_n→Y_n	10.0/12.0
	t_{PLZ},t_{PHZ} G→O	14.0/16.0
	t_{PZL},t_{PZH} G→O	14.0/16.0
CD54/74FCT862	t_{PLH},t_{PHL} A_n→Y_n	10.0/12.0
	t_{PLZ},t_{PHZ} G→O	14.0/16.0
CD54/74FCT862 (cont'd)	t_{PZL},t_{PZH} G→O	14.0/16.0
CD54/74FCT863	t_{PLH},t_{PHL} A_n→Y_n	10.0/12.0
	t_{PLZ},t_{PHZ} G→O	14.0/16.0
	t_{PZL},t_{PZH} G→O	14.0/16.0
CD54/74FCT864	t_{PLH},t_{PHL} A_n→Y_n	10.0/12.0
	t_{PLZ},t_{PHZ} G→O	14.0/16.0
	t_{PZL},t_{PZH} G→O	14.0/16.0
CD54/74FCT7623	t_{PLH},t_{PHL} A_n→Y_n	7.0/7.5
	t_{PLZ} B_n→Y_n	7.5/10.0
	t_{PZL} B_n→Y_n	9.5/10.0

Table XXI - Switching Parameters for Flip-Flops and Registers

Type Number	Descriptive Symbol	COM'L/MIL Limits (ns)
CD54/74FCT273	t_{PLH},t_{PHL} CK→Q	13.0/15.0
	t_{PLH},t_{PHL} R,S→Q	13.0/15.0
	t_{su} D,J,K→CK	3.0/3.5
	t_h CK→D,J,K	2.5/2.5
	t_{rem} R,S→CK	4.0/5.0
	t_w(CK)	7.0/7.0
	t_w(R,S)	7.0/7.0
CD54/74FCT374	t_{PLH},t_{PHL} CK→Q	10.0/11.0
	t_{su} D,J,K→CK	2.0/2.5
	t_h CK→D,J,K	2.0/2.5
	t_w(CK)	7.0/7.0
CD54/74FCT534	t_{PLH},t_{PHL} CK→Q	10.0/11.0
	t_{su} D,J,K→CK	2.0/2.5
CD54/74FCT534 (cont'd)	t_h CK→D,J,K	2.0/2.5
	t_w(CK)	7.0/7.5
	t_{su} CE→CK	—
	t_h CE→CK	—
CD54/74FCT564	t_{PLH},t_{PHL} CK→Q	10.0/11.0
	t_{su} D,J,K→CK	2.0/2.5
	t_h CK→D,J,K	2.0/2.5
	t_w(CK)	7.0/7.5
	t_{su} CE→CK	—
	t_h CE→CK	—
CD54/74FCT574	t_{PLH},t_{PHL} CK→Q,Q	10.0/11.0
	t_{su} D,J,K→CK	2.0/2.5
	t_h CK→D,J,K	2.0/2.5

Table XXI - Switching Parameters for Flip-Flops and Registers (Cont'd)

Type Number	Descriptive Symbol	COM'L/MIL Limits (ns)
CD54/74FCT574 (cont'd)	t_w(CK)	7.0/7.0
	t_{PLZ},t_{PHZ} G→O	8.0/8.0
	t_{PZL},t_{PZH} G→O	12.5/14.0
CD54/74FCT821	t_{PLH},t_{PHL} CK→Q,Q	12.0/14.0
	t_{su} D,J,K→CK	4.0/6.0
	t_h CK→D,J,K	2.0/3.0
	t_w(CK)	7.0/11.0
	t_{PLZ},t_{PHZ} G→O	12.0/14.0
	t_{PZL},t_{PZH} G→O	12.0/14.0
CD54/74FCT822	t_{PLH},t_{PHL} CK→Q,Q	12.0/14.0
	t_{su} D,J,K→CK	4.0/6.0
	t_h CK→D,J,K	2.0/3.0
	t_w(CK)	7.0/11.0
	t_{PLZ},t_{PHZ} G→O	12.0/12.0
	t_{PZL},t_{PZH} G→O	12.0/14.0
CD54/74FCT823	t_{PLH},t_{PHL} CK→Q,Q	12.0/14.0
	t_{PLH},t_{PHL} R,S→Q,Q	13.0/15.0
	t_{su} D,J,K→CK	4.0/6.0

Type Number	Descriptive Symbol	COM'L/MIL Limits (ns)
CD54/74FCT823 (cont'd)	t_h CK→D,J,K	2.0/3.0
	t_{rem} R,S→CK	7.0/7.0
	t_w(CK)	7.0/11.0
	t_w(R,S)	7.0/11.0
	t_{su} CE→CK	4.0/6.0
	t_h CE→CK	2.0/3.0
	t_{PLZ},t_{PHZ} G→O	12.0/12.0
	t_{PZL},t_{PZH} G→O	12.0/14.0
CD54/74FCT824	t_{PLH},t_{PHL} CK→Q,Q	12.0/14.0
	t_{PLH},t_{PHL} R,S→Q,Q	13.0/15.0
	t_{su} D,J,K→CK	4.0/6.0
	t_h CK→D,J,K	2.0/3.0
	t_{rem} R,S→CK	7.0/7.0
	t_w(CK)	7.0/11.0
	t_w(R,S)	7.0/11.0
	t_{su} CE→CK	4.0/6.0
	t_h CE→CK	2.0/3.0
	t_{PLZ},t_{PHZ} G→O	12.0/12.0
	t_{PZL},t_{PZH} G→O	12.0/14.0

Table XXII - Switching Parameters for Latches

Type Number	Descriptive Symbol	COM'L/MIL Limits (ns)
CD54/74FCT373	t_{PLH},t_{PHL} D→Q	8.0/8.5
	t_{PLH},t_{PHL} E→Q	13.0/15.0
	t_{su} D→E	2.0/2.0
	t_h E→D	3.0/3.0
	t_w (E)	6.0/6.0

Type Number	Descriptive Symbol	COM'L/MIL Limits (ns)
CD54/74FCT533	t_{PLH},t_{PHL} D→Q	8.0/8.5
	t_{PLH},t_{PHL} E→Q	13.0/14.0
	t_{su} D→E	2.0/2.0
	t_h E→D	3.0/3.0
	t_w (E)	6.0/6.0

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Table XXII - Switching Parameters for Latches (Cont'd)

Type Number	Descriptive Symbol	COM'L/MIL Limits (ns)
CD54/74FCT563	t_{PLH}, t_{PHL} D→Q	8.0/8.5
	t_{PLH}, t_{PHL} E→Q	13.0/14.0
	t_{su} D→E	2.0/2.0
	t_h E→D	3.0/3.0
	t_w (E)	6.0/6.0
CD54/74FCT573	t_{PLH}, t_{PHL} D→Q	8.0/8.5
	t_{PLH}, t_{PHL} E→Q	13.0/15.0
	t_{su} D→E	2.0/2.0
	t_h E→D	3.0/3.0
	t_w (E)	6.0/6.0
	t_{PLZ}, t_{PHZ} G→O	7.5/10.0
	t_{PZL}, t_{PZH} G→O	12.0/13.5
CD54/74FCT841	t_{PLH}, t_{PHL} D→Q	11.0/14.0
	t_{PLH}, t_{PHL} E→Q	12.0/14.0
	t_{su} D→E	3.0/3.0
	t_h E→D	4.0/4.0
	t_w (E)	6.0/9.0
	t_{PLZ}, t_{PHZ} G→O	12.0/14.0
	t_{PZL}, t_{PZH} G→O	12.0/14.0
CD54/74FCT842	t_{PLH}, t_{PHL} D→Q	11.0/14.0
	t_{PLH}, t_{PHL} E→Q	12.0/14.0
	t_{su} D→E	3.0/3.0
	t_h E→D	4.0/4.0
	t_w (E)	6.0/9.0
CD54/74FCT842 (cont'd)	t_{PLZ}, t_{PHZ} G→O	12.0/14.0
	t_{PZL}, t_{PZH} G→O	12.0/14.0
CD54/74FCT843	t_{PLH}, t_{PHL} D→Q	11.0/14.0
	t_{PLH}, t_{PHL} E→Q	12.0/14.0
	t_{su} D→E	3.0/3.0
	t_h E→D	4.0/4.0
	t_w	6.0/9.0
	t_{PLH}, t_{PHL} R,S→Q	13.0/15.0
	t_{su} S→E	4.0/4.0
	t_{su} R→E	3.0/3.0
	t_w R,S	8.0/12.0
	t_{PLZ}, t_{PHZ} G→O	12.0/14.0
	t_{PZL}, t_{PZH} G→O	12.0/14.0
CD54/74FCT844	t_{PLH}, t_{PHL} D→Q	11.0/14.0
	t_{PLH}, t_{PHL} E→Q	12.0/14.0
	t_{su} D→E	3.0/3.0
	t_h E→D	4.0/4.0
	t_w	6.0/9.0
	t_{PLH}, t_{PHL} R,S→Q	13.0/15.0
	t_{su} S→E	4.0/4.0
	t_{su} R→E	3.0/3.0
	t_w R,S	8.0/12.0
	t_{PLZ}, t_{PHZ} G→O	12.0/14.0
	t_{PZL}, t_{PZH} G→O	12.0/14.0

Table XXIII - Three-State Switching Parameters

Type Number	Descriptive Symbol	COM'L/MIL Limits (ns)
CD54/74FCT240	t_{PLZ}, t_{PHZ} G→O	9.5/12.5
	t_{PZL}, t_{PZH} G→O	10.0/10.5
CD54/74FCT244	t_{PLZ}, t_{PHZ} G→O	7.0/7.5
	t_{PZL}, t_{PZH} G→O	8.0/8.5
CD54/74FCT245	t_{PLZ}, t_{PHZ} G→O	7.5/10.0
	t_{PZL}, t_{PZH} G→O	9.5/10.0
CD54/74FCT373	t_{PLZ}, t_{PHZ} G→O	7.5/10.0
	t_{PZL}, t_{PZH} G→O	12.0/13.5
CD54/74FCT374	t_{PLZ}, t_{PHZ} G→O	8.0/8.0
	t_{PZL}, t_{PZH} G→O	12.5/14.0
CD54/74FCT533	t_{PLZ}, t_{PHZ} G→O	7.0/8.5
	t_{PZL}, t_{PZH} G→O	11.0/12.5
CD54/74FCT534	t_{PLZ}, t_{PHZ} G→O	8.0/8.0
	t_{PZL}, t_{PZH} G→O	12.5/14.0