TQFP
Commercial Temp
Industrial Temp

128K x 36
4Mb Sync Burst SRAM

250 MHz–150 MHz
3.3 V V_{DD}
3.3 V and 2.5 V I/O

Features

- $\overline{FT}$ pin for user-configurable flow through or pipelined operation
- Single Cycle Deselect (SCD) operation
- 3.3 V +10%/–5% core power supply
- 2.5 V or 3.3 V I/O supply
- $\overline{LBO}$ pin for Linear or Interleaved Burst mode
- Internal input resistors on mode pins allow floating mode pins
- Default to Interleaved Pipelined mode
- Byte Write ($\overline{BW}$) and/or Global Write ($\overline{GW}$) operation
- Common data inputs and data outputs
- Clock control, registered, address, data, and control
- Internal self-timed write cycle
- Automatic power-down for portable applications
- RoHS-compliant 100-lead TQFP package

Functional Description

Applications

The GS84036CGT is a 4,718,592-bit high performance synchronous SRAM with a 2-bit burst address counter. Although of a type originally developed for Level 2 Cache applications supporting high performance CPUs, the device now finds application in synchronous SRAM applications ranging from DSP main store to networking chip set support. The GS84036CGT is available in a JEDEC standard 100-lead TQFP package.

Controls

Addresses, data I/Os, chip enables ($\overline{E}_1$, E_2, $\overline{E}_3$), address burst control inputs ($\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$), and write control inputs ($\overline{Bx}$, $\overline{BW}$, $\overline{GW}$) are synchronous and are controlled by a positive-edge-triggered clock input (CK). Output enable ($\overline{G}$) and power down control (ZZ) are asynchronous inputs. Burst cycles can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ inputs. In Burst mode, subsequent burst addresses are generated internally and are controlled by $\overline{ADV}$. The burst address counter may be configured to count in either linear or interleave order with the Linear Burst Order ($\overline{LBO}$) input. The burst function need not be used. New addresses can be loaded on every cycle with no degradation of chip performance.

Flow Through/Pipeline Reads

The function of the Data Output register can be controlled by the user via the $\overline{FT}$ mode pin/bump (pin 14 in the TQFP and bump 5R in the BGA). Holding the $\overline{FT}$ mode pin/bump low places the RAM in Flow Through mode, causing output data to bypass the Data Output Register. Holding $\overline{FT}$ high places the RAM in Pipelined mode, activating the rising-edge-triggered Data Output Register.

SCD Pipelined Reads

The GS84036CGT is an SCD (Single Cycle Deselect) pipelined synchronous SRAM. DCD (Dual Cycle Deselect) versions are also available. SCD SRAMs pipeline deselect commands one stage less than read commands. SCD RAMs begin turning off their outputs immediately after the deselect command has been captured in the input registers.

Byte Write and Global Write

Byte write operation is performed by using byte write enable ($\overline{BW}$) input combined with one or more individual byte write signals ($\overline{Bx}$). In addition, Global Write ($\overline{GW}$) is available for writing all bytes at one time, regardless of the Byte Write control inputs.

Sleep Mode

Low power (Sleep mode) is attained through the assertion (High) of the ZZ signal, or by stopping the clock (CK). Memory data is retained during Sleep mode.

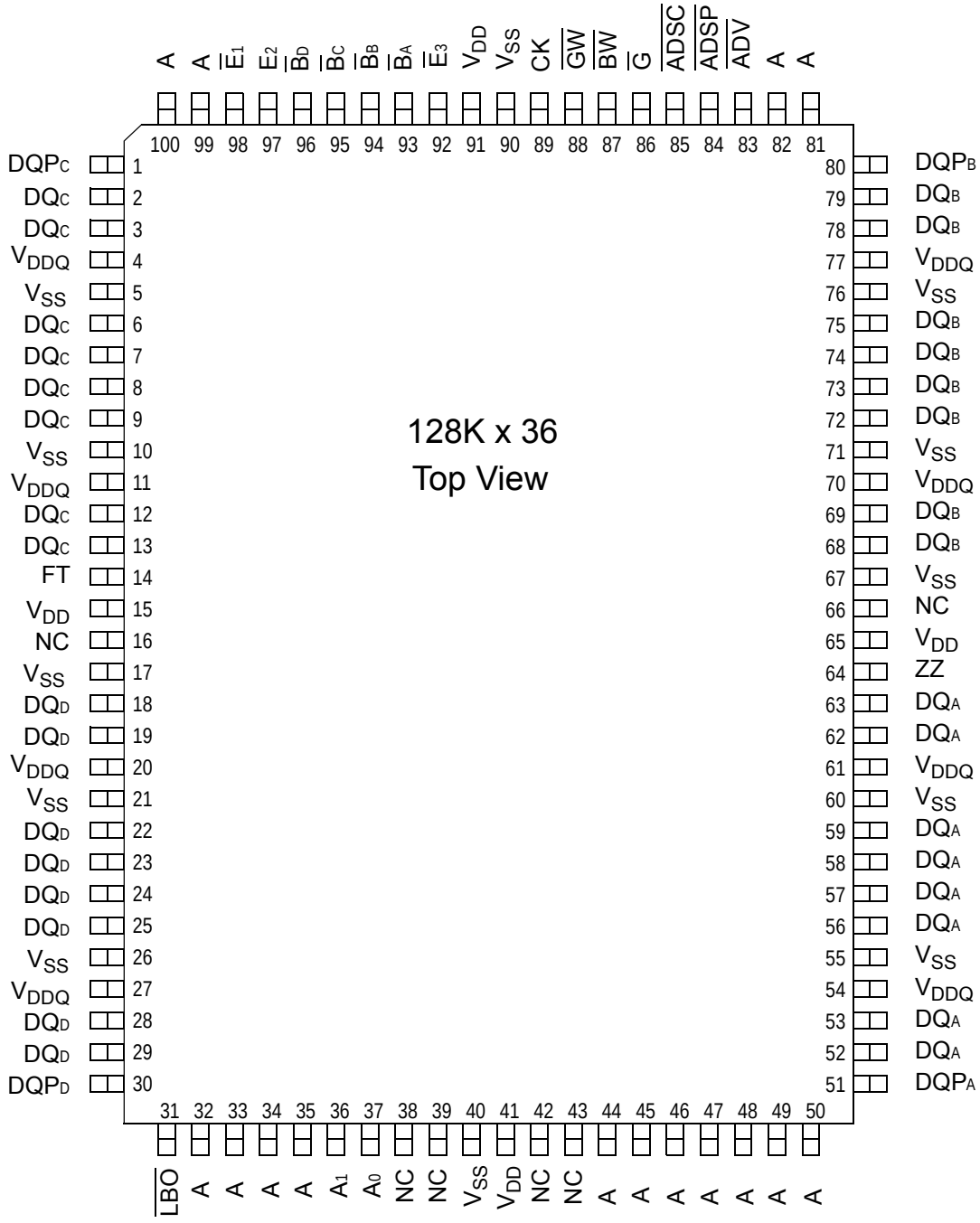
Core and Interface Voltages

The GS84036CGT operates on a 3.3 V power supply and all inputs/outputs are 3.3 V- and 2.5 V-compatible. Separate output power (V_{DDQ}) pins are used to de-couple output noise from the internal circuit.

Parameter Synopsis

		–250	–200	–166	–150	Unit
Pipeline 3-1-1-1	tCycle	4.0	5.5	6.0	6.7	ns
	t_{KQ}	2.5	3.0	3.5	3.8	ns
	Curr	225	195	185	160	MHz
Flow Through 2-1-1-1	t_{KQ}	5.5	6.5	7.0	7.5	ns
	tCycle	5.5	6.5	7.0	7.5	ns
	Curr	180	160	155	145	MHz

GS84036A 100-Pin TQFP Pinout (Package T)

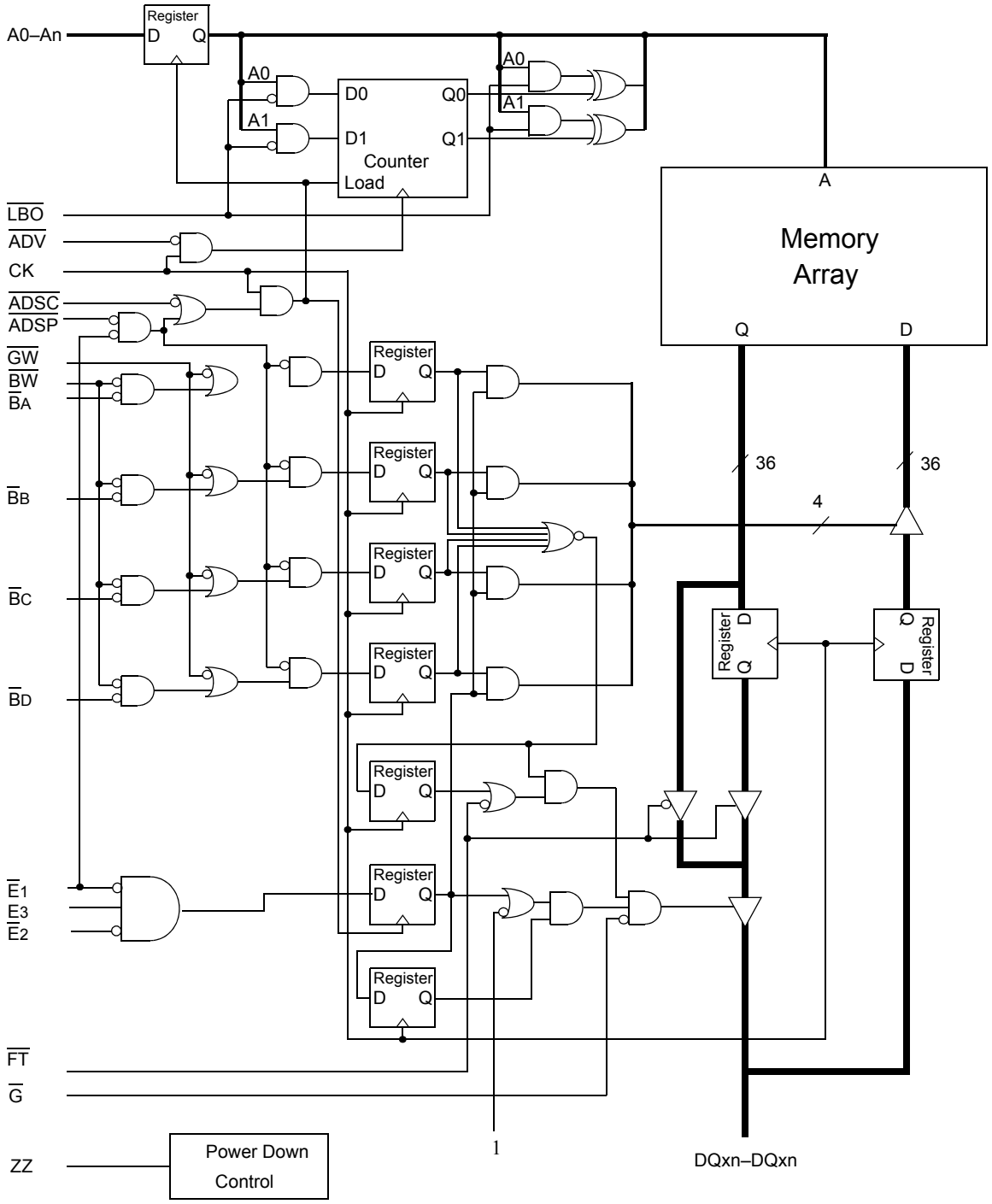


Note:
Pins marked with NC can be tied to either VDD or VSS. These pins can also be left floating.

TQFP Pin Description

Symbol	Type	Description
A_0, A_1	I	Address field LSBs and Address Counter preset Inputs
A	I	Address Inputs
$\overline{B}_A$	In	Byte Write signal for data inputs DQ_A; active low
$\overline{B}_B$	In	Byte Write signal for data inputs DQ_B; active low
$\overline{B}_C$	In	Byte Write signal for data inputs DQ_C; active low
$\overline{B}_D$	In	Byte Write signal for data inputs DQ_D; active low
$\overline{BW}$	I	Byte Write—Writes all enabled bytes; active low
CK	I	Clock Input Signal; active high
$\overline{GW}$	I	Global Write Enable—Writes all bytes; active low
$\overline{E}_1$, $\overline{E}_3$	I	Chip Enable; active low
E_2	I	Chip Enable; active high
$\overline{G}$	I	Output Enable; active low
$\overline{ADV}$	I	Burst address counter advance enable; active low
$\overline{ADSP}$, $\overline{ADSC}$	I	Address Strobe (Processor, Cache Controller); active low
DQ_A	I/O	Byte A Data Input and Output pins
DQ_B	I/O	Byte B Data Input and Output pins
DQ	I/O	Byte C Data Input and Output pins
DQ_D	I/O	Byte D Data Input and Output pins
DQP_A	I/O	9th Data I/O Pin; Byte A
DQP_B	I/O	9th Data I/O Pin; Byte B
DQP_C	I/O	9th Data I/O Pin; Byte C
DQP_D	I/O	9th Data I/O Pin; Byte D
ZZ	I	Sleep Mode control; active high
$\overline{FT}$	I	Flow Through or Pipeline mode; active low
$\overline{LBO}$	I	Linear Burst Order mode; active low
V_{DD}	I	Core power supply
V_{SS}	I	I/O and Core Ground
V_{DDQ}	I	Output driver power supply
NC	-	No Connect

GS84036CGT Block Diagram



Note: Only x36 version shown for simplicity.

Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{LBO}$	L	Linear Burst
		H	Interleaved Burst
Output Register Control	$\overline{FT}$	L	Flow Through
		H or NC	Pipeline
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$

Note:
There is a pull-up device on the $\overline{FT}$ pin and a pull-down device on the ZZ pin , so this input pin can be unconnected and the chip will operate in the default states as specified in the above tables.

Burst Counter Sequences

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note:
The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

Note:
The burst counter wraps to initial state on the 5th clock.

Byte Write Truth Table

Function	$\overline{GW}$	$\overline{BW}$	$\overline{B}_A$	$\overline{B}_B$	$\overline{B}_C$	$\overline{B}_D$	Notes
Read	H	H	X	X	X	X	1
Write No Bytes	H	L	H	H	H	H	1
Write byte a	H	L	L	H	H	H	2, 3
Write byte b	H	L	H	L	H	H	2, 3
Write byte c	H	L	H	H	L	H	2, 3, 4
Write byte d	H	L	H	H	H	L	2, 3, 4
Write all bytes	H	L	L	L	L	L	2, 3, 4
Write all bytes	L	X	X	X	X	X	

Notes:

1. All byte outputs are active in read cycles regardless of the state of Byte Write Enable inputs, $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$ and/or $\overline{B}_D$.
2. Byte Write Enable inputs $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$ and/or $\overline{B}_D$ may be used in any combination with $\overline{BW}$ to write single or multiple bytes.
3. All byte I/Os remain High-Z during all write operations regardless of the state of Byte Write Enable inputs.
4. Bytes "C" and "D" are only available on the x32 and x36 versions.

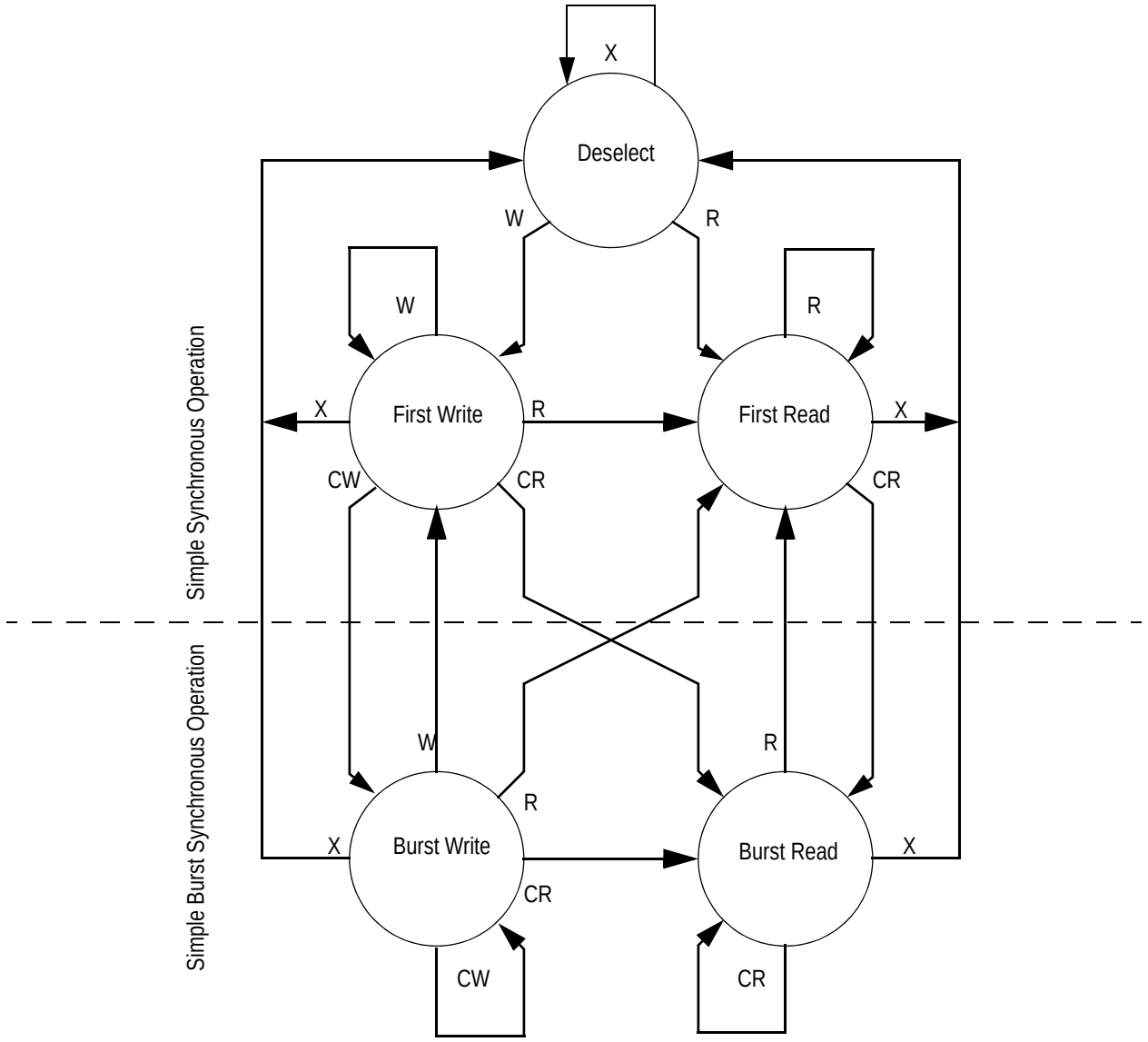
Synchronous Truth Table

Operation	Address Used	State Diagram Key	$\overline{E}_1$	E_2	$\overline{E}_3$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{W}$	DQ^3
Deselect Cycle, Power Down	None	X	L	X	H	X	L	X	X	High-Z
Deselect Cycle, Power Down	None	X	L	L	X	X	L	X	X	High-Z
Deselect Cycle, Power Down	None	X	L	X	H	L	X	X	X	High-Z
Deselect Cycle, Power Down	None	X	L	L	X	L	X	X	X	High-Z
Deselect Cycle, Power Down	None	X	H	X	X	X	L	X	X	High-Z
Read Cycle, Begin Burst	External	R	L	H	L	L	X	X	X	Q
Read Cycle, Begin Burst	External	R	L	H	L	H	L	X	F	Q
Write Cycle, Begin Burst	External	W	L	H	L	H	L	X	T	D
Read Cycle, Continue Burst	*Next*	*CR*	*X*	*X*	*X*	*H*	*H*	*L*	*F*	*Q*
Read Cycle, Continue Burst	Next	CR	H	X	X	X	H	L	F	Q
Write Cycle, Continue Burst	*Next*	*CW*	*X*	*X*	*X*	*H*	*H*	*L*	*T*	*D*
Write Cycle, Continue Burst	Next	CW	H	X	X	X	H	L	T	D
Read Cycle, Suspend Burst	Current		X	X	X	H	H	H	F	Q
Read Cycle, Suspend Burst	Current		H	X	X	X	H	H	F	Q
Write Cycle, Suspend Burst	Current		X	X	X	H	H	H	T	D
Write Cycle, Suspend Burst	Current		H	X	X	X	H	H	T	D

Notes:

1. X = Don't Care, H = High, L = Low
2. E = T (True) if E_2 = 1 and $\overline{E}_1$ = $\overline{E}_3$ = 0; E = F (False) if E_2 = 0 or $\overline{E}_1$ = 1 or $\overline{E}_3$ = 1
3. $\overline{W}$ = T (True) and F (False) is defined in the Byte Write Truth Table preceding.
4. $\overline{G}$ is an asynchronous input. $\overline{G}$ can be driven high at any time to disable active output drivers. $\overline{G}$ low can only enable active drivers (shown as "Q" in the Truth Table above).
5. All input combinations shown above are tested and supported. Input combinations shown in gray boxes need not be used to accomplish basic synchronous or synchronous burst operations and may be avoided for simplicity.
6. Tying $\overline{ADSP}$ high and $\overline{ADSC}$ low allows simple non-burst synchronous operations. See **BOLD** items above.
7. Tying $\overline{ADSP}$ high and $\overline{ADV}$ low while using $\overline{ADSC}$ to load new addresses allows simple burst operations. See *ITALIC* items above.

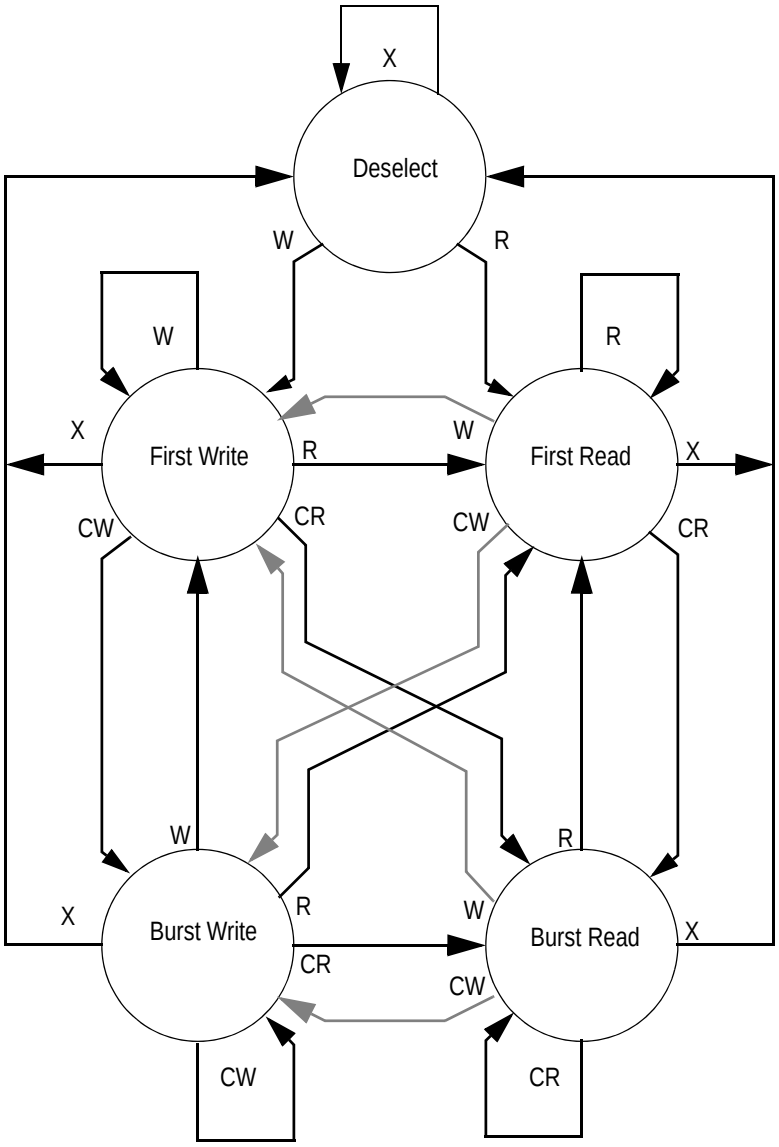
Simplified State Diagram



Notes:

1. The diagram shows only supported (tested) synchronous state transitions. The diagram presumes $\overline{G}$ is tied Low.
2. The upper portion of the diagram assumes active use of only the Enable ($\overline{E}_1$, E_2, $\overline{E}_3$) and Write ($\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$, $\overline{BW}$ and $\overline{GW}$) control inputs and that $\overline{ADSP}$ is tied high and $\overline{ADSC}$ is tied low.
3. The upper and lower portions of the diagram together assume active use of only the Enable, Write and $\overline{ADSC}$ control inputs and assumes $\overline{ADSP}$ is tied high and $\overline{ADV}$ is tied low.

Simplified State Diagram with $\overline{G}$



Notes:

1. The diagram shows supported (tested) synchronous state transitions plus supported transitions that depend upon the use of $\overline{G}$.
2. Use of "Dummy Reads" (Read Cycles with $\overline{G}$ High) may be used to make the transition from Read cycles to Write cycles without passing through a Deselect cycle. Dummy Read cycles increment the address counter just like normal Read cycles.
3. Transitions shown in grey tone assume $\overline{G}$ has been pulsed high long enough to turn the RAM's drivers off and for incoming data to meet Data Input Set Up Time.

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 4.6	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to 4.6	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DDQ} +0.5 (≤ 4.6 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
I_{IN}	Input Current on Any Pin	+/–20	mA
I_{OUT}	Output Current on Any I/O Pin	+/–20	mA
P_D	Package Power Dissipation	1.5	W
T_{STG}	Storage Temperature	–55 to 125	°C
T_{BIAS}	Temperature Under Bias	–55 to 125	°C

Note:

Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

Power Supply Voltage Ranges

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
3.3 V Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
3.3 V V_{DDQ} I/O Supply Voltage	V_{DDQ3}	3.0	3.3	3.6	V	
2.5 V V_{DDQ} I/O Supply Voltage	V_{DDQ2}	2.3	2.5	2.7	V	

Notes:

1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be –2 V > Vi < V_{DDn}+2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.

Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
V_{DD} Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V	1
V_{DD} Input Low Voltage	V_{IL}	–0.3	—	0.8	V	1
V_{DDQ3} I/O Input High Voltage	V_{IHQ3}	2.0	—	V_{DDQ} + 0.3	V	1,3
V_{DDQ3} I/O Input Low Voltage	V_{ILQ3}	–0.3	—	0.8	V	1,3
V_{DDQ2} I/O Input High Voltage	V_{IHQ2}	0.6*V_{DD}	—	V_{DDQ} + 0.3	V	1,3
V_{DDQ2} I/O Input Low Voltage	V_{ILQ2}	–0.3	—	0.3*V_{DD}	V	1,3

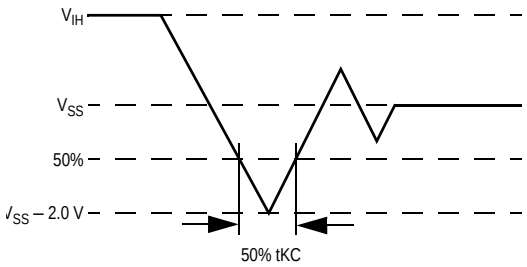
Notes:
1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be –2 V > Vi < V_{DDn}+2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.
3. V_{IHQ} (max) is voltage on V_{DDQ} pins plus 0.3 V.

Recommended Operating Temperatures

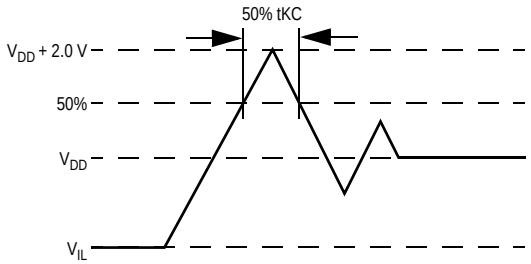
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Ambient Temperature (Commercial Range Versions)	T_A	0	25	70	°C	2
Ambient Temperature (Industrial Range Versions)	T_A	–40	25	85	°C	2

Notes:
1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be –2 V > Vi < V_{DDn}+2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



Capacitance

(T_A = 25°C, f = 1 MHz, V_{DD} = 2.5 V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	4	5	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0 V	6	7	pF

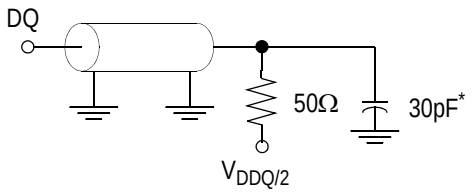
Note:
These parameters are sample tested.

AC Test Conditions

Parameter	Conditions
Input high level	V_{DD} – 0.2 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	V_{DD}/2
Output reference level	V_{DDQ}/2
Output load	Fig. 1

Notes:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted.
3. Device is deselected as defined by the Truth Table.

Output Load 1



* Distributed Test Jig Capacitance

DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DD}	–1 uA	1 uA
ZZ Input Current	I_{IN1}	$V_{DD} \geq V_{IN} \geq V_{IH}$ 0 V ≤ V_{IN} ≤ V_{IH}	–1 uA –1 uA	1 uA 100 uA
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DD}	–1 uA	1 uA
Output High Voltage	V_{OH2}	I_{OH} = –8 mA, V_{DDQ} = 2.375 V	1.7 V	—
Output High Voltage	V_{OH3}	I_{OH} = –8 mA, V_{DDQ} = 3.135 V	2.4 V	—
Output Low Voltage	V_{OL}	I_{OL} = 8 mA	—	0.4 V

Operating Currents

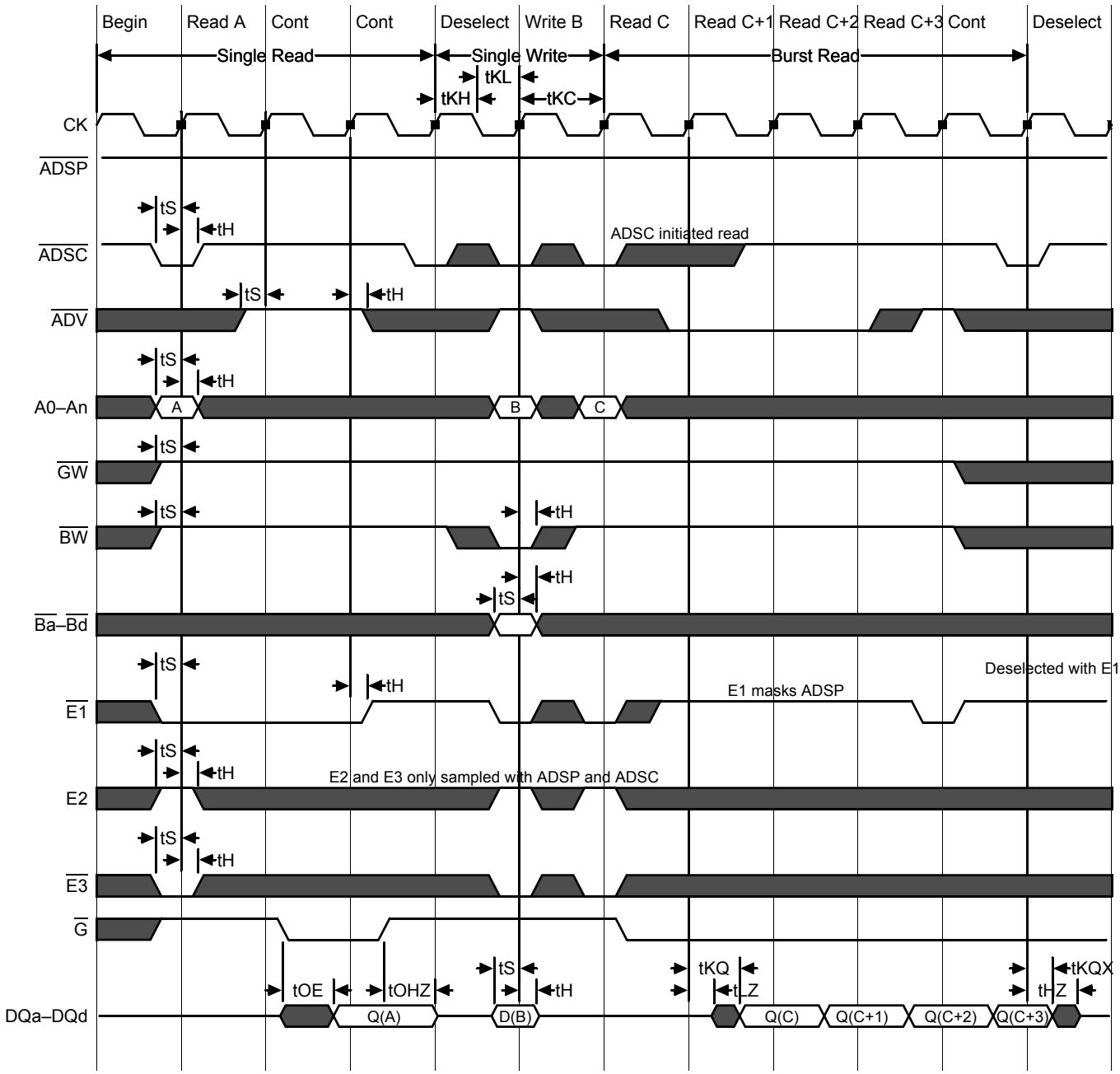
Parameter	Test Conditions	Mode		Symbol	-250		-200		-166		-150		Unit
					0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	
Operating Current	Device Selected; All other inputs ≥V_{IH} or ≤ V_{IL} Output open	(x36)	Pipeline	I_{DD} I_{DDQ}	195 30	215 30	170 25	190 25	160 25	180 25	140 20	160 20	mA
			Flow Through	I_{DD} I_{DDQ}	155 25	175 25	140 20	160 20	135 20	155 20	130 15	150 15	mA
Standby Current	ZZ ≥ V_{DD} – 0.2 V	—	Pipeline	I_{SB}	25	45	25	45	25	45	25	45	mA
			Flow Through	I_{SB}	25	45	25	45	25	45	25	45	mA
Deselect Current	Device Deselected; All other inputs ≥ V_{IH} or ≤ V_{IL}	—	Pipeline	I_{DD}	65	85	65	85	65	85	60	80	mA
			Flow Through	I_{DD}	65	85	65	85	65	85	60	80	mA

AC Electrical Characteristics

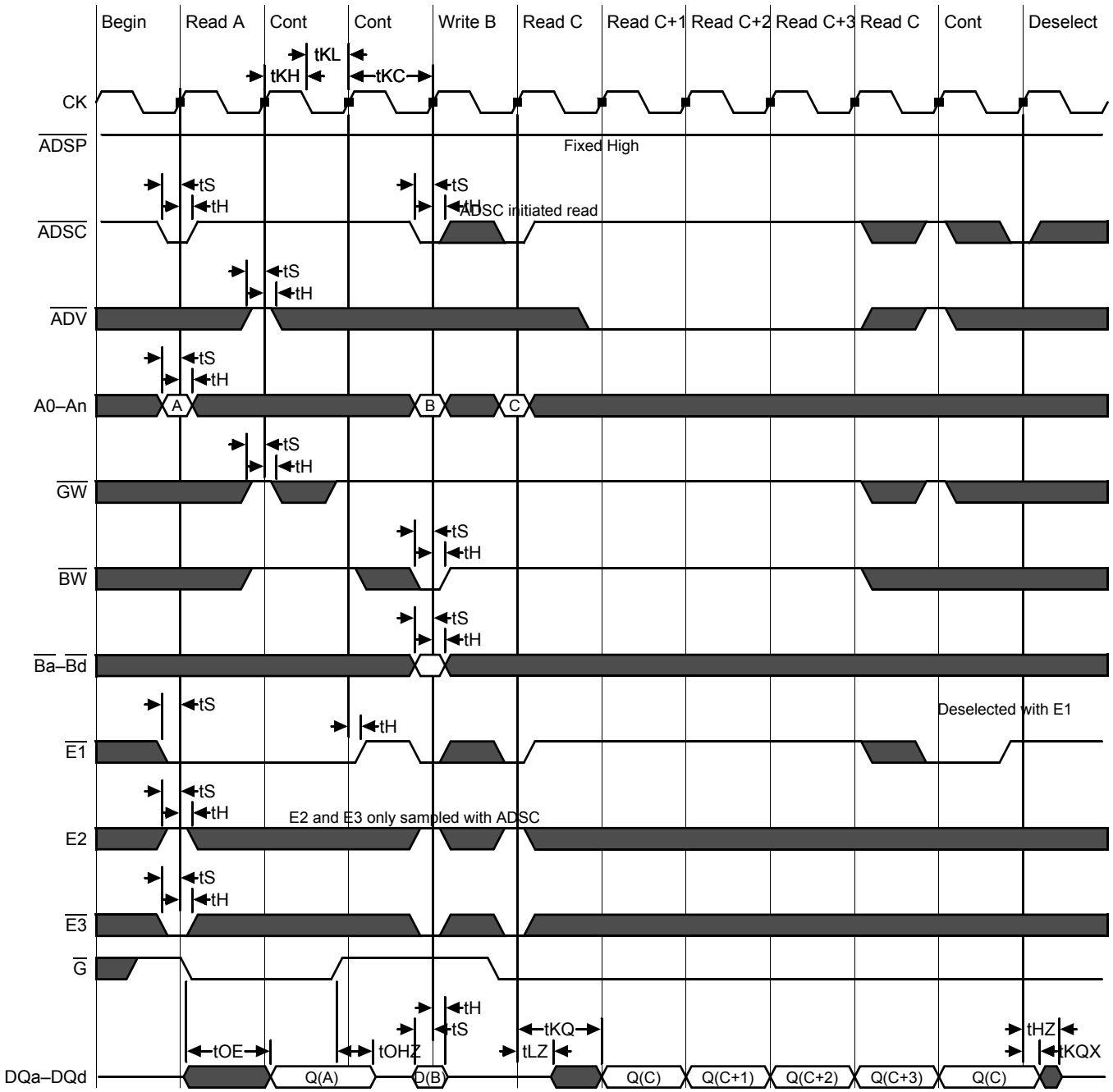
	Parameter	Symbol	-250		-200		-166		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Pipeline	Clock Cycle Time	tKC	4.0	—	5.5	—	6.0	—	6.7	—	ns
	Clock to Output Valid	tKQ	—	2.5	—	3.0	—	3.5	—	3.8	ns
	Clock to Output Invalid	tKQX	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Clock to Output in Low-Z	tLZ[1]	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Setup time	tS	1.2	—	1.4	—	1.5	—	1.5	—	ns
	Hold time	tH	0.2	—	0.4	—	0.5	—	0.5	—	ns
Flow Through	Clock Cycle Time	tKC	5.5	—	6.5	—	7.0	—	7.5	—	ns
	Clock to Output Valid	tKQ	—	5.5	—	6.5	—	7.0	—	7.5	ns
	Clock to Output Invalid	tKQX	2.0	—	2.0	—	2.0	—	2.0	—	ns
	Clock to Output in Low-Z	tLZ[1]	2.0	—	2.0	—	2.0	—	2.0	—	ns
	Setup time	tS	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Hold time	tH	0.5	—	0.5	—	0.5	—	0.5	—	ns
	Clock HIGH Time	tKH	1.3	—	1.3	—	1.3	—	1.3	—	ns
	Clock LOW Time	tKL	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Clock to Output in High-Z	tHZ[1]	1.5	2.5	1.5	3.0	1.5	3.0	1.5	3.0	ns
	$\overline{G}$ to Output Valid	tOE	—	2.5	—	3.0	—	3.5	—	3.8	ns
	$\overline{G}$ to output in Low-Z	tOLZ[1]	0	—	0	—	0	—	0	—	ns
	$\overline{G}$ to output in High-Z	tOHZ[1]	—	2.5	—	3.0	—	3.0	—	3.0	ns
	ZZ setup time	tZZS[2]	5	—	5	—	5	—	5	—	ns
	ZZ hold time	tZZH[2]	1	—	1	—	1	—	1	—	ns
	ZZ recovery	tZZR	20	—	20	—	20	—	20	—	ns

Notes:
1. These parameters are sampled and are not 100% tested
2. ZZ is an asynchronous signal. However, In order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

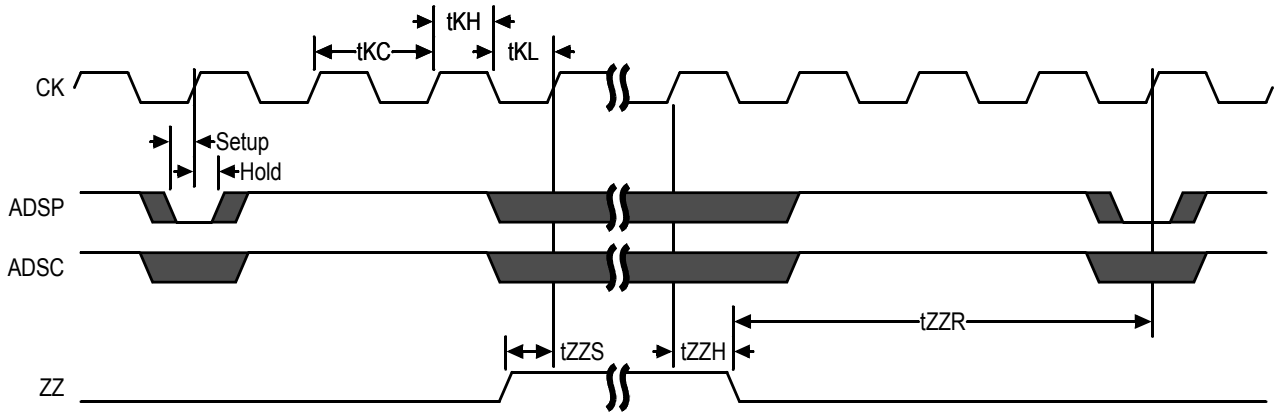
Pipeline Mode Timing



Flow Through Mode Timing



Sleep Mode Timing Diagram



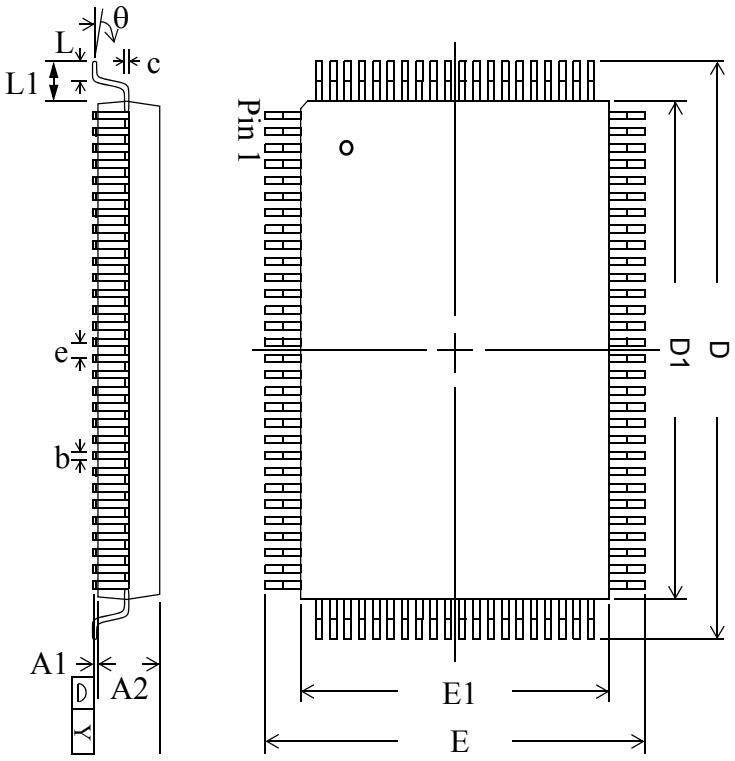
Application Tips

Single and Dual Cycle Deselect

SCD devices force the use of "dummy read cycles" (read cycles that are launched normally but that are ended with the output drivers inactive) in a fully synchronous environment. Dummy read cycles waste performance but their use usually assures there will be no bus contention in transitions from reads to writes or between banks of RAMs. DCD SRAMs do not waste bandwidth on dummy cycles and are logically simpler to manage in a multiple bank application (wait states need not be inserted at bank address boundary crossings), but greater care must be exercised to avoid excessive bus contention.

TQFP Package Drawing (Package GT)

Symbol	Description	Min.	Nom.	Max
A1	Standoff	0.05	0.10	0.15
A2	Body Thickness	1.35	1.40	1.45
b	Lead Width	0.20	0.30	0.40
c	Lead Thickness	0.09	—	0.20
D	Terminal Dimension	21.9	22.0	22.1
D1	Package Body	19.9	20.0	20.1
E	Terminal Dimension	15.9	16.0	16.1
E1	Package Body	13.9	14.0	14.1
e	Lead Pitch	—	0.65	—
L	Foot Length	0.45	0.60	0.75
L1	Lead Length	—	1.00	—
Y	Coplanarity			0.10
θ	Lead Angle	0°	—	7°



Notes:
1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion.

Ordering Information for GSI Synchronous Burst RAMs

Org	Part Number[1]	Type	Package	Speed[2] (MHz/ns)	T_A[3]
128K x 36	GS84036AGT-250	Pipeline/Flow Through	RoHS-compliant TQFP	250/6.5	C
128K x 36	GS84036AGT-200	Pipeline/Flow Through	RoHS-compliant TQFP	200/6.5	C
128K x 36	GS84036AGT-166	Pipeline/Flow Through	RoHS-compliant TQFP	166/7.0	C
128K x 36	GS84036AGT-150	Pipeline/Flow Through	RoHS-compliant TQFP	150/7.5	C
128K x 36	GS84036AGT-250I	Pipeline/Flow Through	RoHS-compliant TQFP	250/6.5	I
128K x 36	GS84036AGT-200I	Pipeline/Flow Through	RoHS-compliant TQFP	200/6.5	I
128K x 36	GS84036AGT-166I	Pipeline/Flow Through	RoHS-compliant TQFP	166/7.0	I
128K x 36	GS84036AGT-150I	Pipeline/Flow Through	RoHS-compliant TQFP	150/7.5	I

Notes:
1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS84036CGT-250T.
2. The speed column indicates the cycle frequency (MHz) of the device in Pipelined mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow through mode-selectable by the user.
3. C = Commercial Temperature Range. I = Industrial Temperature Range.
4. GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsitechnology.com) for a complete listing of current offerings.

9Mb Sync SRAM Datasheet Revision History

Rev. Code: Old; New	Types of Changes Format or Content	Page /Revisions;Reason
84036CGT_r1		• Creation of datasheet

